16. SPI Slave/JTAG to Avalon Master Bridge Cores

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Core Overview

The SPI Slave to Avalon® Master Bridge and the JTAG to Avalon Master Bridge cores provide a connection between host systems and SOPC Builder systems via the respective physical interfaces. Host systems can initiate Avalon Memory-Mapped (Avalon-MM) transactions by sending encoded streams of bytes via the cores' physical interfaces. The cores support reads and writes, but not burst transactions.

The SPI Slave to Avalon Master Bridge and the JTAG to Avalon Master Bridge are SOPC Builder-ready and integrates easily into any SOPC Builder-generated systems.

This chapter contains the following sections:

Functional Description

Figure 16–1 shows a block diagram of the SPI Slave to Avalon Master Bridge core and its location in a typical system configuration.

Figure 16–1. SOPC Builder System with a SPI Slave to Avalon Master Bridge Core

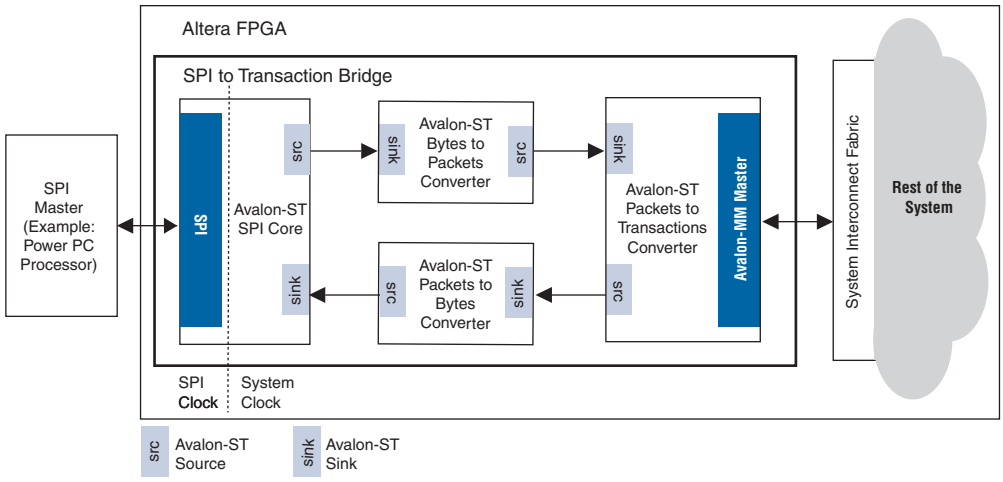
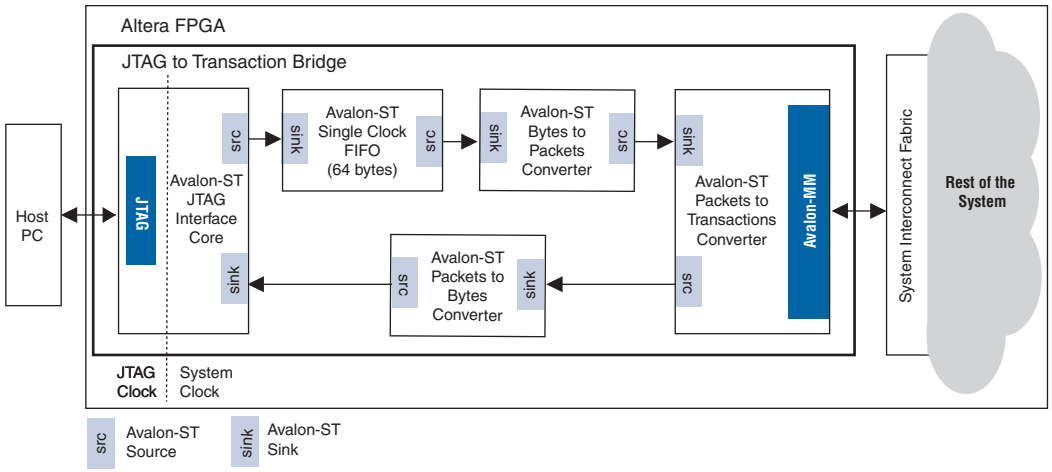


Figure 16–2 shows a block diagram of the JTAG to Avalon Master Bridge core and its location in a typical system configuration.

Figure 16–2. SOPC Builder System with a JTAG to Avalon Master Bridge Core



The SPI Slave to Avalon Master Bridge and the JTAG to Avalon Master Bridge cores accept encoded streams of bytes with transaction data on their respective physical interfaces and initiate Avalon-MM transactions on their Avalon-MM interfaces. Each bridge consists of the following cores, which are available as stand-alone components in SOPC Builder:

- **Avalon-ST Serial Peripheral Interface and Avalon-ST JTAG Interface**—Accepts incoming data in bits and packs them into bytes.
- **Avalon-ST Bytes to Packets Converter**—Transforms packets into encoded stream of bytes, and a likewise encoded stream of bytes into packets.
- **Avalon-ST Packets to Transactions Converter**—Transforms packets with data encoded according to a specific protocol into Avalon-MM transactions, and encodes the responses into packets using the same protocol.
- **Avalon-ST Single Clock FIFO**—Buffers data from the Avalon-ST JTAG Interface core. The FIFO is only used in the JTAG to Avalon Master Bridge.

For the bridges to successfully transform the incoming streams of bytes to Avalon-MM transactions, the streams of bytes must be constructed according to the protocols used by the cores.

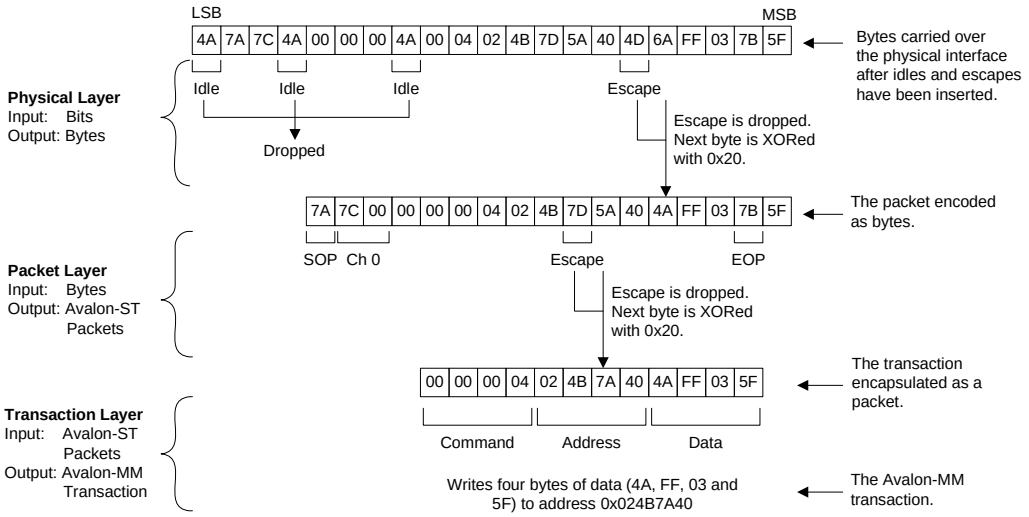
For more information about the protocol at each layer of the bridges and the single clock FIFO, refer to the following chapters:

- *Avalon-ST Serial Peripheral Interface Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST JTAG Interface Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST Bytes to Packets and Packets to Bytes Converter Cores* chapter in volume 5 of the *Quartus II Handbook*

- *Avalon Packets to Transactions Converter Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST Single Clock and Dual Clock FIFO Cores* chapter in volume 5 of the *Quartus II Handbook*

The following example shows how a bytestream changes as it is transferred through the different layers in the bridges.

Figure 16–3. Bits to Avalon-MM Transaction



When the transaction is complete, the bridges send a response to the host system using the same protocol.

Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the SPI Slave to Avalon Master Bridge and the JTAG to Avalon Master Bridge in SOPC Builder to add the cores to a system. There are no user-configurable settings for the JTAG to Avalon Master Bridge core.

For the SPI Slave to Avalon Master Bridge core, the parameter **Number of synchronizer stages: Depth** allows you to specify the length of synchronization register chains. These register chains are used when a metastable event is likely to occur and the length specified determines the meantime before failure. The register chain length, however, affects the latency of the core.

For more information on metastability in Altera devices, refer to *AN 42: Metastability in Altera Devices*. For more information on metastability analysis and synchronization register chains, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Device Support

The SPI Slave to Avalon Master bridge supports all Altera® device families.

Referenced Documents

This chapter references the following documents:

- *Avalon-ST Serial Peripheral Interface Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST JTAG Interface Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST Bytes to Packets and Packets to Bytes Converter Cores* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon Packets to Transactions Converter Core* chapter in volume 5 of the *Quartus II Handbook*
- *Avalon-ST Single Clock and Dual Clock FIFO Cores* chapter in volume 5 of the *Quartus II Handbook*
- *AN 42: Metastability in Altera Devices*
- *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 16–1 shows the revision history for this chapter.

Table 16–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	No change from previous release.	—
March 2009 v9.0.0	Added description of a new parameter **Number of synchronizer stages: Depth**.	—
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—