



Intel FPGA IP

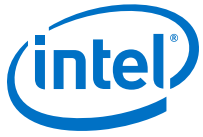
Release Notes

RN-IP
2017.05.15

Last updated for Intel® Quartus® Prime Design Suite: 17.0

 [Subscribe](#)

 [Send Feedback](#)



Contents

1 Intel FPGA IP Release Notes.....	3
1.1 Errata.....	4



1 Intel FPGA IP Release Notes

These release notes include links to versions 17.0, 16.1, and 16.0 of Intel® FPGA IP cores, including the Intel FPGA IP Library and other IP cores.

- [1G/10GbE and Backplane Ethernet 10GBASE-KR PHY Release Notes](#)
- [10-Gbps Ethernet \(10GbE\) MAC IP Core Release Notes](#)
- [1G/2.5G/10G Multi-rate Ethernet PHY Release Notes](#)
- [10GBASE-R PHY IP Core Release Notes](#)
- [25G Ethernet IP Core Release Notes](#)
- [40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes](#)
- [50G Ethernet IP Core Release Notes](#)
- [50G Interlaken IP Core Release Notes](#)
- [100G Interlaken IP Core Release Notes](#)
- [Arria V GZ Hard IP for PCI Express IP Core Release Notes](#)
- [Arria V Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Release Notes](#)
- [Arria 10 External Memory Interface IP Core Release Notes](#)
- [Arria 10 FPLL IP Core Release Notes](#)
- [Arria 10 Hard IP for PCI Express IP Core Release Notes](#)
- [Arria 10 Transceiver ATX PLL IP Core Release Notes](#)
- [Arria 10 Transceiver CMU PLL IP Core Release Notes](#)
- [Arria 10 Transceiver Native PHY IP Core Release Notes](#)
- [BCH IP Core Release Notes](#)
- [CIC IP Core Release Notes](#)
- [CPRI IP Core Release Notes](#)
- [Cyclone V Hard IP for PCI Express IP Core Release Notes](#)
- [DDR2 and DDR3 SDRAM Controller with UniPHY IP Core Release Notes](#)
- [DisplayPort IP Core Release Notes](#)
- [FIR II IP Core Release Notes](#)
- [FFT IP Core Release Notes](#)
- [HDMI IP Core Release Notes](#)
- [High-speed Reed-Solomon IP Core Release Notes](#)
- [Hybrid Memory Cube Controller IP Core Release Notes](#)
- [Interlaken PHY IP Core Release Notes](#)

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.

ISO
9001:2008
Registered



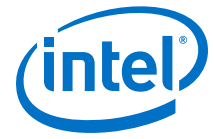
- [IP Compiler for PCI Express Release Notes](#)
- [JESD204B IP Core Release Notes](#)
- [LDPC IP Core Release Notes](#)
- [Low Latency 100-Gbps Ethernet IP Core Release Notes](#)
- [Low Latency 40-Gbps Ethernet IP Core Release Notes](#)
- [Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes](#)
- [Low Latency Ethernet 10G MAC IP Core Release Notes](#)
- [Nios II Processor IP Core Release Notes](#)
- [NCO IP Core Release Notes](#)
- [QDR II and QDR II+ SRAM Controller with UniPHY IP Core Release Notes](#)
- [RapidIO IP Core Release Notes](#)
- [RapidIO II IP Core Release Notes](#)
- [Reed-Solomon II IP Core Release Notes](#)
- [RLDRAM II Controller with UniPHY and RLDRAM 3 PHY-Only IP Core Release Notes](#)
- [SDI IP Core Release Notes](#)
- [SDI II IP Core Release Notes](#)
- [SDI Audio IP Cores Release Notes](#)
- [SerialLite II Release Notes](#)
- [SerialLite III Streaming IP Core Release Notes](#)
- [SmartVID Controller IP Core Release Notes](#)
- [Stratix V Hard IP for PCI Express IP Core Release Notes](#)
- [Triple Speed Ethernet IP Core Release Notes](#)
- [Turbo IP Core Release Notes](#)
- [Video and Image Processing Suite Release Notes](#)
- [Viterbi IP Core Release Notes](#)
- [V-Series Avalon-MM DMA for PCI Express IP Core Release Notes](#)
- [XAUI PHY Release Notes](#)
- [Other IP Cores Release Notes](#)
- [Other Transceiver IP Cores Product Release Notes](#)

Related Links

- [Introduction to Intel FPGA IP Cores](#)
- [Intel FPGA Software Installation and Licensing](#)

1.1 Errata

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.



For full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Altera website.

Related Links

[Altera Knowledge Base](#)