

# Cyclone III FPGA Features

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		Maximum Resource Count for Cyclone III FPGAs (1.2 V)							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Resources	LEs (K)	5	10	15	25	40	56	81	119
	M9K memory blocks	46	46	56	66	126	260	305	432
	Embedded memory (Kb)	414	414	504	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	23	23	56	66	126	156	244	288
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4
	Design security	-							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, LVPECL, SSTL-18 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), Differential HSTL							
	Emulated LVDS channels, 840 Mbps	66	66	136	79	223	159	177	229
	OCT	Series and differential							
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR							

# Cyclone III LS FPGA Features

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		Maximum Resource Count for Cyclone III LS FPGAs (1.2 V)			
		EP3CLS70	EP3CLS100	EP3CLS150	EP3CLS200
Resources	LEs (K)	70	100	151	198
	M9K memory blocks	333	483	666	891
	Embedded memory (Kb)	2,997	4,347	5,994	8,019
	18 x 18 multipliers	200	276	320	396
Architectural Features	Global clock networks	20			
	PLLs	4			
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, LVPECL, SSTL-18 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), Differential HSTL			
	LVDS channels, 840 Mbps	169			
	OCT	Series and differential			
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR			

# Cyclone III Series Package and I/O Matrices


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Cyclone III FPGAs (1.2 V)								
EQFP (E)	MBGA (M) <sup>1</sup>	PQFP (Q) <sup>2</sup>	FBGA (F)				UBGA (U)	
144 pin 22 x 22 (mm) 0.5 mm pitch	164 pin 8 x 8 (mm) 0.5 mm pitch	240 pin 34.6 x 34.6 (mm) 0.5 mm pitch	256 pin 17 x 17 (mm) 1.0 mm pitch	324 pin 19 x 19 (mm) 1.0 mm pitch	484 pin 23 x 23 (mm) 1.0 mm pitch	780 pin 29 x 29 (mm) 1.0 mm pitch	256 pin 14 x 14 (mm) 0.8 mm pitch	484 pin 19 x 19 (mm) 0.8 mm pitch
EP3C5	94	106	182				182	
EP3C10	94	106	182				182	
EP3C16	84	92	160	168	346		168	346
EP3C25	82		148	156	215		156	
EP3C40			128	196	331	535		331
EP3C55					327	377		327
EP3C80					295	429		295
EP3C120					283	531		
EP3CLS70					294	429		294
EP3CLS100					294	429		294
EP3CLS150					226	429		
EP3CLS200					226	429		

Notes:

1. Micro FineLine BGA.
2. Plastic quad flat pack.

**636** Number indicates available user I/O pins.

 Vertical migration (same V<sub>cc</sub>, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.