

## 1 Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Medium Access Control) and PCS (Physical Coding Sub-layer) Cores.

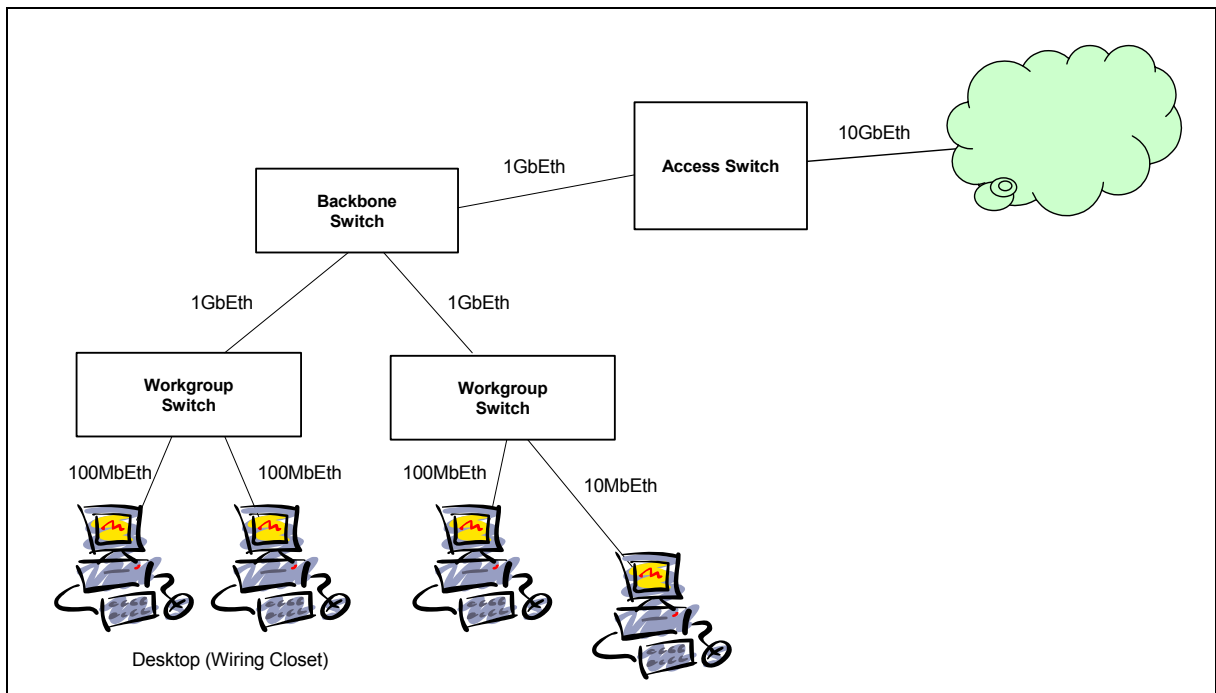


Figure 1: Enterprise LAN Topology Example

The programmable 10/100/100 Ethernet MAC from MorethanIP provides, with a single IP Core solution, a solution for Ethernet applications (Line Card, NIC card or switching) operating at 10/100 or 1000Mbps (Gigabit Ethernet). The 10/100/1000 MAC Core can operate in Half (With 10/100Mbps operation only) or Full Duplex mode, supports transparent (For switching applications) and full Ethernet frame termination / generation (For NIC or line cards applications).

The Core implements a low pin count SGMII which integrates a 1000Base-X compliant with Clause 36 of the IEEE802.3 standard and implements 8B/10B coding, link synchronization, frame encapsulation generation / termination. The Core also supports Auto-Negotiation (Clause 37 or IEEE802.3 standard), which is used to automatically, or under user application software control, exchange ability information between the Core and the remote end of the link and configure the Core to take the best advantage on the advertised features of the Remote node.

The core can seamlessly connect to any industry standard 10/100/1000 Ethernet SERDES (SERializer / DESerializer) device via a SGMII (Serial Gigabit Medium Independent Interface) and to a user application via a SOC (System on a Chip) interface, which provides seamless connectivity to any MorethanIP cores such as Flexbus, POS-PHY interfaces.

The core is optionally delivered in generic synthesizable HDL code (For use in FPGA or ASIC technologies), or as a FPGA netlist, which provides a lower cost solution.

## 2 10/100/1000 Ethernet MAC Core Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively
- Seamless interface to commercial Gigabit 10/100/1000 PHY device via a serial 1.25Gbps SGMII (Serial GMII) interface
- Implements low pin count SGMII (Serial GMII) interface to commercial Ethernet PHY of SFP modules
- Supports AMD Magic Packet detection for node remote power down management
- Supports, for 10/100Mbps operation, full duplex or half duplex operation selectable via a Core configuration option
- Optional PMA (Physical Medium Attachment) SERDES when implemented in Altera Stratix GX
- Simple FIFO interface to user application compatible with Altera Atlantic specification
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Fully automated Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention
- Pause frame generation with dynamically programmable 16-Bit Quanta
- Pause frame generation additionally controllable by user application offering flexible traffic flow control
- Optional forwarding of received pause frames to the MAC Client User application
- Support any type of Ethernet Frames such as SNAP / LLC or IP traffic
- Supports Unicast, Multicast and Broadcast Ethernet frames
- Support for VLAN tagged frames according to IEEE 802.1Q
- Programmable node Unicast MAC address with insertion on transmit and frame filtering on receive
- Programmable Promiscuous mode support to accept all Unicast MAC frames regardless of their destination MAC address
- Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Dynamically programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Implements PCS frame encapsulation / de-encapsulation with /S/, /T/ orderset insertion / termination and // Idle ordered set generation during inter-packet gap
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Implement User controllable 1000Base-X Auto-Negotiation

**Product Brief**  
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- Statistic indicators provide support for IEEE 802.3 basic and mandatory Management Information Database (MIB) package, Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819) enabling implementation in SNMP management environments
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels ensuring data rates of 1Gbps with full back-to-back frame transfer support
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag and error information
- Optional statistic and configuration space providing a generic processor interface delivered with C software package
- Optional MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- Optional internal loopback implemented on the Core internal GMII (Gigabit Medium Independent Interface) interface.

### 3 Core Block Diagram

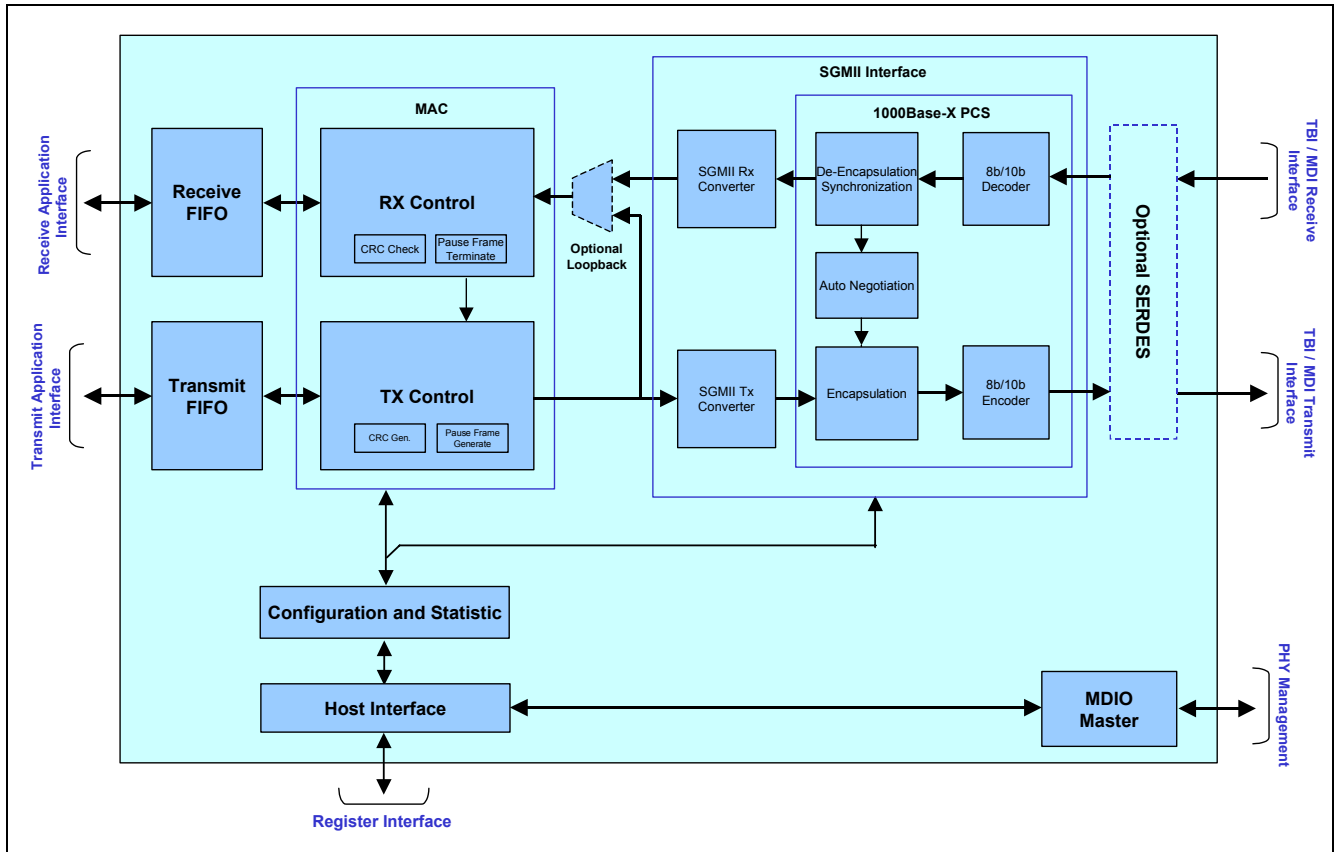


Figure 2: 10/100/1000 Ethernet with SGMII Core Overview

### 4 Implementation Summary

Table 1: Gigabit Ethernet MAC / PHY Core

Target Device Family	Speed Grade	Complexity (With 256 Bytes FIFOs)	Performance	Requirement
STRATIX	-7	4900 LEs	137MHz	125MHz
STRATIX II	-5	4400 LEs <sup>(1)</sup>	152MHz	125MHz
CYCLONE	-8	5000 LEs	127MHz	125MHz
CYCLONE II	-8	5000 LEs	132MHz	125MHz

1. The Logic Element count for Stratix II devices is based on the number of adaptive look-up tables (ALUTs) used for the design as reported by the Quartus II software.

Table 2: Gigabit Ethernet MAC / PHY Core with Integrated SERDES

Target Device Family	Speed Grade	Complexity (With 256 Bytes FIFOs)	Performance	Requirement
STRATIX GX	-7	4900 LEs	140MHz	125MHz

## 5 Gigabit Ethernet MAC / PHY Core Design Kit Overview

Table 3: Design Kit Overview

<i>Design and Simulation</i>	
Language	VHDL / Verilog Source Code or Encrypted VHDL / Verilog Sources Code for Altera FPGAs.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<i>Supported Design Tools</i>	
Simulation	Modelsim Version 5.7a or higher.
Synthesis	Altera Quartus II V4.1 or Higher
Implementation	Altera Quartus II V4.1 or Higher

## 6 References

1. IEEE 802.3 2002 Edition
2. IEEE 802.1Q 1998 Edition
3. RFC2665, Definitions of Managed Objects for the Ethernet-like Interface Type, [www.ietf.org](http://www.ietf.org)
4. RFC2863, The interfaces Group MIB, [www.ietf.org](http://www.ietf.org)

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