The Truth About Die Size: Comparing Stratix & Virtex-II Pro FPGAs

Introduction

Historically, measuring available logic resources in devices from different FPGA vendors has been difficult, due to the lack of a standardized metric for measuring the programmable resources. While "gates" have been used as a proxy for logic capacity, this has proven to be highly variable, even between different products from the same vendor. This lack of a standard metric creates confusion, especially when comparing competitive products.

On December 18th 2002, a Xilinx press release claimed that Virtex-II Pro has a die size advantage of 35% over competing FPGAs. This press release specifically ties to messaging in a Xilinx corporate presentation that illustrates the comparison to Stratix™ FPGAs. The claims in that comparison are erroneous and misleading. In the comparison, Xilinx compares a Virtex-II Pro device with a much larger Stratix device that has 38% more logic resources.

This white paper objectively compares the die sizes for Virtex-II Pro and Stratix devices by comparing devices with similar logic resources. Devices are normalized to 4-input look-up-table (LUT) counts (LUTs are the primary building block of both architectures). This white paper also demonstrates that Stratix FPGAs have smaller die sizes, as compared to equivalent Virtex-II Pro devices, due to the benefits of Altera's patented redundancy technology. In fact, as a result of redundancy, Stratix devices have an effective die size 15% smaller than Virtex-II Pro.

More details on the benchmark analysis and architectural comparisons that are used as the basis for device comparison in this white paper can be found in a companion white paper, "An Analytical Review of FPGA Logic Efficiency in Stratix, Virtex-II & Virtex-II Pro Devices."

Understanding Resource Nomenclature

In order to make a fair comparison of die size, devices with similar resources need to be compared. Measuring resources between Stratix devices and Virtex-II Pro is not intuitive because each vendor uses a different metric to describe device capacity. Altera uses the metric of logic elements (LEs), which are a measurable and quantified device resource on the chip that directly correlate to the number of LUTs. LEs are used consistently in Altera's development tools and documentation.

Xilinx uses a different approach. In their development tools, and much of their technical documentation, they use LUTs and Slices to describe the resource usage for their FPGAs. However, in other documentation, they use the term logic cell (LC). There is no way to physically count LCs, because they are merely a translated metric from the true device resources. A comparison of LCs to LUTs shows that the LC count is inflated by 12.5% over the LUT resources.

Since Altera's LEs and Xilinx's LCs are not based on the same assumptions, it is clear that these metrics cannot fairly be used to compare the capacity of competitive devices. More recently, Xilinx introduced another metric, the "equivalent LE." Equivalent LEs further distort actual device resources, and will be covered in more depth later in this white paper.

In general, each generation of FPGA products has increased logic efficiency so that fewer LUTs are consumed to implement any given function. Over time, the average efficiency advantage of one FPGA architecture over its competitor has varied by as much as 10%. As described in "An Analytical Review of FPGA Logic Efficiency in Stratix, Virtex-II & Virtex-II Pro Devices," Altera's benchmarks show that Stratix devices enjoy the advantage today against Virtex-II Pro. Since the amount of resources that each design uses in different products can vary significantly, the only true method for comparison is to benchmark the individual design. However, the best way for a rough comparison is to use the common architectural feature, the four-input LUT. Both the Stratix and Virtex-II Pro products are based on 4-input LUTs, and the LUT has become the most commonly understood metric of logic resources in FPGAs. In fact, the use of LUTs or thousands of LUTs (KLUTs) has been prominently used as comparison metrics in forums such as the COMP.ARCH.FPGA bulletin board and the FPGA.CPU.ORG website (www.fpgacpu.org/log/sep02.html#020923 and www.fpgacpu.org/log/jan01.html#010116).

The Delta Between LUTs and Xilinx LCs

The number of 4-input LUTs in the Stratix and Virtex-II Pro devices is shown in Table 1. In Stratix devices, there is 1 LE for every LUT. However, in Virtex devices there are 1.125 LCs for every LUT. This means the logic capacity of the Virtex-II Pro devices are overstated by 12.5%.

Table 1. LUT, Logic Element & Logic Cell Counts, as Shown in the Device Data Sheets

Device	4-Input LUTs (1) (2)	Altera LEs (1)	Xilinx Claimed LCs (3)	% Delta (4)
Stratix EP1S20	18,460	18,460	-	0%
Stratix EP1S25	25,660	25,660	-	0%
Virtex-II Pro XC2VP20	18,560	-	20,880	12.5%
Virtex-II Pro XC2VP30	27,392	-	30,816	12.5%

Notes to Table 1:

(1) Source: Stratix FPGA Family Data Sheet.
(2) Source: Virtex-II Pro data sheet, DS083-2, v2.4, page 32, Table 16, "Virtex-II Pro Logic Resources Available in All CLBs."
(3) Source: Virtex-II Pro data sheet, DS083-1, v2.3, page 1, Table 1, "Virtex-II Pro FPGA Family Members."
(4) Delta measures % difference between 4-input LUTs and claimed Logic Cell count.

Xilinx New Metric: "Equivalent LEs"

In addition to the Logic Cell delta, Xilinx also claims an architectural efficiency over Stratix devices with Virtex-II and Virtex-II Pro in the white paper "Comparing Virtex-II and Stratix Logic Utilization." Xilinx uses this claimed efficiency as the basis to create a new term called Xilinx "Equivalent LEs." Using this metric raises the delta over actual LUTs to 25%, as shown in Table 2. As described below, benchmark results do not support this claim.

Table 2. Xilinx Claimed "Effective LEs" for Architectural Efficiency

Device	4-Input LUTs	Altera LEs	Xilinx Claimed LCs	Claimed Xilinx "Equivalent LEs" (1)	% Delta (2)
Stratix EP1S20	18,460	18,460	-	-	0%
Virtex-II Pro XC2VP20	18,560	-	20,880	23,200	25%
Stratix EP1S25	25,660	25,660	-	-	0%
Virtex-II Pro XC2VP30	27,392	-	30,816	34,240	25%

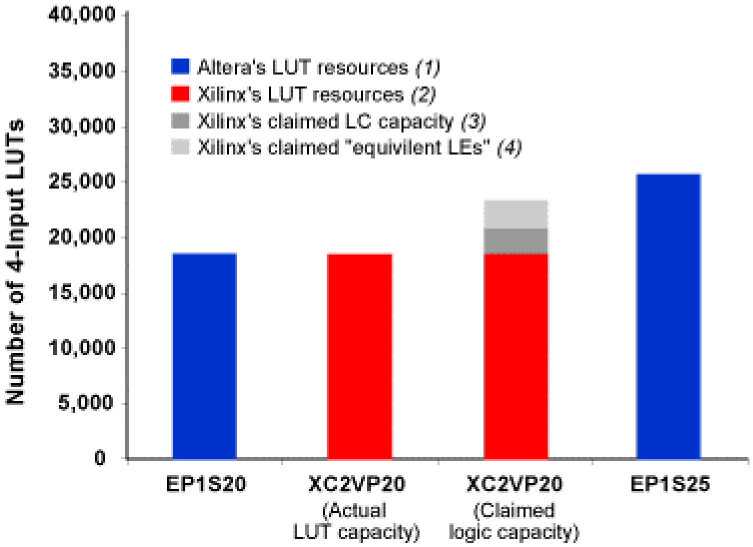
Notes to Table 2:

(1) Source: Xilinx corporate presentations and Xilinx white paper.

(2) Delta measures % difference between 4-input LUTs and claimed "Xilinx LEs."

Using the Xilinx "Equivalent LE" count makes the XC2VP20 appear to be only slightly smaller than the Stratix EP1S25 and should be used for die size comparisons. In reality, the Virtex-II Pro XC2VP20 is much smaller than the EP1S25. A comparison of actual resources shows that the EP1S25 has 7,100 more LUTs (38% more) than the XC2VP20. An accurate comparison is between the XC2VP20 and the EP1S20, which are nearly identical in terms of LUT count. Figure 1 gives a visual representation of actual LUT resources versus the inflated LC and "Xilinx LE" metrics.

Figure 1. Logic Resources in Stratix and Virtex-II Pro Devices



Notes to Figure 1:

(1) Actual LUT resources, as shown in the Stratix data sheet.

(2) Actual LUT resources, as shown in the Virtex-II Pro data sheet.

(3) Logic Cell count in Virtex-II Pro data sheet.

(4) Xilinx "Equivalent LEs", as seen in a Xilinx corporate presentation.

Theory vs. Measurement

In conjunction with this white paper, a companion white paper, “An Analytical Review of FPGA Logic Efficiency in Stratix, Virtex-II & Virtex-II Pro Devices,” reviews benchmarks that compare device efficiencies between Stratix and Virtex-II series FPGAs. The conclusions are based on a suite of 97 customer designs that show Stratix FPGAs are on average 9% more efficient in logic usage (LUTs) than Virtex-II Pro devices. These push-button results are achieved without optimizations for either architecture.

It is important to note that there is a wide variation across the benchmarks. Both architectures offer unique architectural differences and features such as different memory structures, dedicated DSP functions, multiplexers, etc. These features can affect logic utilization efficiency. Some designs are much more efficient in Stratix devices while others are more efficient in Virtex-II families. Ultimately, customers need to do their own analyses to determine the more efficient architecture for their specific design.

True Device and Die Size Comparison

Table 3 shows that normalizing these devices to true 4-input LUTs provides a significantly different picture. The gap in die size is narrowed dramatically by comparing similar devices. It shows that the actual die size difference is about 13%. However, Altera’s Stratix family includes patented redundancy technology to increase yields, which in effect is equivalent to reducing the die size. If the redundancy circuitry were not included, the die size difference would be less than 5%. However, the inclusion of the redundancy circuitry gives the Stratix devices an effective die size that is 15% smaller than Virtex-II Pro.

Table 3. Die Size Normalized to 4-Input LUT Resources

Device	4-Input LUTs	Die Size Normalized to XC2VP20 (1)
Stratix EP1S20	18,460	1.13
Virtex-II Pro XC2VP20	18,560	1.00
Stratix EP1S25	25,660	1.39
Virtex-II Pro XC2VP30	27,392	1.35

Note to Table 3:

(1) Source: Die size ratios based on data shown in a Xilinx corporate presentation. While the Xilinx press release claims a 35% die size advantage, the presentation claims a 39% advantage, comparing the EP1S25 to the XC2VP20, hence a ratio of 1.39.

The concept of effective die size is quite simple. Yield is primarily a function of die size and process defect density. For a given process defect density, die size will generally determine the number of good die that come from each wafer. Redundancy significantly raises the good die per wafer. Starting with number of good die that a wafer with redundancy yields, you can work backwards to a die size that would be associated with a product that does not have redundancy. That is the “effective” die size. On smaller Stratix devices, such as the EP1S20, the effective die size is about 75% of the actual die size. For larger devices, the benefit is even greater. Table 4 illustrates the resulting relative die sizes for Stratix and Virtex-II Pro devices, with the impact of redundancy included.

Table 4. Effective Normalized Die Size with Redundancy

Device	4-Input LUTs	Die Size Normalized to XC2VP20 (1)	Effective Normalized Die Size with Redundancy (2) (3)
Stratix EP1S20	18,460	1.13	0.85
Virtex-II Pro XC2VP20	18,560	1.00	1.00
Stratix EP1S25	25,660	1.39	1.04
Virtex-II Pro XC2VP30	27,392	1.35	1.35

Notes to Table 4:

(1) Die size ratios based on data shown in a Xilinx corporate presentation.
(2) Assumes equivalent defects densities, based on production-qualified processes and products.
(3) Stratix FPGAs and the TSMC 0.13-micron process have both moved to a fully qualified, production status.

With redundancy, the effective cost of Stratix devices is much lower than Virtex-II Pro devices with equivalent logic resources. Likewise, Stratix devices can offer significantly more logic for a similar cost.

Conclusion

The most objective means of quantifying the logic resources available in an FPGA is by determining the number of 4-input LUTs it contains. Even with similar device resources and die sizes, two devices may not necessarily have the same cost structure or price. While Stratix and Virtex-II Pro devices have relatively similar die sizes when normalized to device logic resources, Stratix parts take advantage of redundancy to achieve better yields, in the end offering better availability and lower costs. Coupled with higher resource utilization efficiency, Stratix FPGAs make the most of available logic resources, providing the best FPGA value to customers.

Reference

Table 5 provides a density comparison matrix for Stratix and Virtex-II Series FPGAs.

Table 5. Density Comparison in Stratix and Virtex-II Series FPGA Families

Virtex-II		**Virtex-II Pro**		**Stratix**	
Device	**4-Input LUTs (1)**	**Device**	**4-Input LUTs (2)**	**Device**	**4-Input LUTs (3)**
XC2V1000	10,240	XC2VP7	9,856	EP1S10	10,570
XC2V1500	15,360				
XC2V2000	21,504	XC2VP20	18,560	EP1S20	18,460
XC2V3000	28,672	XC2VP30	27,392	EP1S25	25,660
		XC2VP40	38,784	EP1S30	32,470
XC2V4000	46,080	XC2VP50	47,080	EP1S40	41,250
				EP1S60	57,120
XC2V6000	67,584	XC2VP70	66,176		
				EP1S80	79,040
XC2V8000	93,184	XC2VP100	88,192		
		XC2VP125	111,232	EP1S120	114,140

Notes to Table 5:
(1) Virtex-II data sheet, DS031-2, v2.1, page 22, Table 13, “Virtex-II Logic Resources Available in All CLBs.”
(2) Virtex-II Pro data sheet, DS083-2, v2.4, page 32, Table 16, “Virtex-II Pro Logic Resources Available in All CLBs.”
(3) Stratix data sheet.

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