

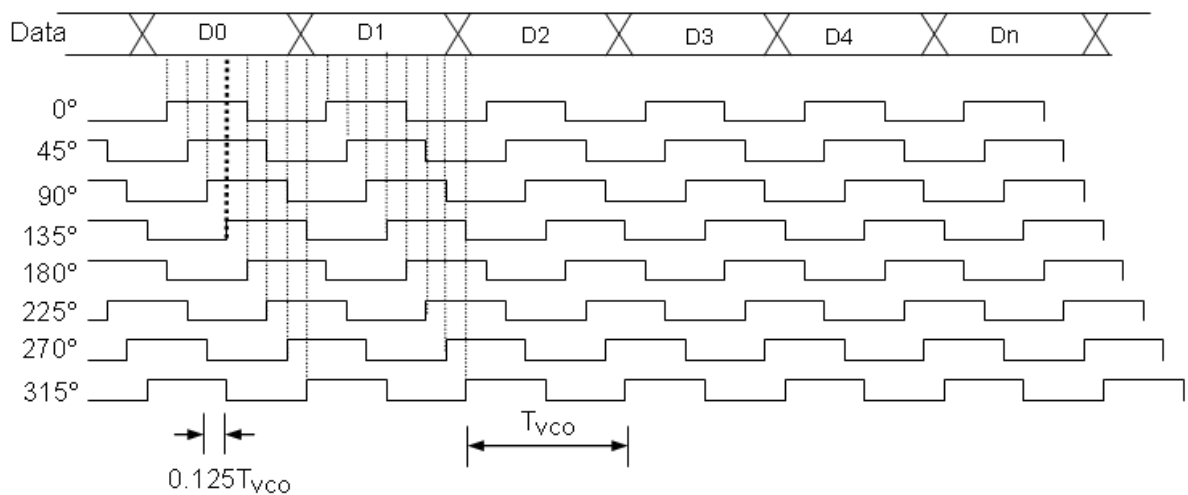
Advantages of the Embedded DPA Circuitry in Stratix GX Devices

Introduction

Stratix™ GX devices have embedded dynamic phase alignment (DPA) circuitry in the receiver circuitry. DPA eliminates clock-to-channel and channel-to-channel skew by aligning the clock to sample at the center of the bit period for each data channel. It uses one of eight phase-shifted clocks from the phase-locked loop (PLL) that is closest to the center of the bit period to sample the data for each channel. See Figure 1. This alignment is continuous and can compensate for dynamic changes in the real-time timing variations between the clock and data signals on a per-channel basis. The DPA solution is optimal for high-speed (greater than 600 Mbps) source synchronous interfaces because it can accommodate more relaxed board layout and connector tolerances and/or give an extra safety margin in board design. The embedded DPA circuitry enables the Stratix GX device family to operate up to 1 Gbps.

For more information on Stratix GX DPA, refer to AN 236: Using Source-Synchronous Signaling with DPA in Stratix GX Devices.

Figure 1: DPA Clock Phase Selection in Stratix GX



Advantages of Altera's Stratix GX DPA

In this white paper, the advantages of Stratix GX embedded DPA over soft DPA solutions (DPA implemented using programmable logic and clock resources) are presented for each of the features listed in Table 1. Comparisons to the Virtex-II and Virtex-II Pro soft DPA solution are also made in some sections of the document. In addition, the advantages that Stratix GX DPA brings to the SPI-4.2 protocol are also discussed.

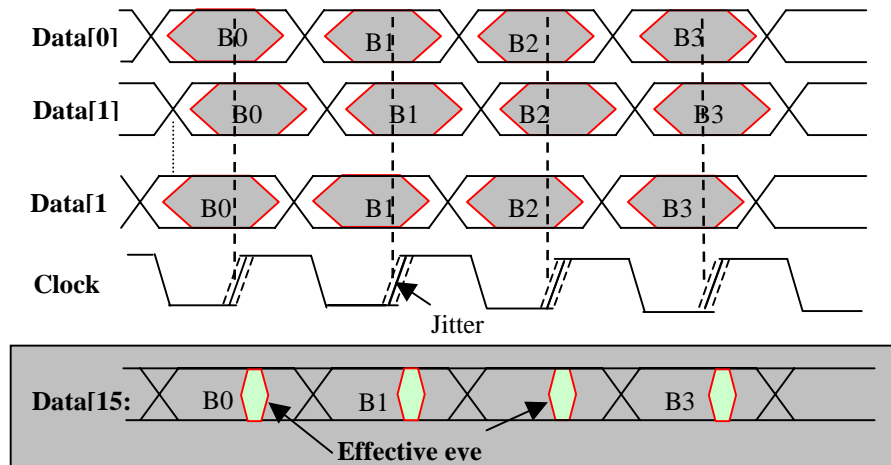
Table 1: Summary of the Stratix GX Embedded DPA Advantages

Features	Stratix GX Embedded DPA
Independent channel operation	Each DPA channel has a digital PLL (DPLL) that selects the right phase of the clock. Clock phase selection happens independently for each channel.
Board flexibility	Up to +/- one clock period.
Ease of design	Built-in DPA circuitry makes implementing DPA in Stratix GX devices very easy.
Resource utilization	Zero logic and clock resources required to implement DPA functionality. Approximately 300 logic elements (LEs) needed to implement control logic for word alignment.
Continuous monitoring of clock to data phase	DPA circuitry continuously center aligns clock to data.
Immunity to process, voltage, and temperature (PVT) variations	Dedicated DPA circuitry and continuous data monitoring feature makes the Stratix GX DPA solution immune to PVT variations.
Immunity to DCD	Immune to DCD because data is sampled at the rising edge of the clock.
Jitter transfer characteristics of PLLs	Stratix GX PLLs filter out high frequency jitter in the input clock.
Performance	Up to 1Gbps.
Built-in bit slipper	Dedicated bit slipper module for word alignment.

Independent Channel Operation

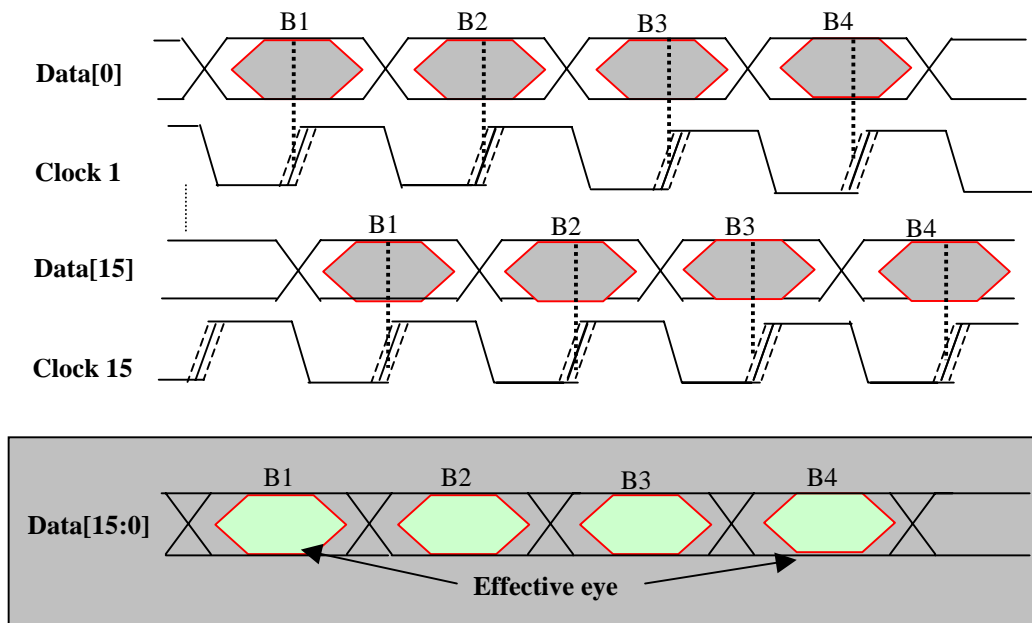
In devices without DPA only one clock phase is used to sample all data channels. In such systems data-to-data skew and clock-to-channel skew consume part of the timing budget. Figure 2 shows an example that illustrates data skew of a 16-bit parallel interface. The first channel is properly aligned with the clock, so sampling occurs at the center of the eye, whereas the second data channel and the 16th data channel are skewed. Variations in trace lengths between channels, operating conditions and jitter creates clock-to-channel and channel-to-channel skew, which could result in sampling errors.

Figure 2: Source Synchronous Implementation – Single Clock for all 16 Data Channels



Stratix GX DPA eliminates the effects of channel-to-channel skew and clock-to-channel skew by using one clock per data channel. Each DPA channel operates independently of each other. The eight clock phases generated by the fast PLLs are inputs to a DPLL associated with every Rx deserializer. The DPLL locks to a phase closest to the serial data's phase. The maximum phase offset between data and the phase-aligned clock is $1/8$ UI. The phase-aligned DPA clock is used to clock the data at the deserializer. Since each channel has its own control circuitry that selects the optimal clock phase, data is always sampled at the center of the bit period. See Figure 3. This significantly reduces the likelihood for bit errors, making the Stratix GX DPA solution robust.

Figure 3: Stratix GX DPA Independent Channel Operation



Board Design Flexibility

Stratix GX DPA compensates for mismatched trace lengths for data and clock channels. This compensation provides a great level of flexibility with board design. This flexibility is possible because clock phase selection is done on a per-channel basis eliminating the effects of channel-to-channel and clock-to-channel skew.

Without DPA, trace lengths for clock and data channels have to be tightly matched to ensure minimum possible skew between channels. This skew places very tight restrictions on the board design. Additionally, having connectors in the signal path makes it close to impossible to meet timing. Connectors induce jitter in the clock and data channels and add skew between data channels. Managing clock-to-channel and channel-to-channel skew to meet timing becomes extremely challenging.

Ease of Design

The Quartus[®] II software provides a simple drop-in solution to implement DPA in Stratix GX. The ALTLVDS megafunction in the Quartus II software provides an option to enable or disable DPA in the design. This allows easy implementation and shortens design cycles.

Designing soft DPA (DPA using LEs and other programmable resources) requires considerable time and effort to meet all necessary timing requirements. The emulation of the DPA circuit is a difficult task; proper implementation can require hand routing within the FPGA core logic. In addition, extensive manual I/O and logic placement constraints need to be assigned to meet design timing requirements.

Furthermore, soft DPA implementations are very sensitive to process, voltage, and temperature (PVT) variations. As a result, the designer must ensure that these delays are matched for all PVT variations. For more details see *Immunity to PVT Variations* on page 7.

Resource Utilization

Stratix GX devices have dedicated DPA circuitry in the silicon. Therefore, implementing Stratix GX DPA does not consume any logic, routing, or clock resources. After the data channels are deserialized, word alignment has to be performed for most source-synchronous interface protocols. Word alignment can be performed using the built-in bit-slip blocks and programmable logic to control the bit slipper. In Stratix GX, approximately 300 LEs are required to implement the control logic for word alignment feature.

For soft DPA implementations, logic elements, clock resources, and general purpose routing are used to generate control logic that selects the clock phase so that data is sampled at the center of the bit period. The Xilinx SPI-4.2 datasheet indicates that 750 slices (1500 LEs) are required to implement the dynamic alignment feature in Virtex-II. Additional logic resources are required for continuous monitoring and word alignment.

If built-in deserialization circuitry is not available, additional logic and clock resources will be required to implement this function in general purpose logic. Xilinx Virtex-II and Virtex-II Pro devices do not have built-in SERDES or DPA circuitry in silicon. General-purpose logic, clock (digital clock managers (DCMs) and global clocks) and routing resources will be required to implement these features. Approximately 588 slices, 2 DCMs, and 5 global clocks are required to implement 16-channel SERDES in Virtex-II and Virtex-II Pro devices.

Continuous Monitoring of Data

Stratix GX embedded DPA circuitry continuously monitors data channels and selects the optimal clock phase so data is sampled at the center of the bit period. Since the phase between data and the reference clock is continuously adjusted so that the clock is always center-aligned to the data, changes in skew due to PVT variations will not cause bit errors.

Immunity to Duty Cycle Distortion (DCD)

In most source-synchronous interfaces, the clock frequency is half the data rate. Data has to be sampled both at the positive edge and the negative edge of the clock. Distortions in clock duty cycle will cut into the available timing budget. See figure 4.

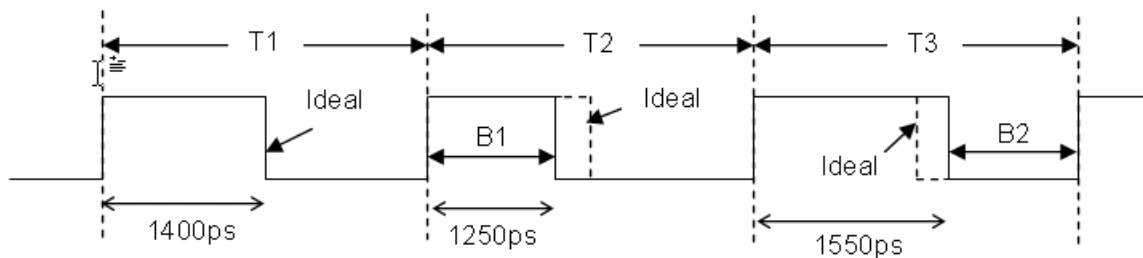
Stratix GX PLLs multiply the received clock frequency so that the frequency of the sampling clock is the same as the data rate. Stratix GX embedded DPA uses single data rate (SDR) clocking to sample the

incoming data signals. Stratix GX DPA is immune to duty cycle distortion because data is always sampled at the rising edge of the clock. Shifts in the falling edge of the clock will not impact timing in any way.

Virtex-II/Pro DPA implementations are not immune to DCD since data is sampled at the rising edge and the falling edge of the clock. DCD cuts into the available timing margin. The designer has to make sure that the design has sufficient timing margin to account for DCD. The Virtex-II datasheet states that the DCM duty cycle can deviate up to ± 150 ps from the ideal value.

Figure 4 is an example of a clock used for 700 Mbps data transfer in Virtex-II/Pro devices. Because double-data rate (DDR) clocking is used, the clock frequency is 350 MHz. The data bit period is approximately 1400 ps (1/700 Mbps) and the clock period is 2800 ps. In time period T1, the falling edge of the clock occurs exactly 1400 ps after the rising edge of the clock. However, in time period T2 the falling edge occurs 1250 ps (1400 ps – 150 ps) after the rising edge of the clock. Therefore, the bit period B1 is only 1250 ps. Similarly, in time period T3 the falling edge occurs 1550 ps (1400 ps + 150 ps) after the rising edge of the clock. The bit period B2 is limited to 1250 ps. Therefore, positive or negative shift in the falling edge of the clock will impact the timing margin. A DCD of 150 ps must be taken into account for timing calculations. In addition to the ± 150 ps duty cycle distortion caused by the DCM (Digital Clock Manager), switching noise in the programmable logic will further impact the duty cycle of clock.

Figure 4: Shift in Falling Clock Edge due to Duty-Cycle Distortion



Superior Jitter Transfer Characteristics of Stratix GX PLLs

Jitter in high-speed source-synchronous systems reduces the “effective eye” of the data signal, causing a higher likelihood for errors. Jitter in the received clock is caused by several sources, including thermal noise, power supply noise, EMI, crosstalk, etc.

Stratix GX PLLs filter out high-frequency jitter in the input clock. The analog circuitry of the Stratix GX PLL translates to a time-continuous transfer function. This transfer function acts as a filter on the PLL input clock, attenuating high-frequency jitter.

PLLs have superior jitter transfer characteristics compared to Xilinx DCMs and delay-locked loop (DLLs). The discrete delay line architecture of DLLs is not capable of filtering the jitter on the input clock. The input jitter accumulates at the output. Therefore, output jitter is a combination of input jitter and the intrinsic jitter of the DLL. If the input clock has high frequency jitter, it is passed on to the output, reducing the “effective eye” of the data signal.

To prove this, experiments were performed to test the jitter transfer characteristics of the Stratix PLL (PLLs in Stratix GX and Stratix are identical) and Virtex-II DCM (DLL in Virtex-II/Pro devices). To test the amount of sinusoidal jitter transferred by the PLL and the DCM, a clock input with a known amount of

sinusoidal jitter was fed to the PLL and the DCM. The sinusoidal jitter at the output of the PLL and the DCM was measured and the jitter transferred was calculated using the formula below.

$$\text{Jitter Transfer (dB)} = 20 \text{Log} \left(\frac{P - P \text{ Sinusoidal Output Jitter}}{P - P \text{ Sinusoidal Input Jitter}} \right)$$

To create sinusoidal jitter, a sinusoidal signal generated by an Agilent E4433B signal generator was modulated onto a 100-MHz carrier. This sine wave was used as an external trigger for the HP8133A pulse generator, creating a square wave with sinusoidal jitter. Square wave with 50% duty-cycle was used as an input clock to Stratix PLL and Virtex-II DCM.

Table 2: Experiment Setup for Jitter Measurements

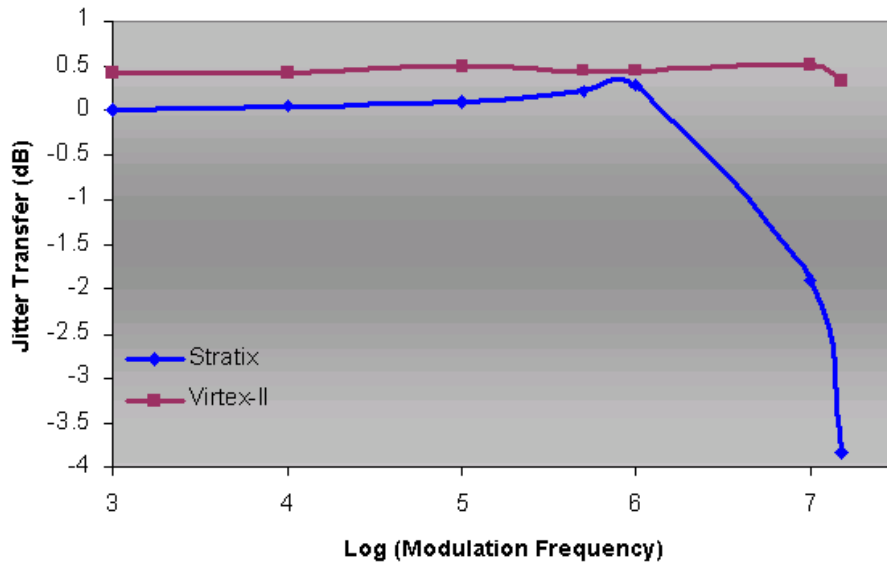
Feature	Stratix	Virtex-II
Device	EP1S10F7806CES	XC2V1000-5FF896C (1), (2)
Logic elements (LEs)	10,570	10,240
Core voltage (V_{CCINT})	1.5 V	1.5 V
I/O voltage (V_{CCIO})	3.3 V	3.3 V
Temperature	Room (25°C)	Room (25°C)

Notes to Table 2:

- (1) Flip Chip package
- (2) Jitter is not a function of speed grade

Sinusoidal jitter transfer test results are shown in Figure 5. Experiment results prove that Stratix PLL filters out up to -4dB of high frequency sinusoidal jitter. In contrast, Virtex-II DCM adds an additional ½ dB of sinusoidal jitter across the entire frequency range.

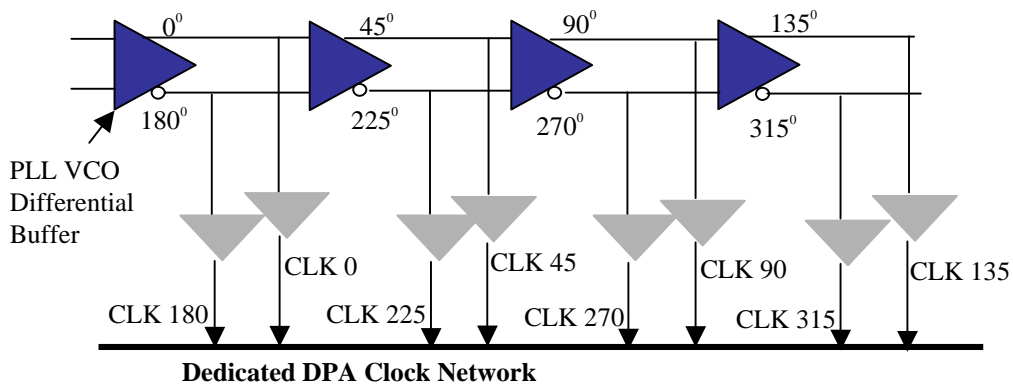
Figure 5: Jitter Transfer Characteristics of Stratix PLL and Virtex-II DCM



Immunity to Process, Voltage and Temperature (PVT) Variations

In Stratix GX, the fast PLL supplies eight phases of the same clock. Each is a separate tap from a four-stage differential voltage-controlled oscillator (VCO) to all the differential channels associated with the selected fast PLL. See Figure 6. The eight clock phases are buffered and routed to a dedicated DPA clock network.

Figure 6: Stratix GX DPA Clock Network



The Stratix GX embedded DPA solution is resistant to PVT variations because of the well-optimized built-in DPA circuitry, dedicated DPA clock network and routing resources. Changes in operating conditions do

not affect the performance or reliability of the circuitry. In addition, continuous monitoring of data ensures that changes in skew due to PVT variations are accounted for. The DPA circuitry, if needed, selects a different clock phase so data is always sampled at the center of the bit period.

Since soft DPA uses logic, general-purpose routing, and clock resources, it is very susceptible to PVT variations. Delay and skew changes that occur due to PVT variations affect the performance and reliability of the system. These delay changes have to be anticipated in the design phase and sufficient timing margin allocated for PVT variations.

Higher Performance

Stratix GX devices support source synchronous transfer at data rates up to 1 Gbps with the use of DPA. This high performance is possible due to the following features:

- Built-in DPA circuitry with matched traces and dedicated clock DPA network
- Independent channel operation, which eliminates timing issues caused by data-to-data and data-to-clock skew
- Continuous monitoring of data, which eliminates skew caused by PVT variations
- Superior jitter transfer characteristics of Stratix GX PLLs

For the Xilinx soft DPA implementation, performance is limited to 700 Mbps. Lack of dedicated DPA circuitry, use of general purpose routing and a global clock network, high susceptibility to PVT variations, lack of immunity to duty cycle distortion, and poor jitter filtering capabilities of the DCM limit the performance of this implementation.

Built-in Bit Slipper

While DPA operation aligns the incoming clock phase to the incoming data phase, it does not guarantee the parallelization boundary or byte boundary. Word alignment circuitry performs data alignment on the parallel data after the deserialization block. This allows the data to be aligned correctly even if the traces vary in length. Stratix GX devices have built-in bit slipper circuitry used for word alignment.

DPA in SPI-4.2

Primarily used in OC-192 systems, the SPI-4.2 standard interfaces cell and packet transfers at 10-Gbps between physical (PHY) and link layer devices. DPA is incorporated in the SPI-4.2 protocol specifications.

The following are the advantages of DPA in Altera's Stratix GX SPI-4.2 solution over DPA in Xilinx SPI-4.2 solution.

Maximum Performance – 1 Gbps

SPI-4.2 performance in Stratix devices is limited to 840 Mbps, and 1 Gbps in Stratix GX devices. In Virtex-II & Virtex-II Pro, SPI-4.2 performance is limited to 800 Mbps without soft DPA and 700 Mbps (+/- 5%) with soft DPA. This performance advantage in Stratix GX can be directly attributed to the dedicated DPA circuitry and advanced PLL technology in Stratix GX devices.

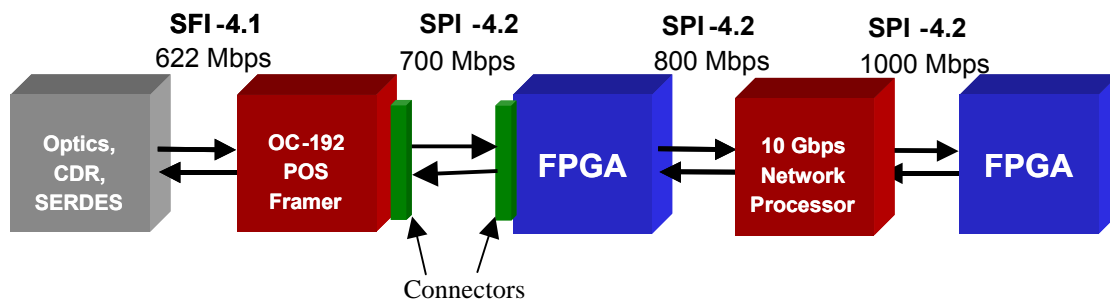
To reduce the effects of latency and ensure that SONET/SDH pipes are fully occupied with real data, as opposed to idle packets, the interfaces between processing devices are typically run at higher rates. 700 Mbps is commonly used to interconnect to Physical layer devices, such as OC-192 POS framers, or 10 Gigabit Ethernet MACs. Higher rates are often used on the system side of a link layer device. 10 Gbps

network processors, such as an Intel IXP2800 device specify rates up to 1 Gbps. See Figure 7. Stratix GX devices can be used to deliver the needed performance for such applications.

Device Utilization

Stratix GX devices do not require any general-purpose logic or clock resources to implement DPA. Soft DPA in Virtex-II and Virtex-II Pro consumes 750 slices (1500 LEs).

Figure 7: Typical Performance Requirements



Summary

DPA in Stratix GX FPGAs offers several advantages over programmable logic-based DPA offerings, including better immunity to temperature and voltage variation, conservation of clock-management resources, higher operational frequencies, and zero consumption of valuable logic resources in the device.

References

Altera® [Stratix GX FPGA Family Datasheet](#)

Altera Application Note 236: [Using Source-Synchronous Signaling with DPA in Stratix GX Devices](#)

Altera White Paper: [The Need for Dynamic Phase Alignment in High-Speed FPGAs](#)

Xilinx Application Note 225: Data to Clock Phase Alignment

Xilinx Application Note 268: Active Phase Alignment

Xilinx Application note 265: High-Speed Data Serialization and Deserialization (840Mb/s)

Xilinx SPI-4.2 (PL4) Core v5.2 Product Specification

Xilinx Virtex-II Datasheet

Xilinx Virtex-II PRO Datasheet



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