

Stratix II GX Product Backgrounder

Introduction

The Stratix[®] II GX FPGA family is Altera's third generation of FPGAs to combine high-speed serial transceivers with a high-performance FPGA fabric. Stratix II GX devices include four to 20 low-power transceivers, each incorporating clock data recovery (CDR) optimized for excellent signal integrity across their entire data range of 622 Mbps to 6.375 Gbps. The transceivers are grouped into four-channel transceiver blocks, and designed for low power consumption and small die size. Altera designed the Stratix II GX family to provide a robust solution for the growing number of applications and protocols requiring high-speed serial data transmission. The family's high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Stratix II GX FPGAs are the cornerstone of Altera's comprehensive solutions for high-speed serial applications. A complete set of intellectual property (IP) cores, system models, reference designs, signal integrity tools and collateral is available for designers to help reduce the cost, time, and risk of developing high-speed systems. Altera's comprehensive solutions make it easier for designers to take advantage of the protocols supported in Stratix II GX devices, including PCI Express, serial digital interface (SDI), XAUI, SONET, Gigabit Ethernet, Serial RapidIO™, SerialLite II, and Common Electrical Interface 6 Gbps Long Reach and Short Reach (CEI-6G-LR/SR).

Transceivers have become commonplace across all markets, including wireless, networking, broadcast, test and measurement, and storage. This trend, fuelled by the need to move more data, is supplemented by the emergence of many new transmission protocols. Altera chose the operating range of the Stratix II GX family's transceivers based on customer requirements for these new applications and the industry's protocol roadmaps.

Best-in-Class Signal Integrity

Altera designed the Stratix II GX transceivers to provide best-in-class signal integrity performance. Low jitter generation and excellent jitter tolerance, hallmarks of the first-

generation Stratix GX transceivers, are also key attributes of Stratix II GX devices. Stratix II GX transceivers have easily adjustable dynamic pre-emphasis, equalization, and output voltage control. These features, combined with special packaging, noise filtering, excellent receiver sensitivity, and robust CDR design, ensure the best signal integrity.

Lowest Power

During the architectural design of Stratix II GX FPGAs, Altera carefully analyzed the “sweet spot” of applications and protocols and optimized the data path and clocking scheme to reduce power consumption over a broad spectrum of protocols, while retaining best-in-class jitter performance. As a result, Stratix II GX transceivers dissipate less than half the power of the nearest competing FPGA transceiver. To illustrate, a 20-port, 6.375-Gbps implementation in Stratix II GX FPGAs dissipates 4.5 watts, versus the competitor’s solution that dissipates 11 watts at the same data rate.

Complete Protocol Support

As part of the Stratix II GX family offering, Altera provides complete protocol solutions that simplify the design process and reduce time-to-market. The physical coding sublayer (PCS) blocks built into the Stratix II GX transceivers make designing for these protocols straightforward because they save valuable logic resources and simplify design. Each transceiver block includes dedicated circuitry to support PCI Express, CEI-6G-LR/SR, SDI, Gigabit Ethernet, Serial RapidIO, XAUI, and SONET. Altera also provides soft IP for protocols including PCI-Express, SDI, Serial RapidIO, and SerialLite II. Stratix II GX devices contain built-in word detection and alignment circuitry and built-in 8b/10b encoder/decoders, (which are by-passable when not required) making these devices suitable for both proprietary and protocol-based applications. Altera also provides protocol-specific design software, development boards, reference designs, and technical collateral (including board layout guidelines, characterization reports, and user guides).

FPGA Architecture

Stratix II GX devices are built on TSMC’s 1.2-V, 90-nm SRAM process and utilize the same innovative logic structure as Stratix II FPGAs. The logic structure is optimized to maximize performance and control static power while allowing designers to conserve device resources by packing more functionality into less area. Stratix II GX FPGAs provide up to 132,540 equivalent logic elements (LEs) and 6.7 Mbits of on-chip

TriMatrix™ memory for demanding, memory-intensive applications. Stratix II GX FPGAs include up to 63 digital signal processing (DSP) blocks with up to 252 (18-bit×18-bit) multipliers for efficient implementation of high-performance filters and other DSP functions. Various high-speed external memory interfaces are supported, including DDR SDRAM and DDR2 SDRAM, RLDRAM II, QDR II SRAM and SDR SDRAM. Stratix II GX devices provide support for a number of source-synchronous differential I/O signaling standards, operating up to 1.2 Gbps, when using dynamic phase alignment (DPA) circuitry. Stratix II GX devices offer a complete clock management solution with internal clock frequency of up to 500 MHz and up to eight phase-locked loops (PLLs). In addition, Stratix II GX devices offer design security, on-chip termination and remote system upgrade capabilities.

Software Support

Designers can begin their Stratix II GX device designs today using Quartus® II software version 5.1. In addition, designers can use board design tools from Cadence (Allegro SI) and Mentor Graphics (ICX and HyperLynx) to verify the design's signal integrity or simulate the entire system. Whether a designer is implementing standard or proprietary protocols or using transceivers for backplane, chip-to-chip, or optical module applications, the Stratix II GX family is designed to provide the most complete transceiver solution.

Stratix II GX Family Overview						
Device	Equivalent Logic Elements	Total Memory Bits	Transceiver Channels	18-Bit x 18-Bit Multipliers	PLLs	Package
EP2SGX30C	33,880	1,369,728	4	64	4	780-pin FBGA⁽¹⁾
EP2SGX30D	33,880	1,369,728	8	64	4	780-pin FBGA
EP2SGX60C	60,440	2,544,192	4	144	8	780-pin FBGA
EP2SGX60D	60,440	2,544,192	8	144	8	780-pin FBGA
EP2SGX60E	60,440	2,544,192	12	144	8	1,152-pin FBGA
EP2SGX90E	90,960	4,520,448	12	192	8	1,152-pin FBGA
EP2SGX90F	90,960	4,520,448	16	192	8	1,508-pin FBGA
EP2SGX130G	132,540	6,747,840	20	252	8	1,508-pin FBGA

Notes:

1. FBGA = FineLine BGA[®] package.

For more information about the Stratix II GX family, visit www.altera.com/stratix2gx.

###

Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations and all other words that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holder.