

Stratix II DDR2 System Validation Summary

Introduction

Today's DDR2 interface solutions need more than just FPGA characterization data to prove functionality. They must demonstrate reliable, robust design in challenging environments. To confront this challenge, Altera carried out a series of tests to pinpoint the most critical issues affecting system functionality. Once these issues were identified, the question then addressed was: Just how well does the Altera® solution perform in those conditions? Tests were conducted at 533 Mbps using an "out-of-the-box" Altera DDR2 intellectual property (IP) core currently available free to Quartus® II customers.

Altera engineers explored drive strength, termination scheme, addressing scheme, data pattern effects, process voltage and temperature (PVT) effects, and memory devices to find the areas critical to system success. Each test examined various responses, including eye quality, edge rates, voltage sag, ground bounce, and, of course, the system functionality, on a "pass or fail" basis. Not only do the results show that the Altera DDR2 memory interface solution on the Stratix® II FPGA family is robust and reliable, they convey that it meets or exceeds expected performance in all areas.

Altera ran all tests at 267 MHz (533 Mbps) using an out-of-the-box DDR2 MegaCore® design, with FPGA utilization set at more than 70 percent. The results of these tests, as shown in the eye diagram of the write operation, the V_{CC} sag and ground bounce, and the read margin, are described below.

Eye Diagram of Write Operation

Figure 1 shows the eye diagram taken during a write operation, with OCT25Ω on the left and 16 mA on the right. The measurement was taken at the DIMM (far) end (i.e., with the FPGA driving). The drive strength was at 16 mA and termination set to Class II. The measurements clearly show that the limit is well above the DDR2 specifications of $900\text{ mV} \pm 125\text{ mV}$ (775 mV to 1.025 V).

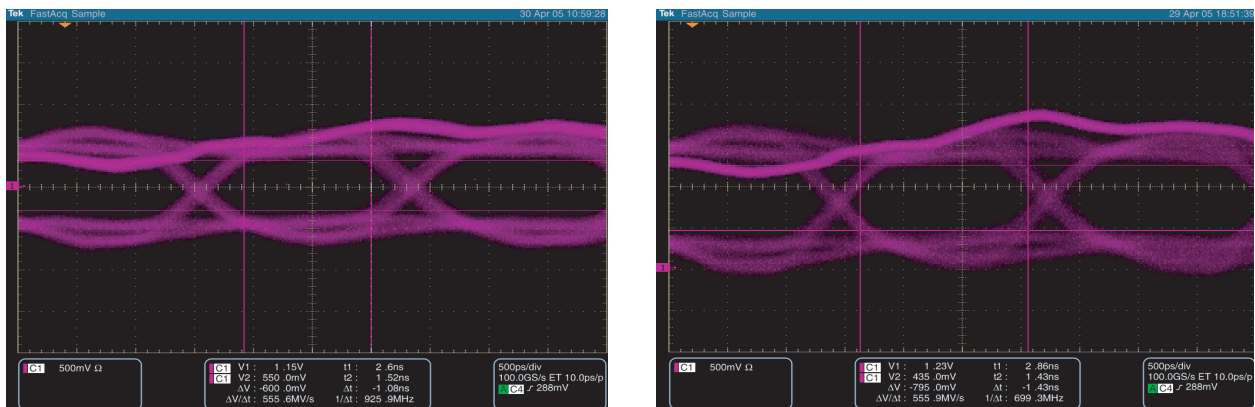


Figure 1. Eye Diagrams Seen During Write to DIMM

Table 1. Eye Diagram Results During Writing to DIMM

Measurement	Drive Strength	Vout (V)	DIMM Spec (V)
V_{oh} Minimum	OCT25Ω	1.15	1.025
	16 mA	1.23	
V_{ol} Maximum	OCT25Ω	0.55	0.775
	16 mA	0.43	

VCC Sag and Ground Bounce

Figure 2 shows V_{CC} sag (right) and ground bounce (left) screenshots for 16-mA drive strength. The 533-Mbps switching signal (light green) is one of the 71 aggressor pins and the static '1' or static '0' signal (orange) is the victim pin.

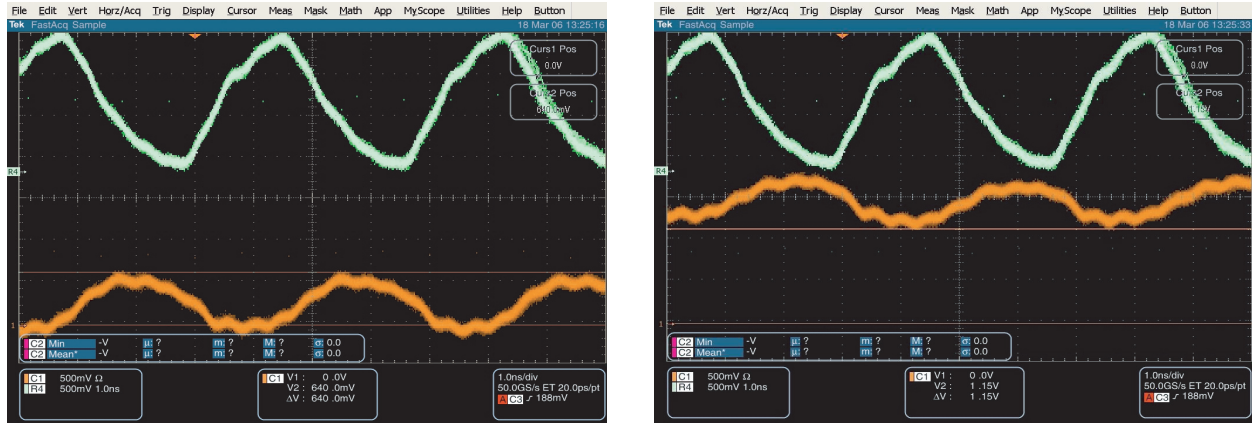


Figure 2. Ground Bounce and V_{CC} Sag Measurements for 16-mA Drive Strength

Table 2. V_{CC} Sag and Ground Bounce While Writing to DIMM

Measurement	Drive Strength	Vout (V)	DIMM Spec (V)
V _{CC} Sag	OCT25Ω	1.12	1.025
	16 mA	1.15	
Ground Bounce	OCT25Ω	0.69	0.775
	16 mA	0.64	

Read Margin

Operating at 267 MHz with DQS phase shift fixed at 90°, the valid read window for various PVT settings was investigated, with results shown in Table 3. As expected, the valid read window shifts for different process, voltage, and temperature settings. Note how the automatically calculated settings of the MegaWizard® resynchronization phase (shown in blue at 315°) are always within the valid range, showing a good read margin.

Table 3. PLL Phase Shift Window Based on 90° DLL Phase Shift With Different PVT Settings

Run	120	135	150	165	180	195	210	240	255	270	285	300	315	330	345	0	15	30
1 (TT, 1.7 V, 0° C)	Red	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
2 (TT, 1.7 V, 50° C)	Red	Red	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
3 (TT, 1.9 V, 0° C)	Red	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
4 (TT, 1.9 V, 50° C)	Red	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
5 (FF, 1.7 V, 0° C)	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
6 (FF, 1.7 V, 50° C)	Red	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
7 (FF, 1.9 V, 0° C)	Red	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red
8 (FF, 1.9 V, 50° C)	Red	Red	Red	Green	Green	Green	Green	Green	Green	Green	Green	Green	Blue	Green	Green	Green	Red	Red

Note:

- (1) FF = Fast silicon and 1.9 volts
- (2) TT = Slow silicon and 1.7 volts (i.e., ±5% of 1.8V VCCIO)

These tests indicate the Altera DDR2 interface solution has a 165° valid read window over these PVT settings. At 267 MHz, that is a valid window of greater than 1.7 ns.

Memory Vendor

The system was tested with both Micron and Infineon memory devices. Changing memory vendors made no difference to operational results.

Conclusion

This series of system validation tests shows that the Altera DDR2 interface solution is a reliable and robust design capable of running at 533 Mbps across a range of PVT settings. Changes to drive strengths, termination schemes, and swapping memory vendors make no difference to the system operation. Furthermore, the results show excellent setup and hold margins. The Altera DDR2 interface solution can be confidently added to a Stratix II IP suite today.

Related Materials

- *AN 408: Stratix II FPGA DDR2 Memory Interface Termination, Drive Strength, and Loading Design Guidelines:*
<http://www.altera.com/literature/an/an408.pdf>
- *AN 328: Interfacing DDR2 SDRAM With Stratix II Devices:*
<http://www.altera.com/literature/an/an328.pdf>



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