

Cyclone II Backgrounder

Introduction

Building on the tremendous success of the Cyclone™ family, Altera's new Cyclone II family offers even lower costs, higher densities and more features with exceptional performance. The new device family provides from 4,608 to 68,416 logic elements (LEs) and is designed with an optimal set of features, including up to 150 embedded 18x18 multipliers, dedicated external memory interface circuitry, 4-Kbit embedded memory blocks, phase-locked loops (PLLs), and high-speed differential I/O capabilities.

FPGAs, with their flexibility and time-to-market advantages, are increasingly being used by designers as ASIC alternatives in systems aimed at the consumer, industrial, automotive, wireline and wireless communication, and medical markets. Altera's new Cyclone II device family, which builds on the low-cost FPGA leadership Altera established with the first-generation Cyclone family, delivers a low-risk, and low-cost solution that makes it a highly attractive alternative to low- and mid-density ASICs.

Cost-Optimized Architecture

Cyclone II devices are designed for the lowest cost, while maximizing performance. Altera consulted with its customers to determine the critical trade-offs between cost and desired device features. These customer inputs played a critical role in determining Cyclone II device characteristics.

Cyclone II devices are built on 300-mm wafers using TSMC's 90-nm, low-k dielectric process technology, which, combined with Altera's low-cost design approach, makes it possible to produce larger density devices at very low cost. The new device family offers more than twice the I/O pins available with first-generation Cyclone products, as well as an optimal mix of programmable logic, memory blocks, and other features. As a result, entire systems can be implemented in Cyclone II devices, at a price that rivals ASIC alternatives, but with lower risk and faster time-to-market.

Key Features

Cyclone II FPGAs offer several new and enhanced features to meet the needs of the low-cost, high-volume marketplace.

Density - Cyclone II devices offer up to 68,416 logic elements (LEs), three times that of Cyclone devices.

Embedded Memory – The Cyclone II device’s 4-Kbit M4K embedded memory blocks (4,096 bits plus 512 parity bits per block) offer up to 1.1 Mbits of embedded memory. This provides the densities needed to address standard system on-chip memory requirements for system cache, data buffering, clock domain translation, and first-in first-out (FIFO) applications. In addition, the Cyclone II device’s embedded memory blocks support multiple configurations, including true dual-port and single-port RAM, ROM, and FIFO buffers.

Embedded Multipliers – Cyclone II devices feature up to 150 embedded 18x18 multipliers ideal for implementing common, low-cost digital signal processing (DSP) functions such as FIR filters, FFTs, correlators, encoders/decoders, and NCO. Capable of running at 250 MHz, the embedded multipliers in Cyclone II devices make them ideal for use as co-processors that offload complex and time-consuming arithmetic computations from digital signal processors to boost overall system performance while lowering system costs.

External Memory Interface – The Cyclone II family has been optimized for high-speed, reliable data transfer to and from external memory devices. All members of the family can communicate with double data rate (DDR and DDR2), single data rate (SDR) SDRAM devices and quad data rate (QDRII) SRAM devices through a dedicated interface that ensures fast, reliable data transfer at up to 668 Mbps.

I/O Standards – Cyclone II devices support an increased number of I/O standards, including single-ended standards required to support DDR and DDR2 SDRAM and QDR II SRAM advanced memories. Newly supported standards include HSTL, PCI-X, LVPECL and mini-LVDS I/O standards, as well as the LVTTL, LVCMOS, PCI, SSTL, LVDS, and RSDS standards supported by first-generation Cyclone devices.

For more details about Cyclone II devices, please visit Altera’s web site at www.altera.com.

Table 1. Cyclone II Family Overview						
Feature	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Logic Elements	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM Blocks	26	36	52	105	129	250
Total RAM Bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded 18x18 Multipliers	13	18	26	35	86	150
Phase-Locked Loops	2	2	4	4	4	4
Maximum User I/O Pins	142	182	315	475	450	622
Available Packages	144-pin TQFP ¹ 208-pin PQFP ² 256-pin FBGA ³	144-pin TQFP 208-pin PQFP 256-pin FBGA	256-pin FBGA 484-pin FBGA	484-pin FBGA 672-pin FBGA	484-pin FBGA 672-pin FBGA	672-pin FBGA 896-pin FBGA

Notes:

¹ TQFP = thin quad flat pack

² PQFP = plastic quad flat pack

³ FBGA = FineLine BGA[®]

Nios II Embedded Soft Processor

The Cyclone II FPGA family is fully supported by Altera's recently introduced Nios[®] II family of soft processors. Consuming as little as \$0.35 of logic, the Nios II family of soft-core processors can be designed into a Cyclone II device at a cost that is 50 percent less than the nearest competing embedded processor. In addition to this significant reduction in implementation cost, a Nios II design in a Cyclone II FPGA offers more than 100 DMIPs performance, an approximate 100 percent improvement compared to the Cyclone device and Nios processor. With a Nios II processor, a designer can build a complete system on a programmable chip (SOPC) on any Cyclone II device, providing new alternatives to low- and mid-density ASICs.

Low-Cost Configuration Devices

Altera offers a family of low-cost serial configuration devices to configure Cyclone II FPGAs. These serial configuration devices are priced for volume applications and cost as little as 10 percent of the cost of the corresponding Cyclone II FPGA. Four serial configuration devices (1 Mbit, 4 Mbit, 16 Mbit, and 64 Mbit) are offered in space-saving 8-pin and 16-pin SOIC packages. Any device memory not used for configuration tasks can be used for general-purpose storage, further enhancing their value.

Quartus II Web Edition Design Software

Cyclone II devices were designed in concert with Quartus[®] II design software version 4.1 to provide customers with unmatched performance and ease-of-use. Quartus II software is the industry's most advanced development software for FPGAs and offers a comprehensive suite of synthesis, optimization, and verification tools in a single, unified design environment. Leveraging Quartus II software technology, designers can select, integrate, and evaluate intellectual property (IP) in Cyclone II designs in a matter of minutes. Quartus II software also integrates seamlessly with all leading third-party synthesis and simulation tools. The free Quartus II Web Edition software, which fully supports the Cyclone II family, can be downloaded at www.altera.com/q2webedition.

Intellectual Property

Altera also offers its Cyclone II device customers a rich suite of fully customizable intellectual property (IP) cores developed and tested both by Altera and its participating Altera Megafunction Partners Program (AMPPSM) partners. The OpenCore[®] Plus evaluation feature allows users to evaluate Altera MegaCore[®] functions and AMPP megafunctions in hardware and simulation prior to licensing. When the user is completely satisfied with the IP function, the full license can be purchased. The IP MegaStore[™] web site provides an easy way to search Altera's and AMPP partners' comprehensive portfolio of IP functions.