

Simplifying Simultaneous Multimode RRH Design

RRH technology with support for simultaneous operation of multiple air-interface protocols is an emerging end-product requirement. The diverse modulation formats and sampling rates between standards such as MC-GSM, WCDMA, and LTE make designing common building blocks, including DUCs and DDCs, challenging. This white paper explores potential filter-chain architectures to simplify simultaneous multimode digital IF processing design, and highlights the productivity and resource utilization tradeoffs between a modular DUC approach and a duplicated DUC approach for a multimode MC-GSM/WCDMA/LTE design.

Introduction

Multimode basestations capable of supporting multiple standards such as MC-GSM, WCDMA, WiMAX, and LTE offer numerous benefits for both operators and infrastructure OEMs.

The benefits to operators include:

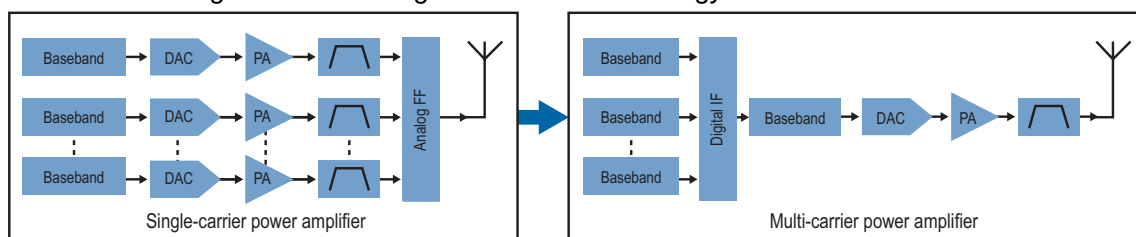
- Flexible use of available spectrum via inlay deployment of new networks such as LTE
- Reduction of capital expenses by reusing existing basestation equipment and making only software or board level upgrades for deploying new networks
- Reduction of operating expenses by reusing cell sites (saves on rental costs), reusing remote radio heads (RRHs) (saves on installation costs), and reusing backhaul
- Ability to future-proof networks and reduction of long-term total cost of ownership

The benefits to infrastructure OEMs include:

- Reduction of R&D expenses via universal basestation approach for multiple standards
- Simplification of product line management
- Ability to quickly adapt to evolving standards and bug fixes via programmable hardware
- Ability to differentiate from competition and charge a premium for future-proof equipment

While separate cost-optimized channel cards can be added to the basestation cabinet to deploy the modem functionality for various standards, upgrading tower-mounted RRHs with corresponding standard-specific cards is not a desirable solution for operators from an operating expense standpoint. Hence, a universal RRH capable of supporting multiple standards via only software upgrades is an emerging market requirement. The emergence of MC-GSM deployment using multicarrier-power amplifier (MC-PA) technology also enables the multimode RRH trend. Recent changes in spectrum regulations make it possible to use MC-PAs and digital intermediate frequency (IF) processing to deploy multiple GSM carriers, as shown in [Figure 1](#).

Figure 1. MC-GSM Digital IF Processing With MC-PA Technology



MC-PAs and digital IF architectures predominantly are used for developing multicarrier 3G basestations, including WCDMA and CDMA2000. With MC-GSM moving to a similar architecture, it is now possible to build multimode RRHs that support MC-GSM, WCDMA, and LTE. Going forward, RRHs may require various levels of multimode support for:

- Factory or remote reconfiguration
- Simultaneous operation
- Run-time reconfiguration
- Run-time reconfigurable simultaneous operation

While support for run-time reconfiguration is a nice-to-have feature for operators, providing significant flexibility in addressing a varying mix of voice and data traffic, support for factory reconfiguration and simultaneous operation are must-have features to enable cost-effective deployment of inlay networks in the short term.

Factory reconfiguration is supported with state-of-the-art FPGAs, which are inherently programmable devices that offer a high-performance platform for implementing multimode RRHs. Altera® 40-nm devices, including Stratix® IV GX and Arria® II GX FPGAs, offer a wide array of highly integrated system-on-chip (SoC) options for implementing multicarrier, multi-antenna RRH systems. For example, with up to 530K LEs, greater than 1200 18x18 multipliers, 20 Mbits of embedded RAM, and transceivers up to 8.5 Gbps, a single Stratix IV GX FPGA can be used to implement all the digital functionality in a RRH that supports a single sector, 20-MHz LTE carrier with 4x4 multiple input/multiple output (MIMO). The same FPGA can be reprogrammed in the factory or remotely in the field to support 12 MC-GSM carriers or four WCDMA carriers.

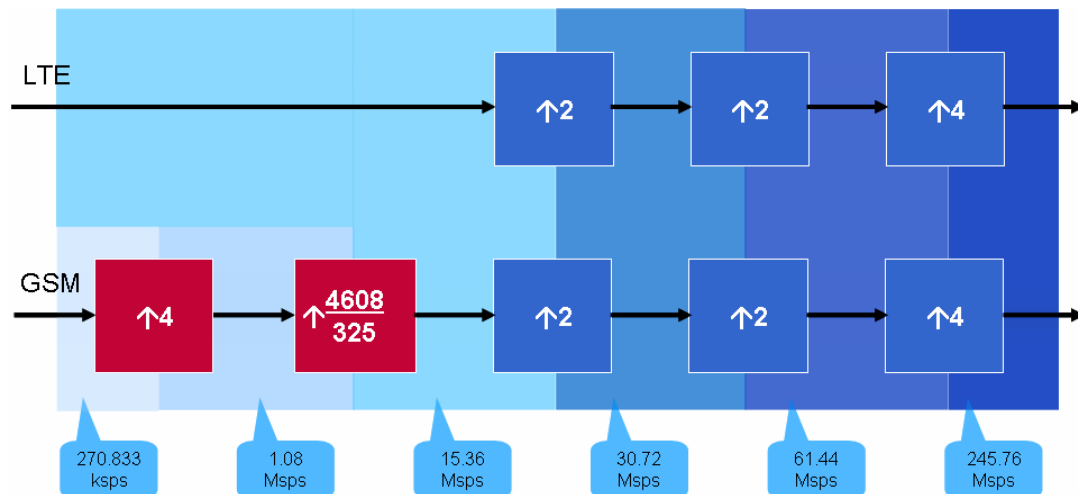
This white paper explores potential solutions for simultaneous multimode support. The digital upconverter (DUC) block requirements and both the modular and duplicated multimode DUC architecture are explored, and relative trade-offs between productivity benefits and FPGA resource requirements are highlighted in each case.

Sampling-Rate Equalization

One of the major challenges of multimode design is that often the sampling-rate requirements are completely different. This makes choosing a clock frequency difficult, and because it is necessary to equalize the sampling frequency before sharing hardware, it also makes hardware sharing difficult. Even if there is no need to share hardware, it is still necessary to equalize the sampling frequencies to combine the multiple air interface signals before using a DAC to convey them across the wireless channel.

LTE and WCDMA systems share similar sampling frequencies, but WiMAX and GSM are completely different. In addition, the ratio of the GSM baseband sampling frequency to the LTE baseband sampling frequency is irrational. [Figure 2](#) summarizes how the additional complexity is associated with the resampling. For GSM, the baseband data must be resampled by a total factor of 4 (4608/325) before it is possible to share LTE hardware. A typical single-mode GSM architecture would usually consist of just three filters: a channel filter, a low-rate interpolation filter, and a cascaded integrator comb (CIC) filter.

Figure 2. Sampling-Rate Equalization



In addition, this problem is exacerbated if a third air interface, not related in sampling frequency to either of the other standards (for example, WiMAX), is necessary. This makes isolating the common frequency harder and complicates the additional logic required for equalization.

Fractional-Rate FIR Filters

A fractional-rate finite impulse response (FIR) filter may be used to increase or decrease the sampling rate of a signal by a non-integer factor. Typically, this operation is an integer upconversion operation followed by an integer downconversion operation, as shown in Figure 3.

Figure 3. Fractional-Rate Resampling



It is possible to implement this as an interpolating filter, followed by a decimation stage. However, if x is very high, the sampling rate before the decimation stage can be greater than the clock rate of the device. When performing decimation after the interpolation, many of the calculations are redundant. As a result, the required calculations are considered when designing architecture to achieve the highest efficiency possible.

For a programmable system, it is possible to design these filters so that the rate change is variable. However, this does mean that there are trade-offs in the design and the size will be determined by the worst-case rate change. This approach is inappropriate for supporting a rate change of 4608/325, as it needs 4608 phases for the filter, and despite time-sharing the phases, still needs a single (probably under-utilized) multiplier per phase. This is clearly not practical, and developing intellectual property (IP) to increase utilization of the multipliers is overly complex considering the enormous parameter space. As a result, the rate change is decomposed into several stages, such as 6/5, 8/5, 12/13, and 8, to get better computational efficiency.

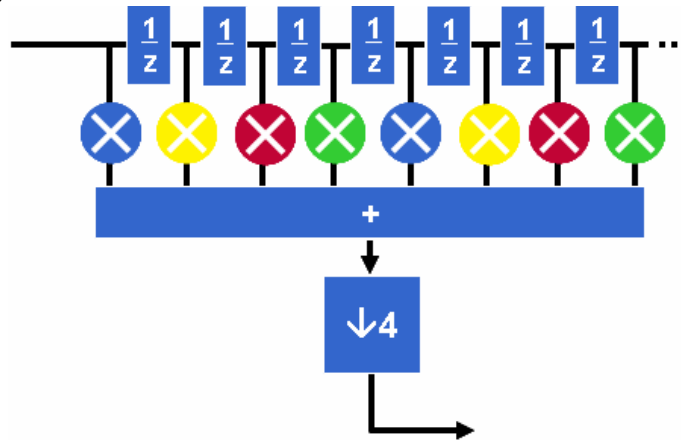
A filter cascade can be included at the input for each air interface, with appropriate configurations of the rate changes. However, this requires a lot of logic, especially considering that some air interfaces do not require such complicated rate changes.

Farrow Filtering Overview

A farrow filter may be used to resample data with an arbitrary rate factor. One of the benefits of this type of filter is that it may be completely runtime configurable if necessary. A polyphase decimation filter only performs a subset of the filtering calculations because certain samples are removed at the output. The fractional delay, or output phase, is determined by the subset of filtering calculations performed.

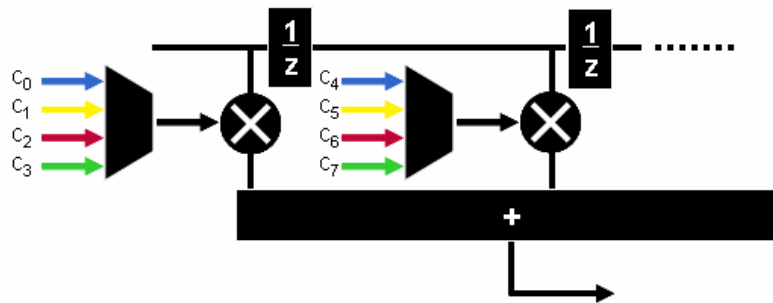
Figure 4 shows a decimation-by-four filter, where only the multiplications associated with the blue multipliers need to be performed because the other samples are discarded during decimation. This example gives a fractional delay of 1/4 after decimation, but it would be equally valid to perform only the multiplications associated with the yellow multipliers, giving a delay of 2/4 samples after decimation.

Figure 4. Decimation-by-Four Filter



The concept of a farrow filter is that since the rate-change factor is irrational, a variable-phase relationship (or variable fractional delay) between the input and output samples is necessary. As a result, more coefficients must be stored than with a fixed-rate change, and selecting the appropriate phase results in a different coefficient set. Figure 5 shows the implemented structure with an over-sampled representation of the required filter and the appropriate polyphase component nearest to the desired phase.

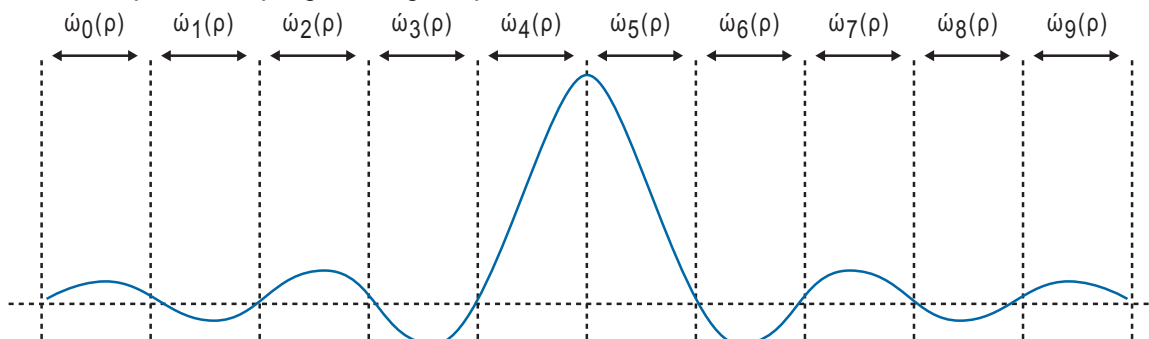
Figure 5. Phase-Switchable Filter



For irrational rate changes, it is impractical to implement such a structure because the memory requirements are too great. Instead, we may take advantage of a technique known as Farrow resampling; we can save memory by evaluating an approximate polynomial to generate the filter coefficients associated with the phase of interest. Figure 6 shows the impulse response divided into L sections, which describe each section of the impulse response (and hence the coefficients) with a polynomial (order M) of the form:

$$\omega_n(\rho) = \alpha_{n,0} + \alpha_{n,1,0}\rho + \alpha_{n,2(0)}\rho^2 + \dots + \alpha_{n,0M}\rho^M$$

Figure 6. Example Resampling Filtering Response

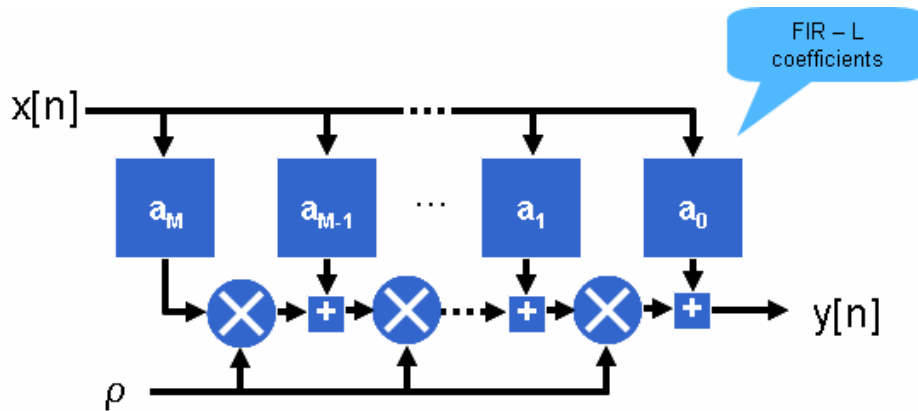


The coefficients $\{\alpha_{n,M}\}$ are determined by fitting a curve in each of the L sections:

$$y[k] = r^T A x = [1 \rho \rho^2 \dots \rho^M] \begin{bmatrix} \alpha_{0,0} & \alpha_{0,1} & \alpha_{0,2} & \dots & \alpha_{0,L-1} \\ \alpha_{1,0} & \alpha_{1,1} & \alpha_{1,2} & \dots & \alpha_{1,L-1} \\ \alpha_{2,0} & \alpha_{2,1} & \alpha_{2,2} & \dots & \alpha_{2,L-1} \\ \dots & \dots & \dots & \dots & \dots \\ \alpha_{M,0} & \alpha_{M,1} & \alpha_{M,2} & \dots & \alpha_{M,L-1} \end{bmatrix} \begin{bmatrix} x[n] \\ x[n-1] \\ x[n-2] \\ \dots \\ x[n-(L+1)] \end{bmatrix}$$

This structure may be realized using the block diagram in Figure 7, which consists of $M+1$, L -tap FIR filters, and M multipliers.

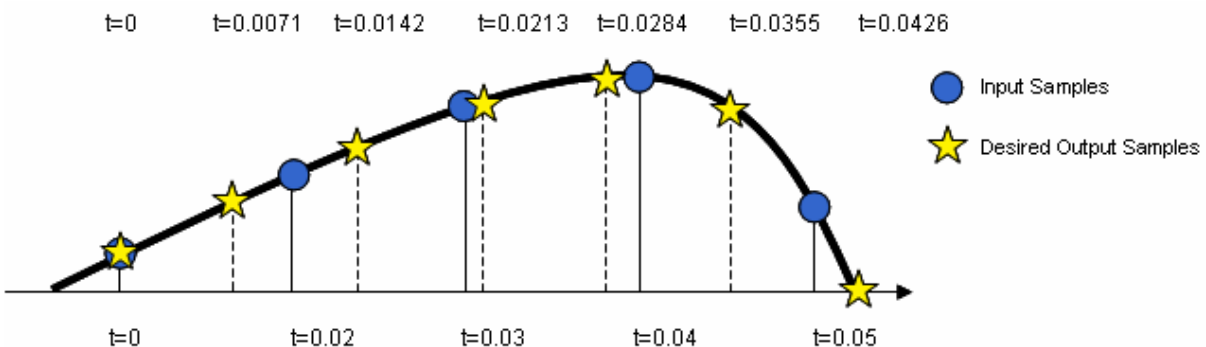
Figure 7. Farrow Filter Structure



ρ is used to quantify the sampling phase difference between the current input and desired output sample. This value is normalized between 0 and 1.

Figure 8 shows an example of an irrational rate change, 1.41 in this case.

Figure 8. Irrational Sampling-Rate Change Example



For each of the desired output samples, the difference in phase between the input samples must be calculated:

$$\rho = \frac{\text{output_time} - \text{input_time}}{\text{input_fs}}$$

Sometimes this calculation generates more than one output sample for an input sample, due to the relationships between the two sampling rates. When calculating $r^T A x$, note that r^T changes, but A (the polynomials) and x (the inputs) stay the same.

Farrow Filter System Design Considerations

A farrow filter is highly beneficial for sampling-rate equalization in a multimode system. Typically, a farrow filter is implemented to perform rate-change factors around 1. As a result, larger rate changes should be split into a fractional change and an integer rate change implemented with a CIC or FIR filter.

We need to consider the following parameters when designing our multimode system

- Rate-change factor (usually expressed as a ratio of output rate to input rate)
- Prototype filter (desired filtering response)
- Polynomial order
- Number of sections

These parameters are used to generate the appropriate polynomials and time-shared filters to realize the overall farrow filter structure. Supporting any variable rate-change factor is possible, but the best performance is achieved when the prototype filter is modified to suit the new system and sampling rate. However, this requires that the polynomials be generated in the hardware. A safe assumption is that the supported air interfaces are relatively static, and it is appropriate to calculate the polynomials externally and simply provide the capability to reload this matrix into the core. This can be calculated using a control microprocessor such as Altera's Nios® II embedded processor.

Hardware and Resource Estimation

Implementing a farrow filter requires:

- $M+1$ FIR filters of L coefficients
- M multipliers and adders to combine the outputs

Each FIR filter uses a single-rate, non-symmetric architecture and processes at a relatively low sampling rate, so together they can time-share the multipliers. State-of-the-art FPGAs, such as Stratix IV GX devices, have embedded 18x18 multipliers capable of running at speeds over 400 MHz, enabling efficient time-sharing of hardware resources.

The number of coefficients L is likely to be quite small because the multipliers in each of the M filters are not fully used due to the large time-share factor. It is possible to combine multiple filters by using a multichannel architecture, but each channel requires a separate coefficient set so there is complexity associated with coefficient switching. It is possible to incorporate the output convolution stage into the same hardware, but this requires more complicated scheduling of the multipliers. The simplest solution is to use $M+1$ highly time-shared filters (resulting in $M+1$ multipliers), followed by a dedicated convolution stage.

Modular DUC/DDC Architectures

Modular DUCs and digital downconverters (DDCs) offer potential benefits to a designer, including:

- Productivity: Using modular DDC/DUC blocks and scaling to meet system requirements is simpler than implementing separate custom designs
- Less maintenance: Debugging is constrained to a single design, and improvements are deployed to all users of the IP

Figure 9 shows a diagram of the different air interfaces supported in a multimode system. We will evaluate the possible merits of developing a reprogrammable datapath that supports multiple bandwidths and sampling frequencies using any combination of the air interfaces shown below. This datapath element can be configured to support a combination of air interfaces in a 10-MHz bandwidth, using a 5-MHz LTE channel and six GSM carriers, or using just a single LTE 10-MHz carrier. It also is possible to connect two configurable datapaths together to support a full LTE 20-MHz carrier.

Figure 9. Possible Frequency Plan and Different Air Interfaces

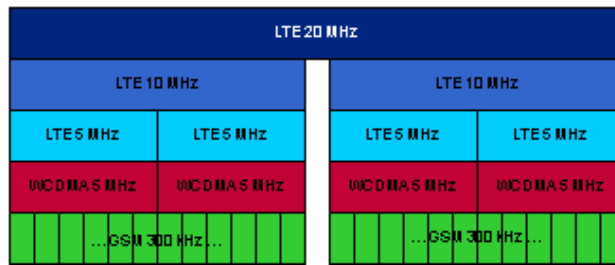
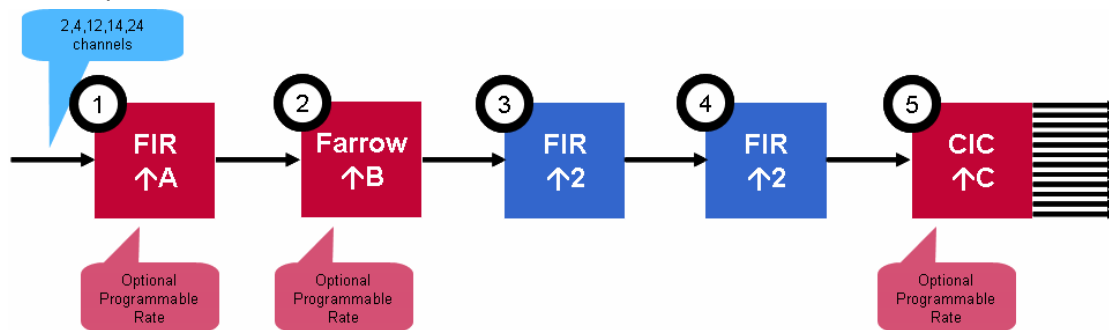


Figure 10 shows the block diagram of a possible architecture for the configurable datapath. This block may be used to handle any 5-MHz spectrum and, as a result, the solution may be scalable by simply duplicating it. To combine any of the configurations above, the architecture must support 1, 2, 6, 7, or 12 carriers, which translates to 2, 4, 12, 14, or 24 hardware channels because of the need to process both the I and Q components.

Figure 10. Proposed Modular Architecture



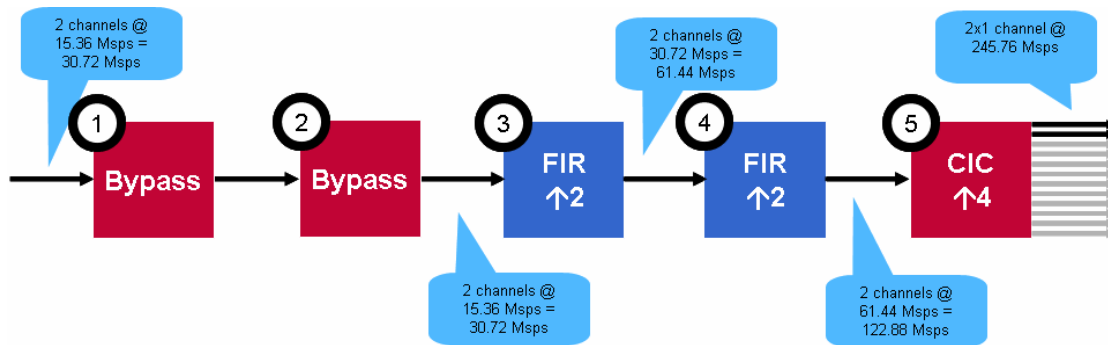
The proposed modular architecture has the following properties:

- Filters shown in red may be enabled or disabled in the chain as required.
- FIR filter coefficients are configurable by the control processor. Blocks in red may be further configured to modify the interpolation rate.
- Systems such as GSM operate with a significantly smaller bandwidth than LTE, so should be able to process enough carriers to fill the same bandwidth.
- The final block must be a CIC filter (5) to support a wide range of sampling-rate and interpolation factors. A FIR filter is impractical because the high sampling frequency requires significant multiplier resources. In addition, this efficiently implements interpolation to a high sampling rate by using a single-input/multiple-output (SIMO) architecture.
- Rounding is required in this datapath, and may need configuring based on the current channel/air interface.
- Numerically controlled oscillators (NCOs) and mixers are not shown in this diagram. Supporting the maximum number of channels requires 12 NCOs and 12 complex mixers running at the full IF sampling rate.

Single LTE Carrier at 10 MHz

Figure 11 shows how the datapath may be configured to support a single 10-MHz carrier. This case has a very simple sampling-rate change, and does not need any sampling-rate equalization because the baseband sampling rate is an integer factor of the clock rate. Although there is only a single carrier, two channels are required in the hardware to accommodate both the I and Q components. As a result, the CIC filter (5) must be parallelized to support the total processing requirements after the decimation.

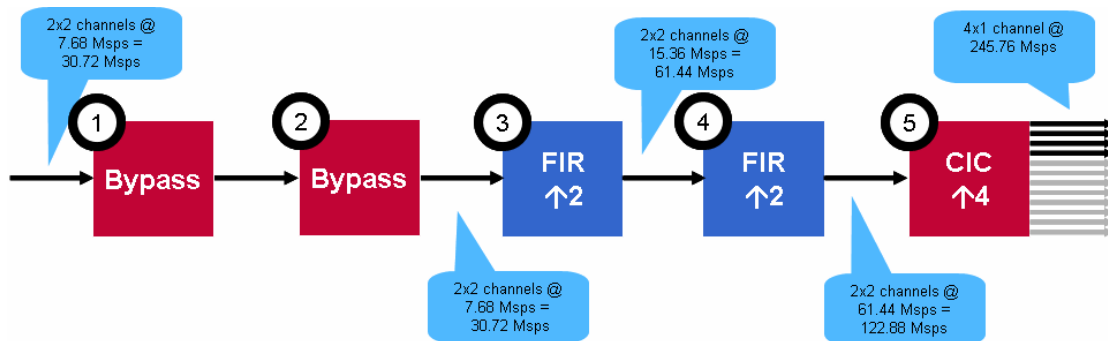
Figure 11. LTE 10-MHz Rate Characteristics



Dual LTE Carriers at 5 MHz

Figure 12 shows another configuration of the modular functional unit that supports two 5-MHz LTE carriers. This design requires the same processing complexity as the previous example, but here the filters are configured to process four hardware channels (I, Q carrier 1 and I, Q carrier 2) rather than just two.

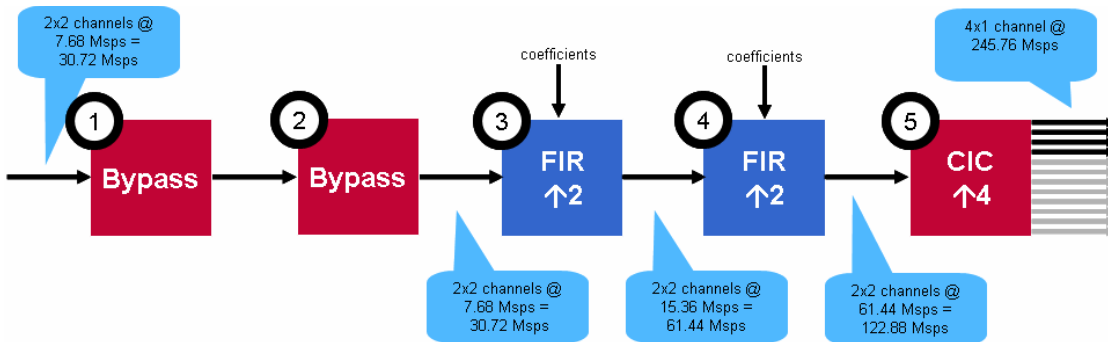
Figure 12. 2X LTE 5-MHz Rate Characteristics



Single LTE Carrier at 5 MHz, Single WCDMA Carrier at 5 MHz

Figure 13 shows a modular functional unit that can process both a single LTE carrier and a single WCDMA carrier. The baseband sampling rates are identical and use the same rate-change characteristics for all channels. However, the spectral mask requirements are different for the two systems, thus they need two separate sets of coefficients. These coefficients change on a sample-by-sample basis, depending on which channel is currently being processed.

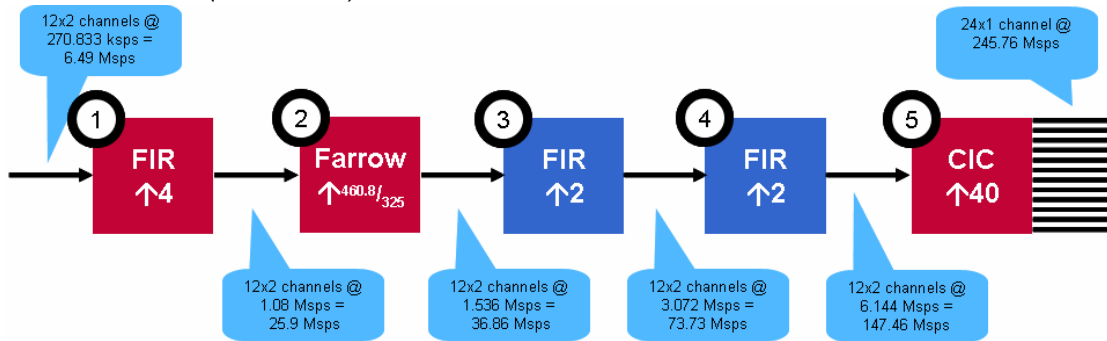
Figure 13. LTE 5-MHz and WCDMA 5-MHz Rate Characteristics



12-Carrier GSM

For GSM, Figure 14 shows the input sampling rate is a non-integer factor of the clock frequency, thus enabling the sampling-rate equalization of the design. The sampling-rate change in the farrow filter (2) should be $4608/325$. In this example, it is configured as $460.8/325$, so this is compensated for in the CIC filter at the end of the chain.

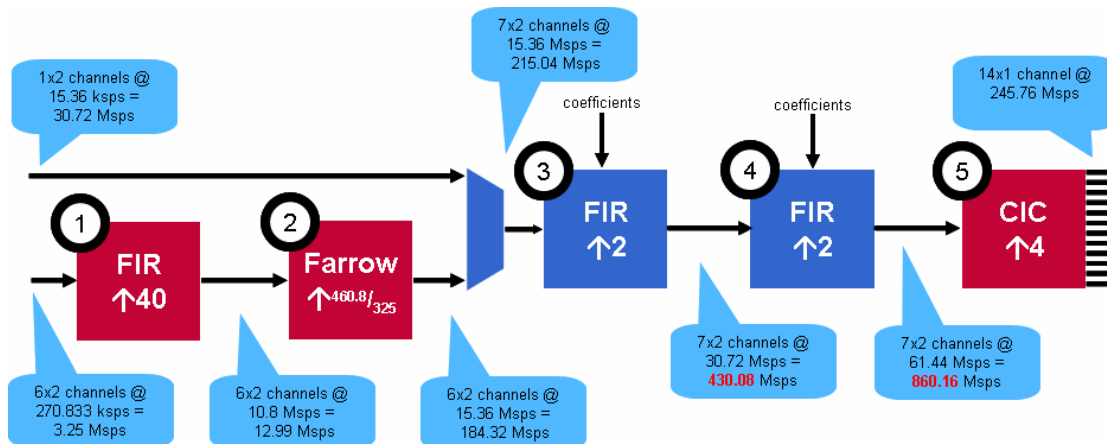
Figure 14. Multicarrier (12 Carriers) GSM Rate Characteristics



6-Carrier GSM and Single-Carrier LTE at 5 MHz

Figure 15 shows an example where two air interfaces with incompatible sampling-rate characteristics are mixed. The GSM requires sampling-rate equalization before it is possible to share any filtering with the LTE system. As a result, it is necessary to have an additional input to the modular functional unit to accept data that does not need to be sampling-rate equalized. After the sampling-rate equalization, the two streams of data must be combined to load the stream into the subsequent filtering chain. Since there are two different air interfaces processed, the coefficient sets in the filters must be switched to ensure the appropriate filtering characteristics are achieved.

Figure 15. Dual-Mode GSM and LTE Architecture and Rate Characteristics



In this particular configuration, the bus-sampling rate after the second FIR filter (3) is greater than the clock frequency. The parallel instances of these filters are required to perform the desired functionality, so there is no benefit in implementing a modular functional unit for practical multimode systems.

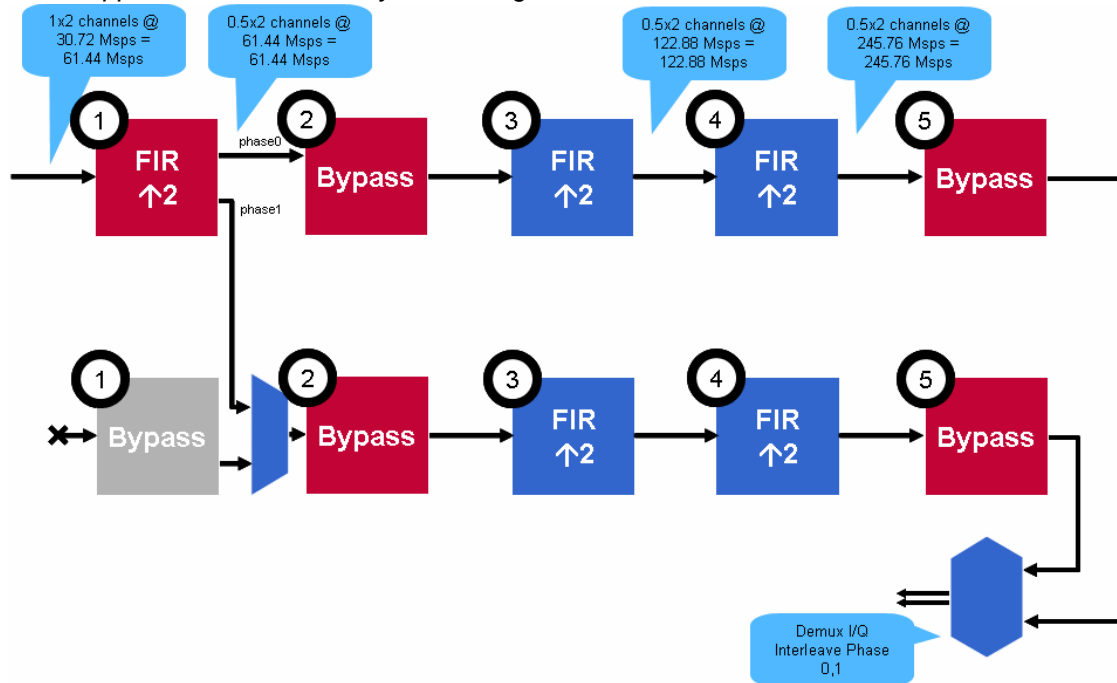
For GSM, it is best to perform the large rate change of factor 40 at the output of the DUC. However, it is essential for this to happen during the equalization stage so the two systems can share the hardware. The rate-change increase at the beginning of the chain is impractical and requires significant numbers of taps to realize an acceptable attenuation. To avoid parallel instances of the filters, the maximum bus-sampling rate between the third FIR filter (4) and the CIC filter (5) should be less than f_{CLK} . This rate supports a maximum of one LTE carrier and three GSM carriers, and

improves when the IF-sampling frequency is dropped to 122.88 Msps. The configurable data path does not have any merit for this particular application.

Single-Carrier LTE at 20 MHz

Figure 16 shows how to design the functional units so they can be cascaded together to support systems with a higher sampling rate, such as a 20-MHz LTE carrier. Although it is possible to design filters that support 20-MHz LTE signals, the design of a flexible filter chain is subject to many trade offs between flexibility and area. Time-sharing considerations may make it impossible to process a 20-MHz LTE signal.

Figure 16. Support for 20-MHz LTE by Combining Two Scalable Units



The first FIR filter (1) in the chain has a mandatory rate change using a polyphase decomposition technique. If the filter outputs both phases of the filter rather than interleaving them together, as is typical, it passes the individual phases to subsequent filters in the chain. Figure 16 shows how the secondary phase output from the filter is passed into the second flexible block. At the output of the two scalable blocks, the I and Q streams must be multiplexed before interleaving the appropriate phase signals.

Summary of Modular Approach

Sharing a datapath between multiple air interfaces is challenging, as the needs include:

- An independent input bus for each system
- An independent sampling-rate equalization chain
- A method to interleave the data together from multiple air interfaces
- Switching coefficient sets at runtime to support multiple air interfaces
- Appropriate partition filtering:
 - A high rate-change CIC filter works for GSM
 - A high rate-change CIC filter does not work for GSM when combined with LTE, as it severely limits the number of channels to be processed
 - Duplicate chains are more efficient
- IP supporting a variable number of channels (or assuming worst case and padding redundant channels with zero)

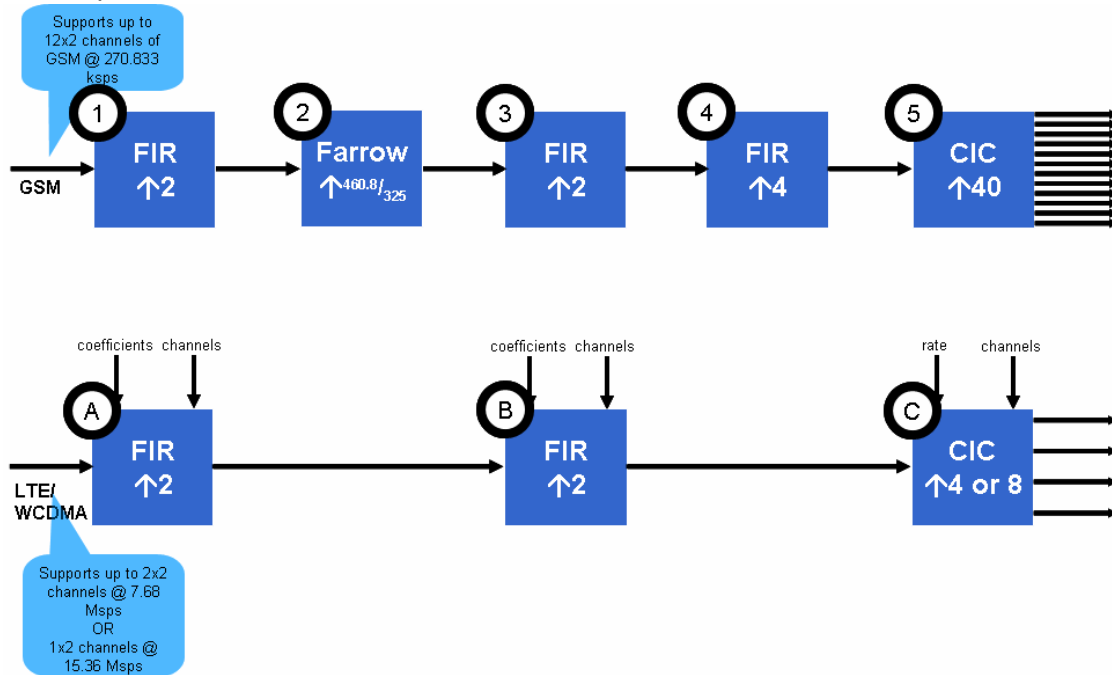
Time-sharing factors should accommodate the highest sampling rate, 61.44 Msps in this case. A 12-carrier GSM DUC chain requires a sampling rate that is ten times less at baseband, so the initial stages of the chain are realized using much simpler hardware. Designing individual processing chains is a more practical approach that offers better filtering performance—due to the custom chains suitable for each air interface—yet offers a more efficient design.

Duplicated DUC/DDC Architectures

Using the same frequency plan as Figure 10, Figure 17 shows an architecture that supports:

- 2X 5-MHz LTE
- 1X 10-MHz LTE
- 2X 5-MHz WCDMA
- 1X 5-MHz LTE, + 1X 5-MHz WCDMA
- 12X GSM
- 12X GSM, 1X 5-MHz LTE/WCDMA

Figure 17. Duplicated Multimode Hardware



Summary of the Properties of the Duplicated Multimode System

This section explores the merits of implementing two data paths, one that supports GSM and one that supports the different requirements of LTE/WCDMA:

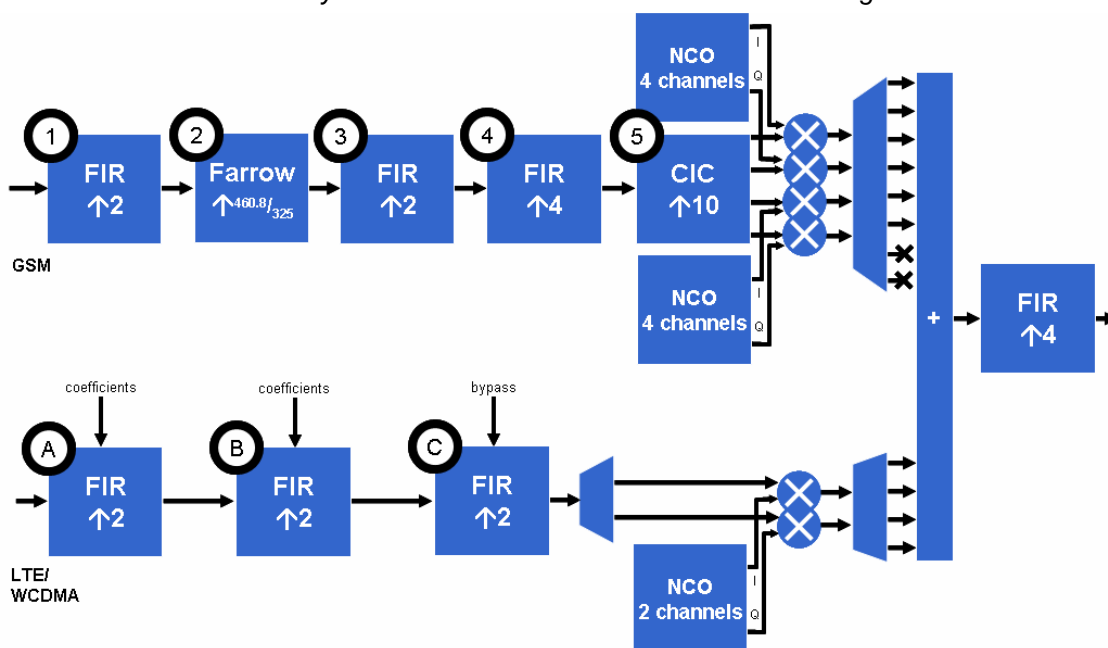
- By partitioning the rate changes associated with GSM, the datapath is as efficient as possible rather than being constrained to the requirements of a different air interface. All FIR filters operate at a relatively low sampling rate, so significant time-sharing is possible.
- The LTE/WCDMA datapath may be shared due to similar sampling rates, but requires coefficient set switching based on the channel number. It may also require a variable number of channels to be supported. This can be avoided if only the worst case is supported (two channels at 15.36 Msps) and the input channel packet is padded. The advantage of a variable number of channels is that they provide more filter taps with the same hardware.
- An additional bypassable FIR/farrow filtering stage is required to support LTEs at 1.4 MHz, 3.0 MHz, and 15 MHz.
- The rate change of individual FIR filters does not need to be variable.

- The outputs of these blocks are required to mix the individual streams with their appropriate carrier (i.e., NCO) and to sum the results together.

Further Improvements

Arguably, an IF-sampling frequency of 245.76 Msps is not required, but it does allow the rate change of the final CIC filter to be adjusted, and the mixing of the carrier frequency at a lower sampling frequency (for example, 122.88 Msps). This enables time-sharing a factor of two, saving half of the multipliers associated with this processing. In addition, since the overall spectrum of the signal of interest is around 10 MHz, the carrier frequency may be mixed at a lower sampling rate, such as 61.44 Msps. Mixing and combining leads to a final upconversion stage using a multichannel FIR filter. As shown in [Figure 18](#), this FIR filter only processes a single IQ channel (for each antenna), leading to significant hardware savings.

Figure 18. Possible Multimode System Architecture With Low-Rate NCO/Mixing



Since the LTE chain supports either two 5-MHz carriers or one 10-MHz LTE carrier, some control logic is needed to enable/disable the unnecessary channels. In addition, it needs a bypassable filter to ensure that the overall rate change results in the correct output sampling frequency. The overall filter-chain design for both LTE and GSM must take into account the common final interpolation-by-four filter. This final filter rate can be adjusted to give the appropriate IF frequency.

Conclusion

Simultaneous multimode support is an emerging basestation requirement as operators try to transition their networks flexibly and seamlessly between 2G, 3G, and 4G technologies. The diverse modulation formats and sampling rates between standards such as MC-GSM, WCDMA, and LTE make designing common building blocks including DUC and DDC challenging. This white paper explores potential multimode DUC architectures including modular and duplicated designs and highlights the tradeoffs between flexibility and FPGA resource usage. Altera's high-performance FPGAs provide an ideal SoC implementation platform for flexible simultaneous multimode RRH design.

Further Information

- *Remote Radio Heads and the Evolution Towards 4G Networks:*
www.altera.com/literature/wp/wp-01096-rrh-4g.pdf
- *Designing Remote Radio Head Applications With Transceiver FPGAs:*
www.altera.com/literature/po/ss-radioheadapps.pdf
- LTE RF Card Solutions:
www.altera.com/end-markets/wireless/lte/rrh-card/wir-lte-rf.html
- Wireless Reference Designs:
www.altera.com/support/refdesigns/sys-sol/wireless/wireless-index.jsp

Acknowledgments

- Lawrence Rigby, Senior Design Engineer, Wireless Systems Solutions Group
- Deepak Boppana, Strategic Marketing Manager, Communications BU



101 Innovation Drive
San Jose, CA 95134
www.altera.com

Copyright © 2009 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.