

Addressing SWaP Challenges in Military Platforms With 65-nm FPGAs and Structured ASICs

Introduction

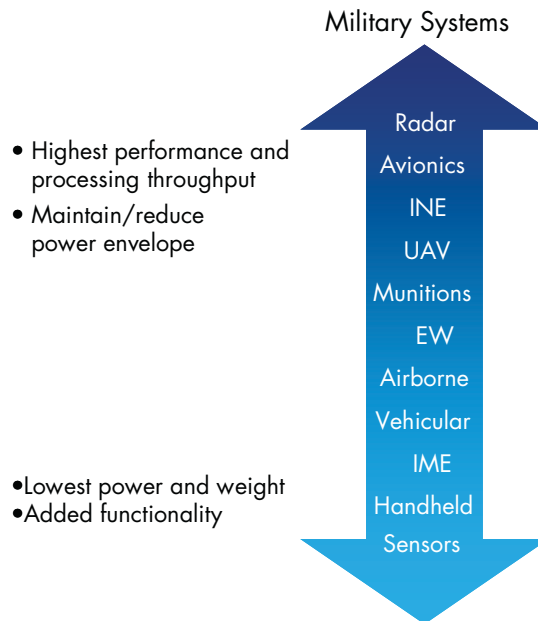
Now more than ever, size, weight, and power (SWaP) must be managed and reduced across virtually all military and aerospace applications to improve operational efficiency and logistics, increase mission life, and reduce the total cost of system ownership. System upgrades are driving added functionality and increased performance, placing additional attention on SWaP. Additionally, markets are expanding as systems become smaller, lighter, and less expensive.

There are obvious challenges to reducing SWaP. Many existing platforms, such as secure communications and radar applications, may have large batteries or power supplies as well as cooling systems such as heat sinks and fans. Even with larger batteries, some of these systems have sustainable mission lives of only a few hours, relegating them to non-deployable lab units. In many other applications, budgets for size, weight, power, or all three may be fixed. Examples include aircraft retrofits where a radio or avionics system must conform to pre-existing chassis size, or radar systems where performance and accuracy must be improved within existing system design limits. Lastly, logistics and maintainability are a challenge. This paper examines the SWaP drivers in military platforms, examines specific applications, and discusses how today’s advanced FPGAs and structured ASICs can be used to effectively address SWaP issues.

Reducing SWaP in Military Systems

SWaP reduction is driven by the needs of the applications, as shown in [Figure 1](#). Many applications require increased functionality and performance, while reducing, or at least maintaining, existing SWaP budgets. For example, an existing chassis size or power bus in an aircraft may set limits on upgrades.

Figure 1. Military Applications SWaP Spectrum



On the other side of the spectrum, some applications require the lowest possible size, weight, power, or all three. Examples include sensors that operate on batteries in the field for months at a time, or handheld radios where battery operation affects mission life. For these applications, the goal is to provide the smallest and lightest product with the longest usable field life.

SWaP Interrelation

Increases in performance and function clearly have an impact on power, which in turn affects power supply type, thermal management requirements, chassis size, and weight. Therefore, it is critical to focus on power reduction early in the design process to meet the smallest size and weight in the end system. SWaP-efficient platforms must target the right silicon solutions to meet static and dynamic power budgets, performance targets, and integration requirements. First, however, it is important to fully understand the end system's needs to target the correct system solution.

Identifying the SWaP Challenges in Secure Communications

In secure communications, there are different requirements for wireless applications, such as mobile radios and sensors, and wireline applications, such as inline network encryptors (INEs) and inline media encryptors (IMEs). For wireless applications, longer mission life and smaller, lighter batteries and radios are critical. Additionally, higher integration is necessary for newer waveforms, such as the soldier radio waveform (SRW). Wireline applications require more functionality, higher performance, and faster encryption designed into the same form factors, and in some cases, smaller form factors such as IMEs.

Identifying the SWaP Challenges in Radar, Sensors, and Electronic Warfare Platforms

Designing for SWaP in radar systems is an increasing challenge. More processing is being pushed to the system front-end, making front-end cards more sophisticated and much more advanced. Enhanced digital beamforming requires increased processing performance, which increases power and heat with limited space for thermal management. New post-processing solutions are driving more power into smaller spaces and new VPX cards place a high importance on cooling, making SWaP a key factor in new system design criteria.

Every advance in technology increases war fighter demands for wider and deeper intelligence. Sensors require greater flexibility, discrimination, range, and reliability, while radar and electro-optical sensors incorporate more sophisticated electronics and signal processing algorithms, leading to challenges in SWaP, including heating and cooling. Designers need to make difficult choices between power and performance at multiple design review points.

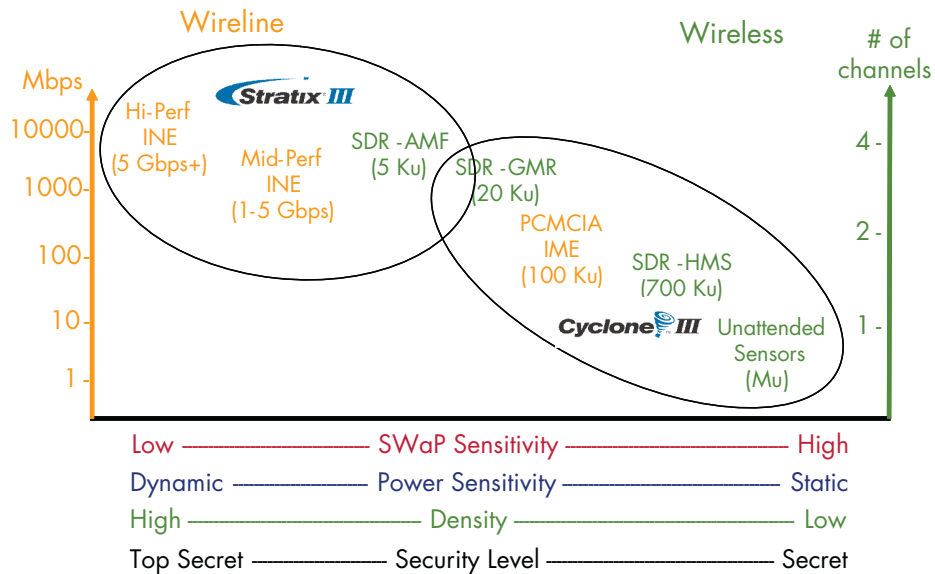
SWaP Challenges in Secure Communications: Case Study

Most wireless and wireline communications systems are bidirectional or full duplex, implying that processing functions for both transmission and reception are required. For example, the receive path processes signals from a medium (RF, copper, or fiber) and converts them into information. Conversely, processing functions from information to transmission include packet processing, cryptographic processing, and waveform and wireline interface processing.

Packet processing includes transforming voice, video, and data into packets, bridging between packet protocols, and routing and switching packets from source to destination, all of which are unsecured. Cryptographic processing involves encrypting bits using redundant crypto engines with classified and unclassified algorithm capabilities, the comparison of encrypted bitstreams to ensure secure encryption, and key generation and management. Waveform (or wireless RF) and wireline interface processing transform encrypted packets into a bitstream for transmission, and transform bits into signals, either through RF—converting bits into symbols, applying modulation, and upconverting symbols to intermediate frequency (IF) and RF—or electrical or optical—converting bits into symbols, applying modulation, and converting symbols to copper or fiber media.

As shown in [Figure 2](#), secure communications applications range from network encryption cards in routers and switches to small form factor modems in sensors and handheld radios.

Figure 2. Secure Communications Application Spectrum



Using Stratix® and Cyclone® FPGAs, HardCopy® structured ASICs, and Quartus® II development software, military system designers can optimize power and performance for their system. The primary applications and FPGA uses are:

- Wireline encryptor blades: In Red/Black separation, gigabit capability for packet processing is required in the red section, whereas the cryptographic section requires gigabit encryption engines. The requirements are similar to commercial communications implementations today.
- Airborne maritime fixed (AMF)-software-defined radio (SDR) requires multiple channels with gigabit capability across for packet processing in the red section and gigabit encryption engines in the crypto section. Requirements are similar to commercial communications implementations today. Waveform processing for multiple protocols on the black side warrants the use of high-performance FPGAs.
- Ground mobile radios (GMR)-SDR requires multiple channels with 100-Mbit packet processing capability and allows spare FPGA bandwidth for digital signal processing (DSP) waveform processing duties on black side.
- Handheld, manpack, and small form factor (HMS)-SDR requires a low-power radio standby mode (ultra-low static power) and a small form factor (low dynamic operating power), due to battery operation.
- PCMCIA inline media encryptors (IMEs) form factor has a 2-W power and 2x3-inch size budget with 100:1 gigabit encryption capability.

Altera Solutions Impact SWaP, Overall Productivity, and System Value

The secure communications applications with greatest SWaP-sensitive requirements are HMS, GMR, and PCMCIA IMEs. Table 1 provides a summary of these applications with corresponding Altera® low-power devices and productivity tools

Table 1. Secure Communication SWaP Sensitive Applications

Benefit	HMS	GMR	PCMCIA IME
Power	Cyclone III static power is one-tenth that of competing devices for longer mission life and more features.	Stratix III Programmable Power Technology and voltage scaling provide 50% lower power than competing devices, enabling more features within the power budget.	Cyclone III static power is one-tenth that of competing devices for more features within the 2-W PCMCIA budget.
	HardCopy II structured ASICs have similar power reduction with anti-tamper capability for sensors.	Seamless migration to HardCopy II structured ASICs provide up to 70% power reduction and anti-tamper capabilities.	HardCopy II structured ASICs have power reductions similar to Cyclone III FPGAs, with anti-tamper capability for encryptor implementations.
Size	Cyclone III FPGA offers low total power, significantly reducing battery size.	Stratix III FPGAs and HardCopy structured ASICs offer high density and superior performance, enabling improved functionality in smaller systems.	Cyclone III FPGAs Small Form Factor (SFF) packaging, such as 0.5-mm ball pitch mBGAs, reduce board area and speed security verification with multi-chip solutions for physical separation.
	Large densities increase integration while small packages reduce board area.		
Weight	Cyclone III power capabilities enable lighter batteries and radios.	Total power savings of Stratix III FPGAs and HardCopy structured ASICs reduces regulation and cooling requirements for lighter systems.	N/A
Productivity	Quartus II design software provides productivity tools to reduce development time. PowerPlay suite provides power optimizations throughout design cycle.	Quartus II design software provides productivity tools to reduce development time throughout the design cycle. PowerPlay suite optimizes Stratix III Programmable Power Technology.	Quartus II design software provides productivity tools to reduce development time. PowerPlay suite provides power optimizations throughout design cycle.
System Value	Cyclone III FPGAs provide the best value per watt, enabling optimum implementations.	Stratix III FPGAs provide the best functionality per watt (Gflops/watt), enabling optimum implementations.	Cyclone III FPGAs provide the best value per watt, enabling optimum implementations.

HMS Form Factor Systems

HMS, GMR, and PCMCIA IMEs have the most SWaP-sensitive requirements. Altera's Cyclone III and Stratix III FPGAs meet these challenges with confident design and efficient SWaP-optimized military production platform implementations. Because soldiers need to carry more ammunition and body armor, not batteries, HMS battery-operated systems have the most demanding requirements for SWaP applications. These challenges include:

- *Severe size and weight restrictions*—The smallest implementations are less than 10 in³.
- *Power consumption directly affects mission life*—Using typical military batteries, today's programmable electronics consume over 4 W, and yield only a 6-hour mission life for the overall radio system.
- *Power budgets dominated by digital electronic processing*—As waveform bandwidth and complexity increases, digital processing absorbs more functionality and power within the radio.
- *Digital logic implementation trade-offs*—Choices for digital processing vary from CPU to ASIC. Typically, DSP devices and FPGAs have provided the best combination of functionality and flexibility with power trade-offs.
- *Static versus dynamic power trade-offs*—Due to the duty cycle of radio modes, standby operation typically dominates radio use by a factor of 10:1. It is therefore imperative to minimize leakage power of digital electronics during standby operation.
- *Voltage and frequency scaling trade-offs to save power*—With careful system design, both voltage and frequency can be scaled back during standby states, leaving only limited functionality in standby mode.
- *Software and hardware partitioning for power*—Software designers need to leverage radio operational modes and intelligently manage hardware resources to minimize power use effectively.

Altera's Cyclone III FPGAs save power for HMS battery-operated systems by increasing mission life fourfold over previous implementations and by adding more triple-play (voice, video, and data) features and software

communications architecture (SCA) capability within the same power envelope. In addition, size and weight are reduced by using much smaller batteries, cooling, and regulation components than previous implementations. Because the smallest implementations must limit the number of components required, entire waveforms are now integrated into a single Cyclone III FPGA, which processes IF, modulation, and bit-level functions at megabits per second.

In addition to increasing mission life by reducing power requirements in these radio platforms, significant size and weight reductions now can be realized. A common battery used in military handhelds is the BA5590 battery (see [Figure 3](#)). If power requirements can be met with a BA5800 battery, size reductions of 92 percent and weight savings of 78 percent can be realized (see [Table 2](#)).

Figure 3. Smaller Batteries Save Size and Weight



Table 2. Comparison of Military Batteries

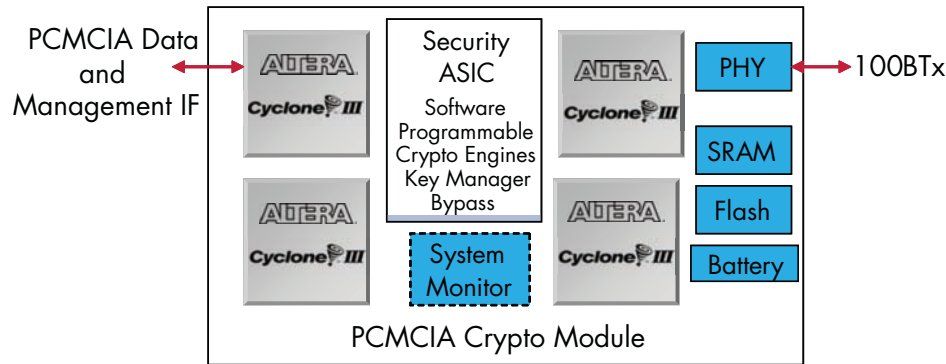
SWaP	Old Battery	New Battery	Savings
Form Factor	Brick	Cylindrical	-
Size, Dimensions	12.5 cm x 11 cm x 6 cm	3 cm x 9 cm	-
Size, Volume	825 cm ³	42 cm ³	95%
Weight	1.0 Kg	0.22 Kg	78%

This savings has other, less obvious benefits, such as operational efficiency and improved logistics. Battery stores and transportation costs quickly add up when batteries for an individual soldier radio weigh over two pounds. Reducing power can drastically lower the cost of ownership from a logistics management perspective.

PCMCIA Inline Media Encryptors

IMEs for PCMCIA enable the use of commercial off-the-shelf (COTS)-based compute platforms for secure military applications. For example, instead of the built-in RJ-45 Ethernet jack, users can plug an existing Ethernet cable into the IME to establish a secure reliable link to the public infrastructure. The SWaP issue for PCMCIA IMEs is a 2-W power budget and a 2x3-inch form factor envelope, as shown in [Figure 4](#).

Figure 4. PCMCIA IME



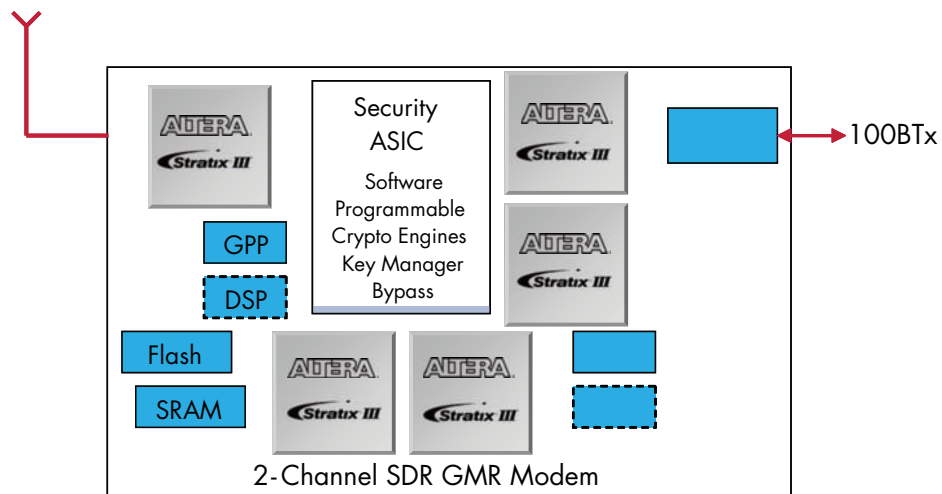
Single-chip IMEs are too power-hungry for these applications, but using multiple low-power Cyclone III FPGAs can reduce power to the 2-W SWaP limit. This solution allows a higher encryption bandwidth and key management capability to be added within the same power envelope. In addition, Cyclone III FPGAs have lower package profiles to fit narrow height requirements and smaller package footprints to enable placement and heat dissipation flexibility.

Altera’s 65-nm Cyclone III FPGAs are optimized for SWaP production. The combination of resource capacity, including logic elements (LEs), embedded memory, multipliers, and I/Os, coupled with the most aggressive power reduction techniques and smallest packaging, enable superior SWaP implementations. Low-power FPGAs such as Cyclone III devices are optimized for battery-operated radios with sufficient signal processing resources for advanced waveforms at one-tenth the static power compared to 90-nm devices.

Ground Mobile Radios

GMRs are at the heart of future combat systems. They form the vehicular link between the soldiers and command structure for network-centric warfare. GMRs require 4-channel multiple waveforms at higher bandwidths than HMS radios and have different SWaP needs. The functionality is much higher the HMS radios, while the power concern is reduced. For this application, Stratix III devices provide more functional capability, while keeping power in check (see Figure 5).

Figure 5. 2-Channel GMR Modem



Stratix III Programmable Power Technology adds triple-play features, waveform flexibility, packet processing, and SCA capability to a vehicular power envelope that can withstand environmental extremes of desert warfare with much smaller cooling and regulation components than previous implementations. With 340K LEs, and +17 Mbytes

of memory, Stratix III FPGAs can integrate multiple waveforms into a single FPGA, and process IF, modulation, and bit-level functions at megabits per second. With advanced I/O interfaces, Stratix III FPGAs can perform coprocessing with general-purpose processors (GPPs) and DSP devices, and with advanced soft core CPUs, Stratix III FPGAs can perform packet processing for the GPP.

Altera's high-performance, high-density Stratix III FPGAs provide maximum functionality with minimum power using advanced architecture capabilities including Programmable Power Technology and Selectable Core Voltage. With the maximum DSP performance available, these devices are designed to address the broadest range of AMF devices, GMRs, and special operation modems.

Silicon Solutions for SWaP-Constrained Systems Targeting

Today's advances in 65-nm FPGAs such as Cyclone III and Stratix III FPGAs, HardCopy II structured ASICs, and Quartus II development tools have all been designed taking key military-aerospace application requirements in mind, with power reduction as the top priority.

TSMC's 65-nm low-power (LP) process, already proven in production by leading suppliers of mobile phone semiconductors, is a key factor in power reduction. Cyclone III devices are the only low-power FPGAs with the density required to support the soldier radio waveform in under 200 milliwatts of static power, versus multi-watt restrictions in prior solutions. Altera's Cyclone III FPGAs are optimized for low power to help you manage thermal requirements, reduce or eliminate system cooling costs, and extend battery life for handheld applications. The Cyclone III device family offers the only FPGA with up to 120K logic elements (LEs) that consumes less than 0.2 watts of static power.

Stratix III devices provide the highest performance in the industry while using 50 percent less power than previous generation FPGAs, enabling the highest throughput-per-watt for performance driven systems that must still be power conscious. With innovations at the silicon level, circuit technologies, architecture and software tools, next-generation military platforms can add performance and functionality without adversely affecting power budgets.

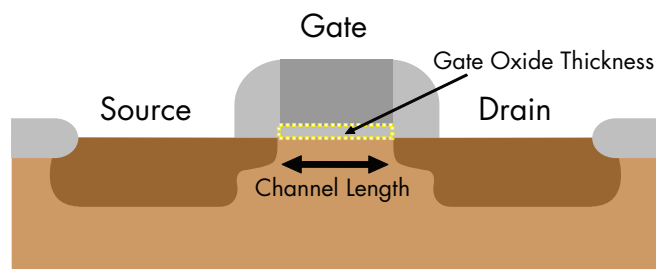
For systems with the highest density and performance demands, HardCopy structured ASICs provide the industry's only seamless FPGA-to-structured ASIC flow, enabling systems' needs to add functionality or integrate functions, increase performance while reducing power, and provide cost advantages for volume applications.

Solving the SWaP Dilemma: Cyclone III Low-Power FPGAs

Cyclone III FPGAs are developed on TSMC's 65-nm low-power (LP) process technology, which is also employed by other major semiconductor manufacturers for handset components. The smaller geometries made possible by this advanced process combined with architectural optimizations enable Cyclone III devices to deliver up to 30 percent lower total power consumption compared to 90-nm-based Cyclone II devices by keeping dynamic and static power consumption to a minimum. The process and architectural enhancements that Altera employs with Cyclone III devices includes the use of low-k dielectrics, variable channel lengths and oxide thicknesses, and multiple transistor threshold voltages (see [Figure 6](#)).

For more information on these enhancements, visit [Delivering the World's First Low-Cost 65-nm FPGAs](#).

Figure 6. TSMC 65-nm Process



Cyclone III FPGAs employ multiple oxide thicknesses, using thicker gate oxides for noncritical speed transistors to lower the leakage current flowing through those transistors, which in turn, reduces static power consumption. Using multiple threshold voltages provides the opportunity to use higher threshold voltages for noncritical speed transistors to reduce leakage current.

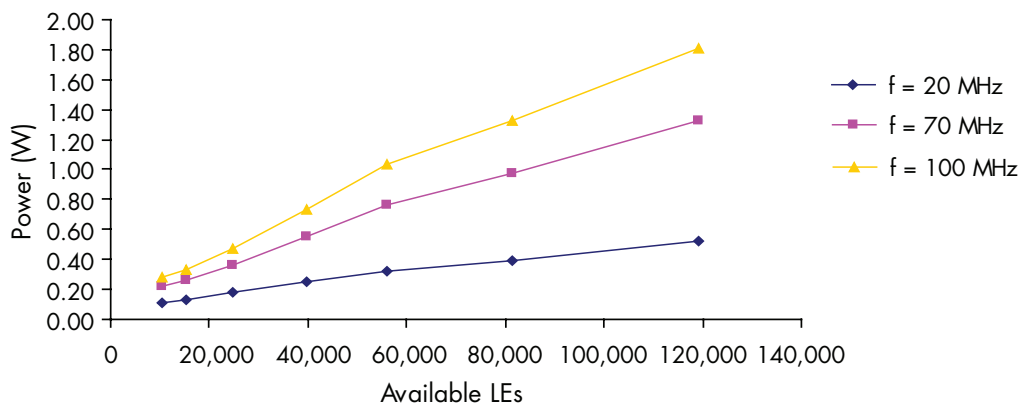
The gate or channel length of a transistor affects its speed and subthreshold leakage. As the length of a transistor approaches the minimum gate length of the 65-nm process, the subthreshold leakage current increases significantly. Altera uses longer gate lengths to reduce leakage current in circuits where performance is not required, and short gate lengths where performance is critical. Altera also uses low-k dielectrics in Cyclone III FPGAs to insulate metal layers, which reduces capacitance and has a direct relationship with reducing dynamic power consumption.

Cyclone III FPGA Power Consumption

Cyclone III FPGAs are optimized for low power to help you manage thermal requirements, reduce or eliminate system cooling costs, and extend battery life for handheld applications. The Cyclone III device family is the first to offer an FPGA with up to 120K logic elements (LEs) that consumes less than 0.2 watts of static power.

Figure 7 shows typical power consumption for Cyclone III family FPGAs at different operating frequencies. At a representative operating frequency such as 20 MHz, the largest Cyclone III device, the 120K-LE EP3C120, consumes less than 600 mW of power. Even at operating frequencies as high as 100 MHz, the EP3C120 consumes less than 2 W of power.

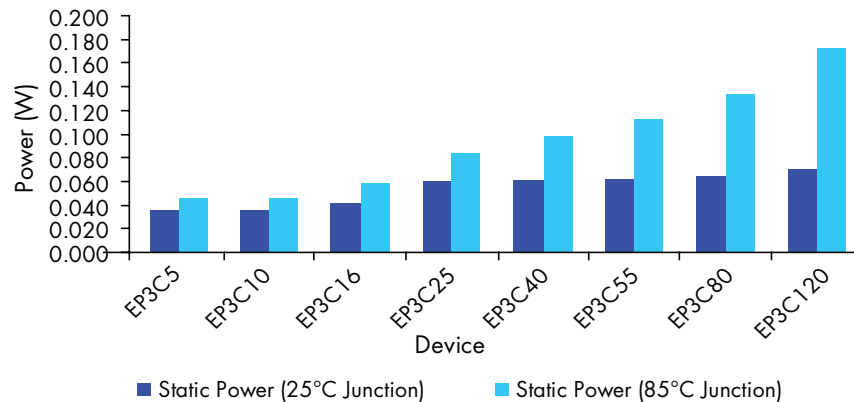
Figure 7. Typical Power Consumption of Cyclone III FPGAs



Static power can increase dramatically with the 65-nm semiconductor process if no power-reduction strategies are employed. Static power consumption rises at sub-micron process technologies largely because of increases in leakage current (including tunneling current across the thinner gate oxides that are used in the 65-nm process), as well as subthreshold leakage (channel- and drain-to-source current). Altera has taken significant steps to reduce static power in Cyclone III devices.

Figure 8 shows the static power consumption of Cyclone III devices at 25°C and 85°C junction temperature. The smallest Cyclone III device consumes as little as 35 mW at 25°C, and the largest Cyclone III device consumes as little as 170 mW static power at 85°C.

Figure 8. Typical Static Power Consumption of Cyclone III FPGAs



Solving the SWaP Dilemma: Stratix III High-Performance FPGAs

Stratix III devices provide the highest performance in the industry while using 50 percent less power than previous-generation FPGAs. Next-generation military platforms can take full advantage of these Stratix III FPGA power conservation innovations:

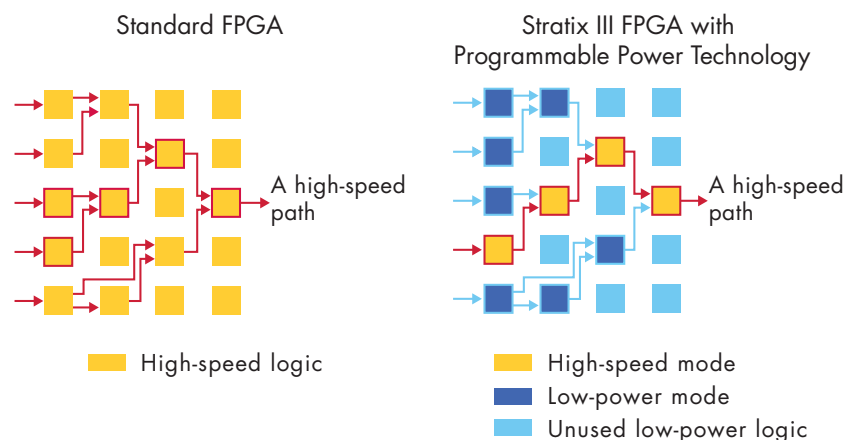
- Programmable Power Technology
- Selectable Core Voltage
- Process and Circuit Technologies
- Quartus II PowerPlay Power Analysis and Optimization Tool
- Stratix III PowerPlay Power Estimator

Programmable Power Technology

Available exclusively in Stratix III FPGAs, Programmable Power Technology enables every programmable logic array block (LAB), digital signal processing (DSP) block, and memory block to deliver high speed or low power, depending on your design requirements.

All other FPGAs contain blocks that are designed to run at only one speed—the highest possible—to support timing critical paths (as depicted by yellow blocks in Figure 9). Using the Programmable Power Technology in Stratix III FPGAs, all logic blocks in the array except those designated as timing critical are set to low-power mode (as depicted by blue blocks in Figure 9). With only the timing critical blocks set to high-speed mode, power dissipation in Stratix III devices is substantially reduced.

Figure 9. Standard FPGA Fabrics vs. Stratix III FPGA Fabric With Programmable Power Technology



Most designs have very few critical paths that need the highest performance logic to meet timing, while the majority of the design paths have ample excess slack (based on slack histograms for 71 customer designs). Quartus II software uses the Stratix III Programmable Power Technology to automatically take advantage of the excess slack found on non-critical design paths and minimizes power consumption while maintaining the highest performance possible in critical paths.

 For more information about design slack histogram analysis, refer to [Stratix III Programmable Power](#).


Selectable Core Voltage

Another unique Stratix III power feature (independent of Programmable Power Technology), called Selectable Core Voltage, gives you the option of using a power-saving 0.9V core voltage. Designs needing the highest performance use the 1.1V core voltage, while designs requiring minimum power consumption can use the 0.9V core voltage. Programmable Power Technology lowers power significantly, independent of which core voltage is used.

 For more information about Selectable Core Voltage, refer to [Stratix III Programmable Power](#).

Process and Circuit Technologies

Stratix III devices use the latest process and circuit techniques along with major circuit and architecture innovations to minimize power and still deliver the highest performance of any FPGA. Some of the technologies employed in Stratix III FPGAs include multi-threshold transistors, variable gate-length transistors, low-k dielectric, triple-gate oxide (TGO), super-thin gate oxide, and strained silicon.

 For additional information on these process and circuit technologies, refer to [Stratix III Programmable Power](#).

Quartus II PowerPlay Power Analysis and Optimization Tool

The Quartus II PowerPlay power analysis and optimization tool helps keep the total power consumption of your designs to a minimum. Altera began offering advanced power optimization capabilities in Quartus II software in 2005, and it immediately provided an average 25 percent reduction in dynamic power in our customers' designs.

Since then, the PowerPlay power analysis and optimization tool has been improved with the addition of intelligent decision making in synthesis, placement, and routing. Today, by working in conjunction with Programmable Power Technology in the Stratix III silicon, the power consumption minimizing capability of PowerPlay power optimization is the best it has ever been.

 To learn more, visit [Power Optimization for Stratix III FPGAs](#).

Tools and IP

Productivity tools play a key role in reducing design effort and minimizing program risk for military systems. Designers can leverage third-party and FPGA vendor intellectual property (IP) and tool offerings such as Altera's Quartus II development software. These offerings can accelerate time-to-market with advanced tool capabilities, including accurate power estimation and optimization, virtual team and project management, automated system integration, and application acceleration capabilities that automate and simplify the design flow for integrating both existing and newly developed algorithms. Some high-productivity software suites simplify porting and debugging of advanced waveforms and enable design methodologies like software programmable reconfiguration (SPR). SPR methodology reduces risk, leverages IP reuse, and even enables lower power and cost implementations using FPGA-based structured ASIC devices.

Supplier Ecosystem

To begin development of application software as quickly as possible, designers can leverage modular development baseboards for the desired device families. Device baseboards with high-speed I/O interfaces can extend functionality and I/O flexibility, providing advanced prototyping capabilities using modular supplier and third-party-developed

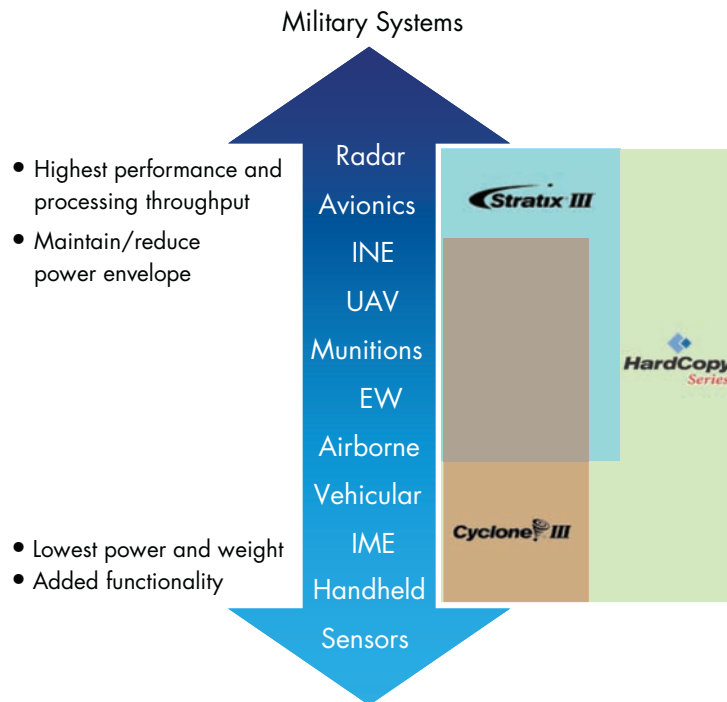
daughter cards. For rugged system implementations, COTS system companies offer a wide range of industry-standard interface boards, including VME, PCI, and AMC form factors, while system integrators and SCA suppliers can provide middleware, engineering, and application expertise across SDR and other military segments.

Beyond SWaP solutions, some FPGA suppliers focus on the special requirements of the military and aerospace market, going far beyond basic COTS devices. Suppliers with enhanced COTS capabilities offer business practices and services tailored to military government contractors, such as device encryption security features for anti-tampering, bare die for multichip module integration, single-event upset (SEU) detection, availability of reliable leaded packaging, and more. Devices for SWaP applications should be qualified across industrial and military temperature ranges, including verified performance under environmental extremes. Using enhanced COTS devices for defense applications also enables major price and lifecycle advantages, compared to dedicated military devices.

Conclusion

FPGAs continue to provide more flexibility and functionality at reduced cost. Altera's latest generation FPGAs provide an optimum solution for SWaP requirements by enabling new secure communications, sensors, radar, and other military systems with smaller footprints, lighter weight, and smaller batteries. As shown in Figure 10, Altera provides SWaP-sensitive solutions across key military applications, resulting in optimum implementations, supporting the highest functionality per watt available in 65-nm FPGAs. This includes the highest performance per watt with Stratix III FPGAs for applications such as radar, and lowest static power for waveform integration under 0.2 W with Cyclone III FPGAs. For performance-driven applications that do not require reprogrammability in the field, HardCopy II structured ASICs offer an ITAR-compliant, seamless FPGA-to-structured ASIC solution. Quartus II development tools support PowerPlay Power Analysis and Optimization Technology to optimize system power. For confident design and efficient SWaP-optimized military production platform implementations, explore Altera's latest 65-nm Cyclone III and Stratix III FPGAs.

Figure 10. Military Applications SWaP Spectrum



Further Information

SWaP

- Military Secure Communication:
www.altera.com/end-markets/military-aerospace/secure/mil-secure.html
- SWaP webcast:
www.altera.com/end-markets/military-aerospace/swap/mil-swap.html

Cyclone III FPGAs

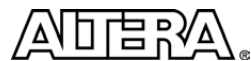
- *Achieving Low Power in 65-nm Cyclone III FPGAs:*
www.altera.com/literature/wp/wp-01016.pdf
- Delivering the World's First Low-Cost 65-nm FPGAs:
www.altera.com/products/devices/cyclone3/overview/power/cy3-65nm-lowpower.html

Stratix III Programmable Power Technology

- Stratix III FPGA Low Power Consumption Features:
www.altera.com/products/devices/stratix3/overview/power/st3-power.html
- Power Optimization for Stratix III FPGAs:
www.altera.com/products/devices/stratix3/overview/power/st3-power-tools.html
- *Stratix III Programmable Power:*
www.altera.com/literature/wp/wp-01006.pdf

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