White Paper

Reduce Total System Cost in Portable Applications Using MAX II CPLDs

Introduction

Traditionally, portable system designers have used ASICs and ASSPs to implement memory interfaces, I/O expansion, power-on sequencing, discrete logic functions, and display functions in portable systems. Low-cost, low-power, and small board space requirements have limited the use of programmable logic devices in portable applications. Today, however, low average selling prices combined with low power consumption and small form-factor packages allow programmable logic devices to replace or augment ASICs, ASSPs, and discrete devices in portable applications.

Due to their very low-cost and differentiating product features such as new ultra-small form-factor packages, high density, on-chip voltage regulator, and new power-down capability, MAX® II CPLDs offer portable system designers, on average, 50 percent lower cost and power than competing CPLD solutions. They continue to provide the time-to-market and flexibility benefits that ASICs and ASSPS cannot deliver.

Portable System Challenges

Portable applications are proliferating as demand increases for small, inexpensive products that support high levels of functionality with extended battery life. Table 1 lists some end markets and applications.

Table 1. Portable Markets and Applications

Markets	Applications
Consumer	• Educational toys • Portable media players
Industrial	• Barcode scanners • Industrial PDAs • Camera modules
Medical	• Handheld ultrasounds
Test and Measurement	• Handheld testers • Multimeters
Wireless and Wireline	• PCMCIA cards • Optical modules
Automotive	• Mobile GPS

As portable systems continue to shrink and get cheaper, the demand to support higher levels of functionality at a lower cost increases and poses a challenge for system designers. Board components such as an external voltage regulator, external clock sources for power-up sequencing, and discrete logic devices that implement logic functions for voltage level translation and serial I/O expansion are a direct function of the end product cost. Thus, the more components on a board, the more expensive the end product.

Portable system designers also need to reduce the board space due to shrinking product size. Designers need very small form-factor packages that can integrate complex logic functions such as battery charger functions, display graphics, and display protocol bridging and translation functions, as well as support very I/O intensive functions such as memory management functions.

Power consumption is another challenge portable design engineers face. Consumers demand smaller products with more features, but also want extended battery life to meet their mobile lifestyles. Three aspects of power design most concern portable system designers: dissipation, simplicity, and transitions. Power dissipation consists of dynamic and static components; in most portable applications, low dynamic power is required to extend the battery life, though for some applications, low static power is required. Extending the battery life of a product by lowering the dynamic or static power dissipation is desirable but not always at any cost.

The power system should also be as simple as possible. In battery-powered applications, multiple power rails can be very prohibitive. It is critical that a portable system with multiple power domains have a very flexible control mechanism and that each domain be very easy to power up and power down. Power transitions are also important, as a typical power management system is constantly transitioning from one power mode to another. Depending on the hot-socket characteristics of a device, it might consume more power parasitically in the “off” state than in the “on” state, due to poor hot-socket characteristics.

Another challenge faced by engineers is related to the lifespan of the portable product in development. Portable products may have changing standards such as display requirements over time, including the need to show text, graphics, and video. The fixed-function nature of ASICs and ASSPs does not support changing product requirements like these very well. In addition, ASICs, ASSPs, and discrete devices often become obsolete over time as process technology advances. As a result, system designers using these devices can be forced into costly and time-consuming hardware and software redesigns.

MAX II CPLDs Reduce Total System Cost and Board Space

The functionality provided by ASICs, ASSPs, and discrete devices in portable applications can be integrated into Altera® MAX II CPLDs, which offer the maximum logic capability in ultra-small form-factor packages. These packages are ideal for functions that require high I/O count per board area, such as interfacing with an LCD display, keypad, flash, or memory in portable applications. In addition, they also provide a high logic-to-board area ratio, which is needed for integration of discrete components to minimize PCB space.

MAX II CPLDs are offered in low-cost thin quad flat pack (TQFP), FineLine BGA® (FBGA) (1.0-mm pitch) and Micro FineLine BGA (MBGA) (0.5-mm pitch) packages. Ideal for portable applications, the small form-factor 100-pin and 256-pin 0.5-mm MBGA packages enable the portable system designer to pack more functionality into less board space so as to develop smaller products without sacrificing on device functionality. Figure 1 shows the package footprints of the 0.5-mm MBGA packages.

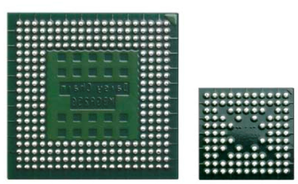

Figure 1. 0.5-mm MBGA Package Footprints (Left: 256 Pin; Right: 100 Pin)

These small form-factor packages offer the compact size of a 0.5-mm BGA with the easy breakout of a partially populated array. The packages are designed so that all pins and power connections can be broken out with only two layers of the PCB.

Besides saving board space, the ultra-small form-factor package lowers total system cost by enabling system designers to integrate 50 percent more user I/O and logic density per board area (mm^2) than other CPLDs. Table 2 shows a comparison of the I/O per mm^2 and macrocells per mm^2 of some CPLD families. On average, the small form-factor packages on MAX II CPLDs offer 50 percent more I/O per board area (mm^2) and 200 percent more logic density per board area (mm^2) than comparable CoolRunner-II and ispMACH 4000Z packages.

Table 2. I/O per mm^2 and Logic Density per mm^2 Comparison of CPLD Families

PLD Family	Device	Package	Size	I/O	MC	I/O per mm^2	MC per mm^2
CoolRunner-II	XC2C64	CP56	6x6	45	64	1.25	1.78
ispMACH 4000Z	4064Z	CS56	6x6	32	64	0.89	1.78
ispMACH 4000Z	4064Z	CS132	8x8	64	64	1.00	1.00
MAX II	**EPM240**	**M100**	**6x6**	**80**	**192**	**2.22**	**5.33**
CoolRunner-II	XC2C128	CP132	8x8	100	128	1.56	2.00
ispMACH 4000Z	4128Z	CS132	8x8	96	128	1.50	2.00
MAX II	**EPM240**	**M100**	**6x6**	**80**	**192**	**2.22**	**5.33**
CoolRunner-II	XC2C256	CP132	8x8	106	256	1.66	4.00
ispMACH 4000Z	4256Z	CS132	8x8	96	256	1.50	4.00
MAX II	**EPM570**	**M100**	**6x6**	**76**	**440**	**2.22**	**12.22**

The high density of the MAX II device reduces the number of board components, which also reduce total system cost. The MAX II device supports a MultiVolt™ core (Figure 2), which allows these devices to operate with a 1.8-V, 2.5-V, or 3.3-V supply voltage, and allows system designers to minimize the number of power rails and simplify the board-level design.

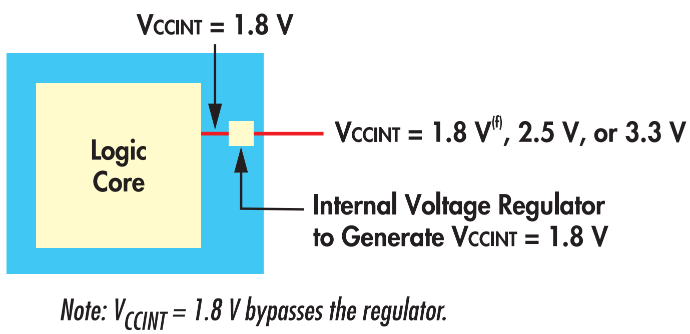

Figure 2. MultiVolt Core Operation

One less power rail can mean fewer traces on the PCB, which means fewer board layers, thereby reducing total system cost. MAX II devices also support a low-frequency internal oscillator that can eliminate the need for external clock sources for power-up sequencing or event timers and keyboard encoders.

Table 3 shows a comparison of the costs and benefits of some ASSP, discrete device, and CPLD solutions used in typical portable applications. MAX II CPLDs reduce the total solution cost of the portable system, as they offer programmable logic resources that integrate other board functions, reducing board space and system complexity. Also, MAX II CPLDs are a better alternative to ASSPs and discrete devices as they are not prone to obsolescence.

Table 3. Comparison of Altera MAX II CPLD-Based and Discrete-Based Functions in Portable Systems

Solution	CPLD Density (MCs)	Voltage Regulator	Frequency Oscillator	BOM Flexibility *(2)*	Obsolescence	Approximate Solution Price *(3)*
Altera MAX II EPM240M100C5	192	✔	✔	✔	✔	$4.80
Microchip PIC16F883-I/SP + TI TPS79118DBVR (LDO) + TI SN74AHC1G00DBVR (voltage translator) + TI PAL16R4 (I/O expander)		✔	✔			$4.45
FTDI 245RL (ASSP) + TI TPS79118DBVR (LDO) + TI PAL16R4 (I/O expander)		✔				$4.76
Non-Altera CPLD *(1)* + TI TPS79118DBVR (LDO) + Microchip PIC12F683-E/SN-ND (power-up sequence controller)	128-256	✔	✔	✔	✔	$8.00-$16.50

Notes:
(1) An example of a non-Altera CPLD is the Xilinx XC2C128CP132-7C (priced at $7.31 for 1000 units)
(2) BOM flexibility is the ability to work with multiple/different suppliers (e.g., display, flash, or A/D converter suppliers)
(3) Pricing based on 1000-unit list price

MAX II CPLDs Reduce and Simplify Total System Power

MAX II devices have many power system characteristics that are beneficial for portable applications. MAX II devices deliver the lowest dynamic power in the CPLD industry and offer a power-down capability that conserves battery life. In a typical portable application, the system is either running or is off, waiting for a user to turn on the system. PLDs with low core voltage can mask the true power of the application. The total power consumed by the PLD is $V_{CCINT} * I_{CC}$, where I_{CC} is the dynamic and static I_{CC} of the PLD device. The V_{CCINT} voltage is derived from a low dropout regulator (LDO), which generates the core voltage level.

Figure 3 shows a comparison of system power curves for the MAX II device and CoolRunner-II device, using a 3.0-V lithium polymer battery. The application example has 128 registers of core state machine logic and 16 switching inputs running at the specified frequency. The dashed line for the CoolRunner-II device represents the actual power dissipated by the system, which includes the power dissipated by the LDO regulator running off the battery and supplying the 1.8-V core.

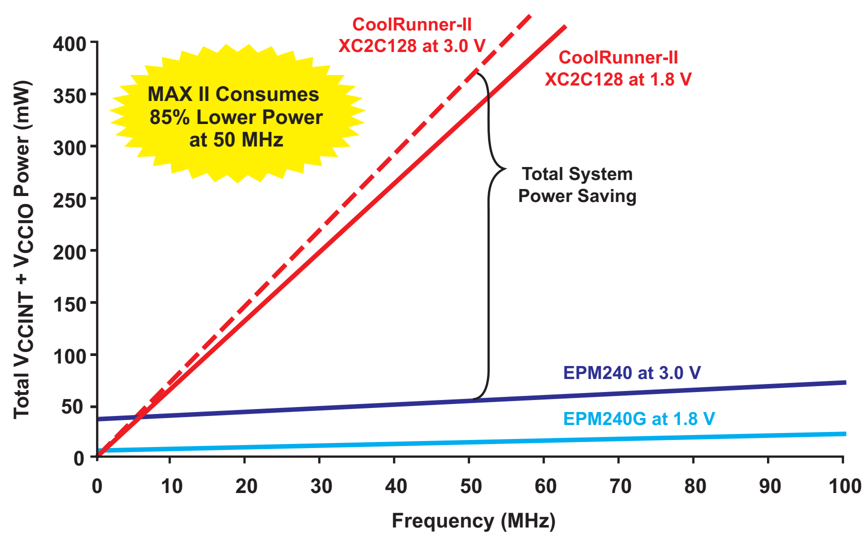

Figure 3. MAX II vs. CoolRunner-II: Dynamic Power Dissipation in Portable System

The new, easy-to-use power-down capability of MAX II CPLDs enables portable system designers to achieve zero power at 0 MHz. Unlike competing CPLDs, the superior power system characteristics of MAX II CPLDs—such as hot-socketing support, power-sequence flexibility, and single power supply simplicity—enable them to be completely powered down without any power-sequence restrictions, thereby conserving battery power when the portable system is not in use.

Figure 4 shows the ability of the MAX II device to achieve zero power at 0 MHz when completely powered down. The application example assumes 50 percent of inputs are stuck at V_{CC} and 50 percent are at GND when the CPLD's V_{CCINT} and V_{CCIO} are powered down. As illustrated, the leakage current through the I/O pins on the CoolRunner-II device results in greater power dissipation when the device is "off" compared to when the MAX II device is "off." Multiple I/Os at V_{CC} or GND have very little or no effect on the MAX II device's power dissipation when it is turned "off". Existing PLD devices cannot be turned "off" to save power unless every input from all parts of the circuit is guaranteed to be "off." MAX II devices have no such requirement.

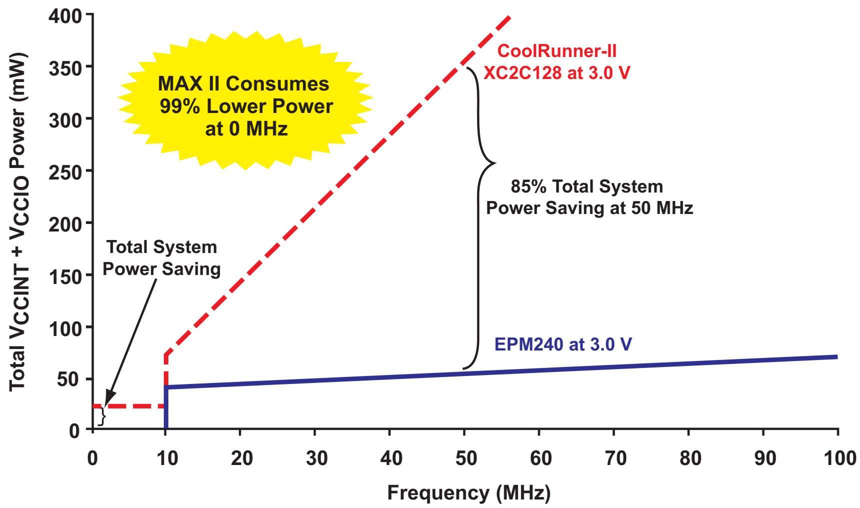

Figure 4. MAX II vs. CoolRunner-II: Power Down Mode in Portable System

Table 4 shows the power characteristics of various CPLDs.

Table 4. Power Specification Comparisons

Family	Minimum Power Rails *(1)*	Maximum I/O Banks	Power-Up Sequence Requirement	Hot-Socket Leakage
MAX II	1	4	No	No
MAX IIG	2	4	No	No
MachXO	2 *(2)*	4	No	Yes
ispMACH 4000Z	2	2	No	Yes
CoolRunner-II	2	2	Yes	Yes

Note:
(1) Power rails required in a 3.3-V I/O battery-powered system
(2) MachXO V_{CC} and V_{CCIO} work over wide range 1.71-3.465-V but V_{CCAUX} has a limited range of 3.135-3.465-V

The second column of Table 4 shows the minimum number of power rails needed in a battery-powered 3.3-V I/O portable system. In such a system, at least one or more I/O banks are at 3.3 V. The other power rails are required for non-3.3-V core supplies and various auxiliary supply requirements of the respective PLDs. There is a distinct advantage to having fewer power supplies. The minimum number of supplies required by a MAX II device is one supply. Furthermore, MAX II devices have the same single-supply capability for 2.5-V systems and can even operate over a 2.3-V to 3.2-V range, as required in a battery-powered portable system.

The third column of Table 4 shows the number of independent I/O banks. Although 3.3 V will be the most common system voltage, there are applications that utilize PLDs for voltage-level shifting. Compared to other CPLD devices, MAX II devices have the most number of I/O banks. Even in cases where only two V_{CCIO} levels are required, having four is an advantage, as they offer more flexibility when assigning pins to power rails.

The fourth column shows whether there is any requirement for sequencing V_{CC} power rails during power up. A "no" is most desirable, as it puts no restriction on the user to power-up or power-down V_{CCIO}, V_{CCINT}, or V_{CCAUX} in any specific order. MAX II CPLDs have no restrictions on the power-up order. In the case where V_{CCIO} and V_{CCINT} are the same supply, this is not even a concern. A "yes" indicates that not following a prescribed sequence will result in unwanted current surges or possibly a stuck state. Requiring a specific power-up sequence can increase the complexity and total cost of a system. It may also prevent the use of the PLD to control the power-up sequence of other devices on the board.

The fifth column of Table 4 shows whether the device has full hot-socket protection. The main hot-socket concern is the I/O pin leakage when power is not applied to the PLD. Hot-socket leakage is the current leakage of an I/O pin at V_{CC} or GND when the device V_{CCIO} or V_{CCINT} is not applied. Hot-socket leakage can cause system power dissipation through an I/O pin even when the device is powered down. MAX II devices offer hot-socket support with very low static hot-socket leakage. The hot-socket feature removes some of the difficulty that designers face when using components on PCBs that have a mix of 3.3-, 2.5-, 1.8-, and 1.5-V devices that are powered down in different modes. In a portable system, hot-socket support facilitates power-down of sections of the system without unwanted parasitic leakage paths through the CPLD I/O pins.

Conclusion

MAX II CPLDs offer several key benefits over ASIC, ASSP, discrete, and other CPLD devices. The ultra-small form-factor packages combined with high-density, core voltage regulator, and internal frequency oscillator features, allow system designers to integrate existing discrete devices on a board, reducing total system cost and minimizing board space. In addition, MAX II CPLDs enable the system designer to not only reduce system power consumption, but also to simplify system power management in the end product. For most portable applications where ASICs, ASSPs, and discrete devices are traditionally used, MAX II CPLDs' low total solution cost provides a compelling argument for replacing or augmenting these devices.

Additional Resources

- MAX II Power-Down Design:
  www.altera.com/support/examples/max/exm-power-down.html
- Portable Applications Using MAX II Devices:
  www.altera.com/max2-portable
- *AN 422: Power Management in Portable Systems Using MAX II CPLDs:*
  www.altera.com/literature/an/an422.pdf
- *AN 114: Designing With High-Density BGA Packages for Altera Devices:*
  www.altera.com/literature/an/an114.pdf

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