



# Temperature Sensor (ALTTEMP\_SENSE) Megafunction

## User Guide



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This user guide describes the features of the ALTTEMP\_SENSE megafunction that you can configure through the MegaWizard™ interface in the Quartus® II software.

The ALTTEMP\_SENSE megafunction configures the temperature sensing diode (TSD) block to utilize the temperature measurement feature in the FPGA. The TSD block includes an 8-bit analog to digital converter (ADC), a clock divider, a comparator, a decoder, and a temperature sensing diode.

 This user guide assumes that you are familiar with megafunctions and how to create them. If you are unfamiliar with Altera® megafunctions or the MegaWizard interface, refer to the [Megafunction Overview User Guide](#).

## Features

The ALTTEMP\_SENSE megafunction provides the following features:

- An internal TSD with built-in 8-bit ADC circuitry to monitor die temperature
- A clock divider to reduce the frequency of the clock signal to 1 MHz or less before clocking the ADC
- An asynchronous clear signal to reset the TSD block

## Device Support

The ALTTEMP\_SENSE megafunction supports the following device families:

- Stratix® V
- Stratix IV
- HardCopy®IV

This section describes the parameter settings for the ALTTEMP\_SENSE megafunction.

You can parameterize the megafunction using the MegaWizard Plug-In Manager or the command-line interface (CLI). Altera recommends that you configure the megafunction using the MegaWizard Plug-In Manager.

Expert users may choose to instantiate and parameterize the megafunction through the command-line interface using the clear box generator command. This method requires you to have command-line scripting knowledge.


 For more information about using the clear box generator, refer to “Clear Box Generator” on page A-1.

Table 2-1 lists the MegaWizard and CLI parameter settings for the ALTTEMP\_SENSE megafunction.

**Table 2-1. ALTTEMP\_SENSE Parameter Settings**

MegaWizard Parameter		CLI Parameter		Description
Name	Legal Values	Name	Legal Values	
<b>General Options Page</b>				
What is the input frequency?	<b>1.0 – 80.0 MHz</b>	clk_frequency	1.0 – 80.0	Specifies the input frequency of the <code>clk</code> signal. The input frequency value must be less than or equal to the clock divider value.  The CLI parameter is type string.  The default value is <b>1.0</b>
What is the clock divider value?	<b>40, 80</b>	clock_divider_value	40, 80	Specifies the clock divider value. The megafunction divides the clock frequency value with the clock divider value before feeding the ADC. This option is only enabled when the <code>clk</code> signal frequency is more than 1 MHz.  Altera recommends clocking the ADC with a 500 kHz signal.  The CLI parameter is type integer. Ensure that you enable the clock divider by setting the <code>clock_divider_enable</code> parameter value to <code>on</code> .  The default value is <b>40</b> .

Table 2-1. ALTTEMP\_SENSE Parameter Settings

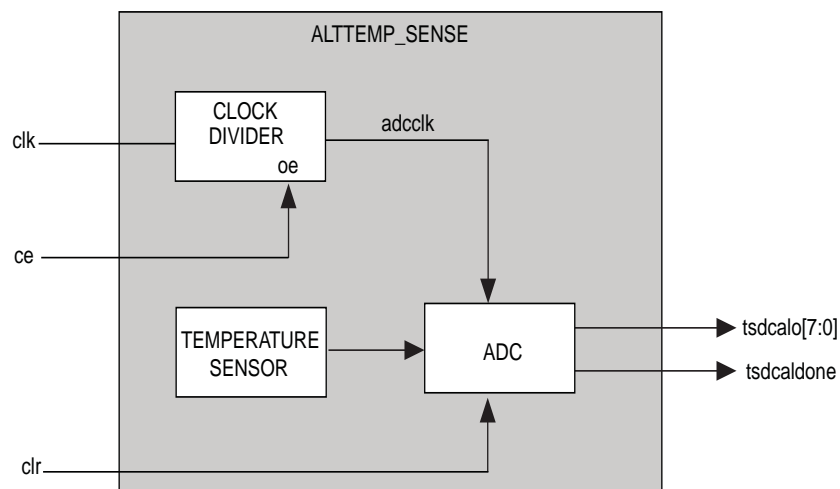
MegaWizard Parameter		CLI Parameter		Description
Name	Legal Values	Name	Legal Values	
Create a clock enable port	On/Off	ce	—	Specifies whether to turn on the asynchronous clock enable ( <i>ce</i> ) port. Turn on this option when you want to enable the ALTTEMP_SENSE megafunciton. When you turn off this option, the clock enable port automatically connects to VCC.
Create an asynchronous clear port	On/Off	clr	—	Specifies whether to turn on the asynchronous clear ( <i>clr</i> ) port. Turn on this option when you want to reset the ALTTEMP_SENSE megafunciton. When you turn off this option, the clear port automatically connects to GND.
<b>EDA Page</b>				
Simulation Libraries	—	—	—	Specifies the libraries needed for functional simulation. However, ALTTEMP_SENSE megafunciton does not have simulation model files and cannot be simulated.
Generate netlist	On/Off	—	—	Specifies whether to turn on the option to generate synthesis area and timing estimation netlist.
<b>Summary Page</b>	—	—	—	Specifies the types of files to be generated. A gray checkmark indicates a file that is automatically generated; a green checkmark indicates an optional file. Choose from the following types of files: <ul style="list-style-type: none"> <li>■ AHDL Include file (<i>&lt;function name&gt;.inc</i>)</li> <li>■ VHDL component declaration file (<i>&lt;function name&gt;.cmp</i>)</li> <li>■ Quartus II symbol file (<i>&lt;function name&gt;.bsf</i>)</li> <li>■ Instantiation template file (<i>&lt;function name&gt;_inst.v</i> or <i>&lt;function name&gt;_inst.vhd</i>)</li> <li>■ Verilog HDL block box file (<i>&lt;function name&gt;_bb.v</i>)</li> </ul> If <b>Generate netlist</b> option is turned on, the file for that netlist is also available ( <i>&lt;function name&gt;_syn.v</i> ).

This section describes the operation of the megafunction and the functionality of each port.

## Temperature Sensing Operation

Figure 3–1 shows the top-level ports and the basic building blocks of the ALTTEMP\_SENSE megafunction.

**Figure 3–1. Block Diagram of the ALTTEMP\_SENSE Megafunction**




The ALTTEMP\_SENSE megafunction runs at the frequency of the `clk` signal. The `clk` signal can run at a frequency of 80 MHz and below. The clock divider divides the `clk` signal to 1 MHz or less to feed the ADC. You can set the value of the clock divider using the ALTTEMP\_SENSE MegaWizard interface.

The `ce` signal connects to the output enable (`oe`) port of the clock divider block. Assert the `ce` signal to enable the ALTTEMP\_SENSE megafunction. When you deassert the `ce` signal, the megafunction disables the ADC, and maintains the previous values of the `tsdcalo[7:0]` and `tsdcaldone` signals unless you assert the `clr` signal, or reset the device. The `clr` signal is asynchronous, and you must assert the `clr` signal at least one clock cycle of the `adcclock` signal to clear the output ports.



When you choose not to create the `ce` port, the megafunction connects the `ce` port to VCC. In this case, the ADC circuitry is always enabled. Altera recommends that you disable the ADC by deasserting the `ce` signal when the ADC is not in use to reduce power consumption.

During device power-up or when you assert the asynchronous `clr` signal, the megafunction sets the `tsdcaldone` port to 0 and the `tsdcalo[7:0]` signal to 11010101 or 0xD5. After 10 clock cycles of the `adcclk` signal, the megafunction asserts the `tsdcaldone` signal to indicate that the temperature sensing operation is complete and that the value of the `tsdcalo[7:0]` signal is valid. The value of the `tsdcalo[7:0]` signal corresponds to the device temperature range shown in [Table 3-2 on page 3-3](#). To start another temperature sensing operation, assert the `clr` signal for at least one clock cycle of the `adcclk` signal, or reset the device.

 When you choose not to create the `clr` port, the megafunction connects the `clr` port to GND. In this case, you must reset the device to clear the output signals or start a temperature sensing operation. Altera recommends that you generate the `clr` port if you are planning to run the temperature sensing operation more than once.

## ALTTEMP\_SENSE Ports

This section describes the ports of the ALTTEMP\_SENSE megafunction.

[Table 3-1](#) lists the ALTTEMP\_SENSE megafunction input and output ports.

**Table 3-1. ALTTEMP\_SENSE Megafunction Input and Output Ports**

Port Name	Direction	Width (Bit)	Description
<code>clk</code>	Input	1	Input clock signal that runs at a frequency of 80 MHz and below. The internal clock divider reduces the frequency of the <code>clk</code> signal to 1 MHz or less before clocking the ADC.
<code>ce</code>	Input	1	The asynchronous clock enable signal for the <code>clk</code> signal. This signal turns on/off the ALTTEMP_SENSE megafunction that implements the TSD block. This is an active-high signal. By default, this port connects to VCC.
<code>clr</code>	Input	1	The asynchronous clear signal. When you assert the <code>clr</code> signal, the megafunction sets the <code>tsdcalo[7:0]</code> signal to 11010101 (0xD5) and the <code>tsdcaldone</code> signal to 0. This is an active-high signal. By default, this port connects to GND.
<code>tsdcalo[7:0]</code>	Output	8	8-bit output signal that contains the analog-to-digital-conversion temperature value. The 8-bit value maps to a unique temperature value. Refer to <a href="#">Table 3-2</a> for the <code>tsdcalo[7:0]</code> value that corresponds to the device temperature range. During device power-up or when you assert the <code>clr</code> signal, the megafunction sets the <code>tsdcalo[7:0]</code> to 11010101 (0xD5).
<code>tsdcaldone</code>	Output	1	This signal indicates the completion of the temperature sensing process. The megafunction asserts this signal when the process is complete. During device power-up or when you assert the <code>clr</code> signal, the megafunction sets the <code>tsdcaldone</code> to 0.

Table 3–2 shows the value of `tsdcalo[7:0]` that corresponds to the device temperature range. The temperature specification ranges from -70°C to 127°C.

**Table 3–2. The Mapping of `tsdcalo [7..0]` Value to Stratix IV Device Temperature**

Value of <code>tsdcalo[7:0]</code> in Hexadecimal	Temperature in Degree Celsius (°C)
FF	127
...	...
E4	100
...	...
D5	85
...	...
D0	80
...	...
B2	50
...	...
9E	30
...	...
8A	10
...	...
80	0
...	...
76	-10
...	...
6C	-20
...	...
62	-30
...	...
4E	-50
...	...
3A	-70°C

## Prototypes and Component Declarations

This section describes the prototypes and component declarations of the ALTTEMP\_SENSE megafunction. These ports and parameters are available to customize the ALTTEMP\_SENSE megafunction according to your application.

### Verilog HDL Prototype

The following Verilog HDL prototype is located in the Verilog Design File (.v) `altera_mf.v` in the `<Quartus II installation directory>\eda\synthesis` directory.

```
module alttemp_sense
#( parameter clk_frequency = "unused",
  parameter clock_divider_enable = "off",
  parameter clock_divider_value = 40,
  parameter intended_device_family = "unused",
  parameter number_of_samples = 128,
  parameter poi_cal_temperature = 85,
  parameter sim_tsd_cal = 0,
  parameter use_wys = "on",
  parameter user_offset_enable = "off",
  parameter lpm_type = "alttemp_sense",
  parameter lpm_hint = "unused" )
( input wire aclr,
  input wire ce,
  input wire clk,
  input wire clr,
  input wire compouttest,
  input wire fdbkctrlfromcore,
  input wire [5:0] offset,
  output wire [5:0] offsetout,
  input wire [7:0] testin,
  output wire [7:0] tsd_avg,
  output wire tsd_busy,
  input wire tsd_trig,
  output wire tsd_caldone,
  output wire [7:0] tsd_cal,
  output wire tsd_compout) /* synthesis syn_black_box=1 */;

endmodule //alttemp_sense
```

## VHDL Component Declaration

The following VHDL component declaration is located in the VHDL Design File (.vhd) `altera_mf_components.vhd` in the `<Quartus II installation directory>\libraries\vhdl\altera_mf` directory.

```

component alttemp_sense
  generic (
    clk_frequency:string;
    clock_divider_enable:string := "off";
    clock_divider_value:natural := 40;
    intended_device_family:string := "unused";
    number_of_samples:natural := 128;
    poi_cal_temperature:natural := 85;
    sim_tsdcalo:natural := 0;
    use_wys:string := "on";
    user_offset_enable:string := "off";
    lpm_hint:string := "UNUSED";
    lpm_type:string := "alttemp_sense"
  );
  port(
    aclr: in std_logic := '0';
    ce : in std_logic := '1';
    clk: in std_logic;
    clr: in std_logic := '0';
    compouttest:in std_logic := '0';
    fdbkctrlfromcore:in std_logic := '0';
    offset:in std_logic_vector(5 downto 0) := (others => '0');
    offsetout:out std_logic_vector(5 downto 0);
    testin:in std_logic_vector(7 downto 0) := (others => '0');
    tsd_avg:out std_logic_vector(7 downto 0);
    tsd_busy:out std_logic;
    tsd_trig:in std_logic := '0';
    tsdcaldone:out std_logic;
    tsdcalo:out std_logic_vector(7 downto 0);
    tsdcompout:out std_logic
  );
end component;

```

This section describes the design example provided with this megafunction. You can download design examples for this megafunction from the following locations:

- On the [Quartus II Development Software Literature](#) page, in the **Using Megafunctions** section under **I/O**
- On the [Literature: User Guides](#) webpage, with this user guide

Simulate the designs using the ModelSim<sup>®</sup>-Altera software version 6.5e to generate a waveform display of the device behavior. For more information about the ModelSim-Altera software, refer to the [ModelSim-Altera Software Support](#) page on the Altera website. The support page includes links to such topics as installation, usage, and troubleshooting.

## Temperature Sensing Operation in Stratix IV Device

This design example uses the ALTTEMP\_SENSE megafunction to perform temperature measurement in a Stratix IV device (EP4SGX180DF29C3). This design example demonstrates temperature measurement with the following specifications:

- Set the input clock signal of the ALTTEMP\_SENSE megafunction to 40 MHz
- Clock the ADC with a 500 kHz signal
- Enable the asynchronous clear signal to reset the ALTTEMP\_SENSE megafunction
- Enable or disable the clock enable signal to turn on/off the ALTTEMP\_SENSE megafunction

### Generating the Megafunction

To generate the ALTTEMP\_SENSE megafunction, follow these steps:

1. Open the **alttemp\_sense\_ex1.zip** file and extract **alttemp\_sense\_ex1.qar**.
2. In the Quartus II software, open the **alttemp\_sense\_ex1.qar** file and restore the archive file into your working directory.
3. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 of the MegaWizard Plug-In Manager appears.
4. Select **Create a new custom megafunction variation**.
5. Click **Next**. Page 2a of the MegaWizard Plug-In Manager appears.

6. In the MegaWizard Plug-In Manager pages, select or verify the configuration settings shown in Table 4-1. Click **Next** to advance from one page to the next.

**Table 4-1. Configuration Settings for the ALTTEMP\_SENSE Megafunction**

MegaWizard Plug-In Manager Page	Option	Value
2a	Megafunction	Under the I/O category, select <b>ALTTEMP_SENSE</b>
	Which device family will you be using?	<b>Stratix IV</b>
	Which type of output file do you want to create?	<b>Verilog HDL</b>
	What name do you want for the output file?	<b>tsd_s4</b>
	Return to this page for another create operation	Turned off
General Options	Currently selected device family	<b>Stratix IV</b>
	Match project/default	Turned on
	What is the input frequency?	<b>40 MHz</b>
	What is the clock divider value?	<b>80 MHz</b>
	Create a clock enable port	Turned on
	Create an asynchronous clear port	Turned on
EDA	Generate netlist	Turned off
Summary	Variation file (.v)	Turned on
	Quartus II IP file (.qip)	Turned on
	Quartus II symbol file (.bsf)	Turned on
	Instantiation template file (.v)	Turned on
	AHDL Include file (.inc)	Turned on
	VHDL component declaration file (.cmp)	Turned on

7. Click **Finish**. The `tsd_s4` module is built.

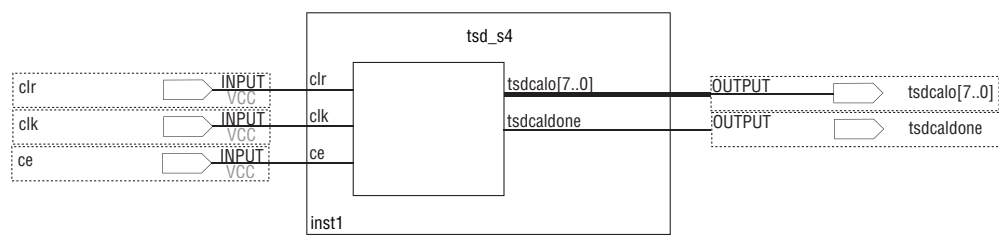
## Compiling the Megafunction

To compile the megafunction in the Quartus II software, follow these steps:

1. Open the top-level file **alttemp\_sense\_ex1.bdf** in the Quartus II Block Editor software. This file contains the input and output assignments and a placeholder for the `tsd_s4` module.
2. To insert the `tsd_s4` module, double-click on the Block Editor window. The Symbol window appears.
3. Under **Name**, browse to the **tsd\_s4.bsf** file.
4. Click **OK**.
5. Place the `tsd_s4` module onto the **INSERT TSD\_S4 BLOCK HERE** placeholder so that the module aligns with the input and output ports.

Figure 4-1 shows the complete design file.

**Figure 4-1. Complete Design File**



6. On the Processing menu, click **Start Compilation**.
7. When the **Full Compilation was successful** message box appears, click **OK**.

## Using Clear Box Generator

You can use clear box generator, a command-line executable, to configure parameters that are in the ALTTEMP\_SENSE MegaWizard interface. The clear box generator creates or modifies custom megafunction variations, which you can instantiate in a design file. The clear box generator generates megafunction variation file in Verilog HDL or VHDL format.


To generate the ALTTEMP\_SENSE megafunction using the clear box generator, perform the following steps:

1. Create a text file (.txt) that contains your clear box ports and parameter settings in your working directory.

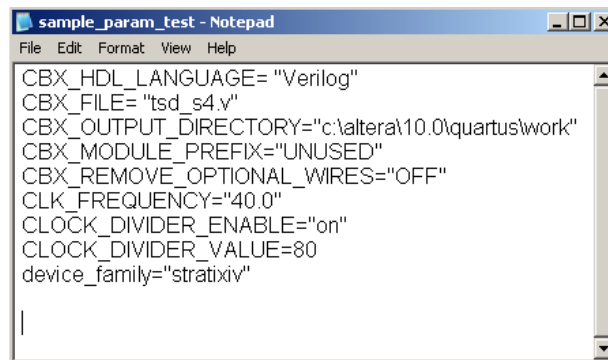
For example,

c:\altera\10.0\quartus\work\sample\_param\_test.txt.

Figure A-1 shows a sample text file to generate the ALTTEMP\_SENSE megafunction.

 Ensure that you enclose String-type values with double-quotes.


**Figure A-1. Sample Text File for Clear Box Generator**



2. Access the command prompt of your operating system, and change the current directory to your working directory by typing the following command:

```
cd c:\altera\10.0\quartus\work\
```

The clear box executable file name is **clearbox.exe**.

 When you install the Quartus II software, the %QUARTUS\_ROOTDIR%\bin is added into your system's environment variables. Therefore, you can run the clear box command from any directory.

- To view the available ports and parameters for this megafunction, type the following command at the command prompt of your operating system:

```
clearbox alttemp_sense -h
```

- To generate the ALTTEMP\_SENSE megafunction variation file based on the ports and parameter settings in the text file, type the following command:

```
clearbox alttemp_sense -f *.txt
```

For example, `clearbox alttemp_sense -f sample_param_test.txt`


- After the clear box generator generates the megafunction variation files, you can instantiate the megafunction module in a HDL file or a block diagram file in the Quartus II software.


- To view the estimated hardware resources that the ALTTEMP\_SENSE megafunction uses, type the following command:

```
clearbox alttemp_sense -f sample_param_test.txt -resc_count
```



This command does not generate a HDL file.

 For more information about the clear box parameters, refer to “[Parameter Settings](#)” on [page 2-1](#).

 For more information about the ports, refer to “[ALTTEMP\\_SENSE Ports](#)” on [page 3-2](#).

## Document Revision History

[Table A-1](#) displays the revision history for this user guide.

**Table A-1. Document Revision History**

Date	Document Version	Changes Made
September 2010	3.0	<ul style="list-style-type: none"> <li>■ Updated the <a href="#">Parameter Settings</a> chapter.</li> <li>■ Added the <a href="#">Prototypes and Component Declarations</a> section.</li> <li>■ Added the <a href="#">Clear Box Generator</a> chapter.</li> </ul>
February 2010	2.0	Updated the <a href="#">Temperature Sensing Operation</a> section.
November 2009	1.0	Initial release.