Technical Brief

OpenCore Stamping and Benchmarking Methodology

FPGA Selection for Benchmarking

In the OpenCore benchmarks, the largest comparable parts from Altera and Xilinx were selected. Table 1 shows the device and speed grade used for benchmarking on the latest available software.

Table 1. Device and Speed Grade

FPGA	Altera	Xilinx
Device	EP3S340-3*(1)*	XC5VLX330-2*(1)*
Speed Grade	Medium*(2)*	Medium*(2)*

Note:
(1) Similar results are seen on smaller parts.
(2) The medium speed grades are the fastest available in software.

Stamping Methodology

To simulate the impact of design size on FPGA performance, utilization, and compile times, multiple instances of a particular OpenCore were instantiated in the core of the FPGAs. The selection process of the OpenCore was based on density and popularity (defined by OpenCores.org).

At the time of the benchmarks, the seven largest OpenCores on www.OpenCores.org in terms of logic elements (LEs) were selected, as shown in Table 2.

Table 2. OpenCores.org Largest Cores

OpenCores	LEs	ALMs
oc_aquarius	6475	2590
oc_des_des3perf	15670	6268
oc_ethernet	3548	1419
oc_oc8051	4115	1646
oc_or1k	7028	2811
oc_pc1	3630	1452
oc_usb_funct	4318	1727

To increase the design size in the FPGA, as shown in Figure 1, each OpenCore design was repeatedly instantiated (stamping the same core) in the FPGA such that:

- Each stamp was implemented in parallel.
- I/O wrapper logic was added to reduce the number of I/O pins required for the larger design.
- No timing critical paths between the cores and the wrapper logic existed.
- The wrapper logic provided very little overhead.

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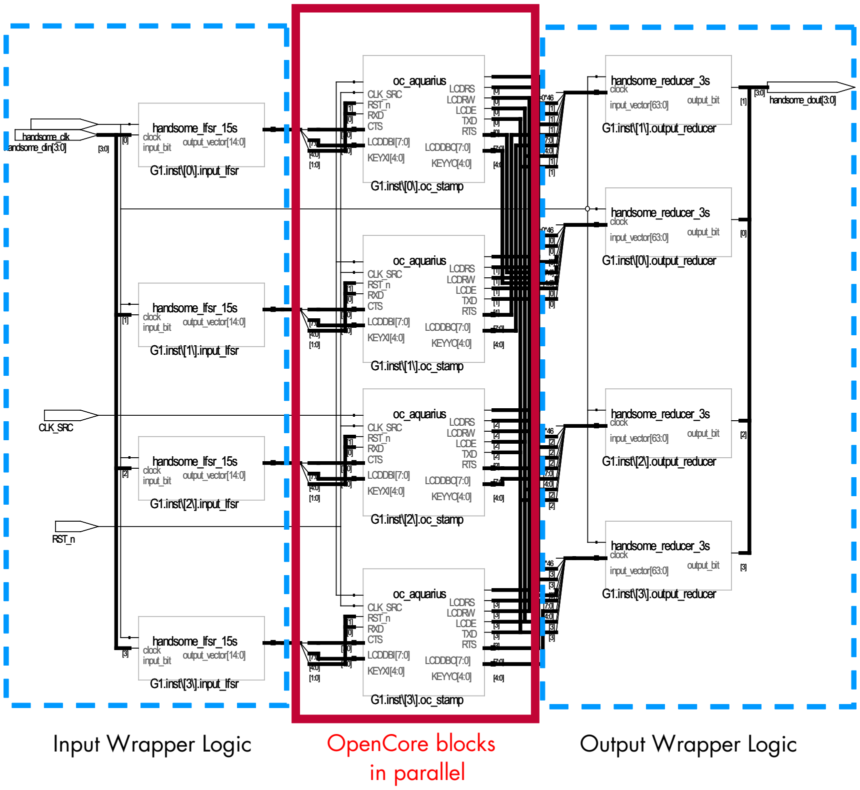
Figure 1. The oc_aquarius design instantiated four times in the FPGA



As the number of instantiations of the OpenCore design increases (and thus design size increases), resources such as I/O pins and global clocks become limited.

- To avoid running out of pins, each OpenCore was wrapped in a shift register, such that one physical pin would feed all input pins of a core and all output pins of a core would feed into a loadable shift register. The input and output shift registers are shown in Figure 2 and Figure 3. The shift register size is dependent on the number of I/Os, and the number of shift registers is dependant on the number of OpenCores implemented in the FPGA.

Figure 2. Input shift register implementation

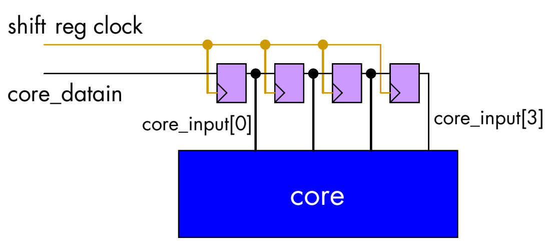
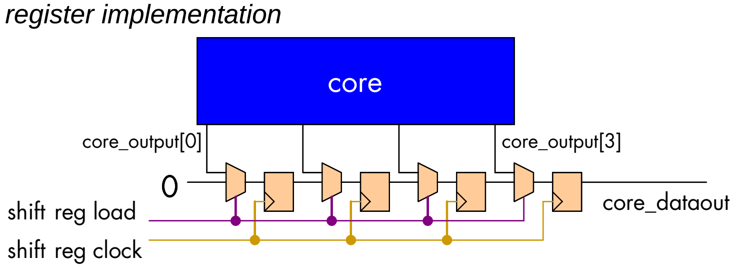
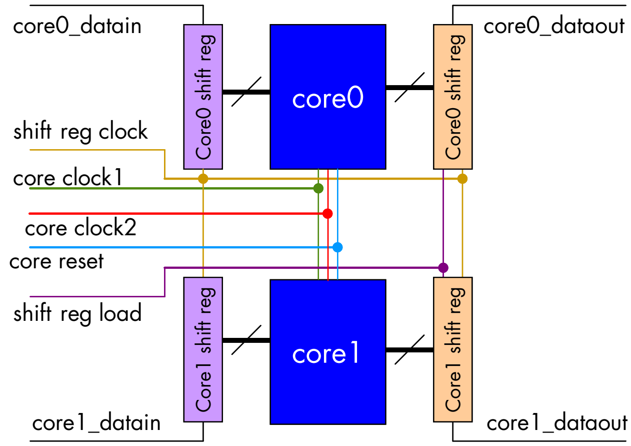


Figure 3. Output shift register implementation



- To avoid running out of global clock resources, the global clock and reset signals for all OpenCores were directly fed by a pin. For example, if a core requires two clocks (core clock 1 and core clock 2) and one reset signal, then all instances of core clock 1 are fed by one pin, all instances of core clock 2 are fed by a different pin and finally all instances of the reset signal are fed by a third pin. This way all OpenCores were fed by the same clock and reset signals (see Figure 4).

Figure 4. Two-core implementation with shared clock and reset signals



Once the wrapper logic tied up all the OpenCores in the in the FPGA, the next step was to ensure that no critical paths existed between the wrapper logic (shift registers) and OpenCore. To achieve this, false paths were created and, by making the core clock(s) and wrapper logic clock on different unrelated clock domains, no timing paths existed. The cores were available to be optimized separately from the shift registers by the CAD tools.

The OpenCores were instantiated as many times as the device and software would allow such that there were no compilation errors. The performance, utilization and compile times were then compared for each FPGA.

Performance Benchmarking Methodology

Altera has a third-party, industry-expert-endorsed performance benchmarking methodology, which is used to compare FPGA performance between families from a single FPGA vendor and with those of competitive solutions. This ensures a consistent benchmarking environment when testing Altera® FPGAs and when comparing them to competitor FPGAs.

Further Information

- *Altera's FPGA Performance Benchmarking Methodology*:
  www.altera.com/literature/wp/wpfpgapbm.pdf
- *Guidance for Accurately Benchmarking FPGAs:*
  www.altera.com/literature/wp/wp-01040.pdf
- OpenCores.org:
  www.opencores.org
- OpenCore Designs Validate—Stratix III FPGA Advantages Increase with Design Size:
  www.altera.com/products/devices/stratix3/overview/architecture/performance/st3-opencores.html.

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