

FPGA Features: New Devices

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		Stratix II (1.2 V) High Density, High Performance						Cyclone II (1.2 V) Low Cost, High Volume					
		EP2K15	EP2K30	EP2K60	EP2K90	EP2K130	EP2K180	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Density & Speed	Adaptive Logic Modules (ALMs)	6,240	13,552	24,176	36,384	53,016	71,760	—	—	—	—	—	—
	Adaptive Look-Up Tables (ALUTs)	12,480	27,104	48,352	72,768	106,032	143,520	—	—	—	—	—	—
	Logic Elements (LEs) ¹	15,600	33,880	60,440	90,960	132,540	179,400	4,608	8,256	18,752	33,216	50,528	68,416
	Total RAM Bits (K) ²	419	1,370	2,544	4,520	6,748	9,383	120	166	240	484	594	1,152
	M512 RAM Blocks (512 bits + 64 parity bits)	104	202	329	488	699	930	—	—	—	—	—	—
	M4K RAM Blocks (4 Kbits + 512 parity bits) ³	78	144	255	408	609	768	26	36	52	105	129	250
	M-RAM Blocks (512 Kbits + 65,536 parity bits) ³	0	1	2	4	6	9	—	—	—	—	—	—
	Speed Grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-4, -5	-4, -5	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8
Architectural Features & Other	Available Embedded Processor	Nios® II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II
	DSP Blocks	12	16	36	48	63	96	—	—	—	—	—	—
	18x18-bit/9x9-bit Embedded Multipliers	48 / 96	64 / 128	144 / 288	192 / 384	252 / 504	384 / 768	13 / 26	18 / 36	26 / 52	35 / 70	86 / 172	150 / 300
	I/O Registers per I/O Element	6	6	6	6	6	6	3	3	3	3	3	3
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	48	48	48	48	48	48	8	8	16	16	16	16
	Phase-Locked Loops (PLLs)/Unique Outputs	6 / 28	6 / 28	12 / 56	12 / 56	12 / 56	12 / 56	2 / 6	2 / 6	4 / 12	4 / 12	4 / 12	4 / 12
	Design Security ⁴	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy™ Devices Support	—	✓	✓	✓	✓	✓	—	—	—	—	—	—
	Industrial & Lead-Free Device Support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Configuration Devices	Configuration File Size (Mbits)	5.0	10.1	17.1	27.5	39.6	52.4	1.23	1.99	3.93	7.07	9.13	10.25
	Number of EPCS1 Devices (1 Mbit)	—	—	—	—	—	—	1	—	—	—	—	—
	Number of EPCS4 Devices (4 Mbits)	1	—	—	—	—	—	1	1	1	—	—	—
	Number of EPCS16 Devices (16 Mbits)	1	1	1	—	—	—	1	1	1	1	1	1
	Number of EPCS64 Devices (64 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1
	Number of EPC2 Devices (1.6 Mbits)	2	4	7	11	16	21	1	1	2	4	5	7
	Number of EPC4 Devices (4 Mbits)	1	—	—	—	—	—	1	1	1	—	—	—
	Number of EPC8 Devices (8 Mbits)	1	1	—	—	—	—	1	1	1	1	1	—
Number of EPC16 Devices (16 Mbits)	1	1	1	—	—	—	1	1	1	1	1	1	
I/O Features	I/O Voltage Levels Supported	1.5V, 1.8V, 2.5V, 3.3V						1.5V, 1.8V, 2.5V, 3.3V					
	I/O Standards	LVDS, LVPECL, HyperTransport, Differential SSTL-18 (I & II), Differential SSTL-2 (I & II), 1.5-V Differential HSTL (I & II), 1.8-V Differential HSTL (I & II), SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTTL, LVCMOS						LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I & II), Differential SSTL-2 (I & II), 1.5-V Differential HSTL (I & II), 1.8-V Differential HSTL (I & II), SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTTL, LVCMOS					
	External Memory Device Interfaces	QDRII, DDR2, RDRAM II, DDR, SDR						QDRII, DDR2, DDR, SDR					
	True-LVDS™ Maximum Data Rate (Mbps)	1,000	1,000	1,000	1,000	1,000	1,000	—	—	—	—	—	—
	True-LVDS Channels (Receive/Transmit)	42 / 38	62 / 58	84 / 84	118 / 118	156 / 156	156 / 156	—	—	—	—	—	—
	Medium-Speed LVDS Data Rate (Mbps) (Receive/Transmit)	—	—	—	—	—	—	805 / 622	805 / 622	805 / 622	805 / 622	805 / 622	805 / 622
	Medium-Speed LVDS Channels	—	—	—	—	—	—	60	79	136	209	197	265
	RSDS Maximum Data Rate (Mbps) (Transmit)	—	—	—	—	—	—	170	170	170	170	170	170
	Mini-LVDS Maximum Data Rate (Mbps) (Transmit)	—	—	—	—	—	—	170	170	170	170	170	170
	Embedded Dynamic Phase Alignment (DPA) Circuitry	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—
	Series On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—
Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Notes: ¹For Stratix II, the values represent the number of equivalent logic elements (1 ALM = 2.5 LEs); ²K=1,000; ³Kbit=1,024 bits; ⁴Design Security for Cyclone II available with MAX® II handshaking solution

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FPGA Package & I/O Matrix: New Devices



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- Device Available Now in Commercial (0 to 85° C) & Industrial (-40 to 100° C) Temperatures.
- Device Available Now in Commercial Temperature; Contact Altera for Industrial Temperature
- ↔ Vertical Migration (Same VCC, GND, ISP & Input Pins)

	Stratix II (1.2 V) High Density, High Performance						Cyclone II (1.2 V) Low Cost, High Volume					
	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Thin Quad Flat Pack (T)	144-Pin TQFP						89 → 85					
Plastic Quad Flat Pack (Q)	208-Pin PQFP						142 → 138 → (2)					
FineLine BGA (F)	256-Pin FBGA						(2) → 182 → 152					
	484-Pin FBGA (Wirebond)						← 315 → 322 → 294					
	484-Pin FBGA (FlipChip)						← 342 → 342 → 334					
	672-Pin FBGA (Wirebond)						← 475 → 450 → 422					
	672-Pin FBGA (FlipChip)						← 366 → 500 → 492					
	780-Pin FBGA						← 534 ⁽¹⁾ → 534 ⁽¹⁾					
	896-Pin FBGA											
	1,020-Pin FBGA						← 718 → 758 → 742 → 742					
Hybrid FineLine BGA (H)	1,508-Pin FBGA						← 902 → 1,126 → 1,170					
	484-Pin HFBGA						308 ⁽¹⁾					

Notes: ⁽¹⁾User I/O counts are preliminary and subject to change. ⁽²⁾Contact your local sales representative for device information.

Package Statistics	TQFP	PQFP	FBGA						HFBGA			
Number of Pins	144	208	256	484	484	672	672	780	896	1,020	1,508	484
Package Technology	Wirebond	Wirebond	Wirebond	Wirebond	FlipChip	Wirebond	FlipChip	FlipChip	Wirebond	FlipChip	FlipChip	FlipChip
Nominal Length x Width (mm)	22 x 22	30.6 x 30.6	17 x 17	23 x 23	23 x 23	27 x 27	27 x 27	29 x 29	31 x 31	33 x 33	40 x 40	27 x 27
Maximum Surface Area (mm ²)	493	952	296	538	538	740	740	853	974	1,102	1,616	740
Maximum Height (mm)	1.60	4.10	1.55	2.60	3.50	2.60	3.50	3.50	2.60	3.50	3.50	3.50
Nominal Lead Pitch (mm)	0.50	0.50	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Maximum Lead Width (mm)	0.27	0.27	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70

	Configuration Devices							
	EPC2	EPC4	EPC8	EPC16	EPC31	EPC64	EPC16	EPC64
8-Pin SOIC					✓	✓		
16-Pin SOIC							✓	✓
20-Pin PLCC	✓							
32-Pin TQFP	✓							
88-Pin UBGA*				✓				
100-Pin PQFP		✓	✓	✓				
Reprogrammable	✓	✓	✓	✓	✓	✓	✓	✓
Data Compression	✓	✓	✓	✓	✓	✓	✓	✓
Page Mode		✓	✓	✓				

*UBGA: Ultra FineLine BGA