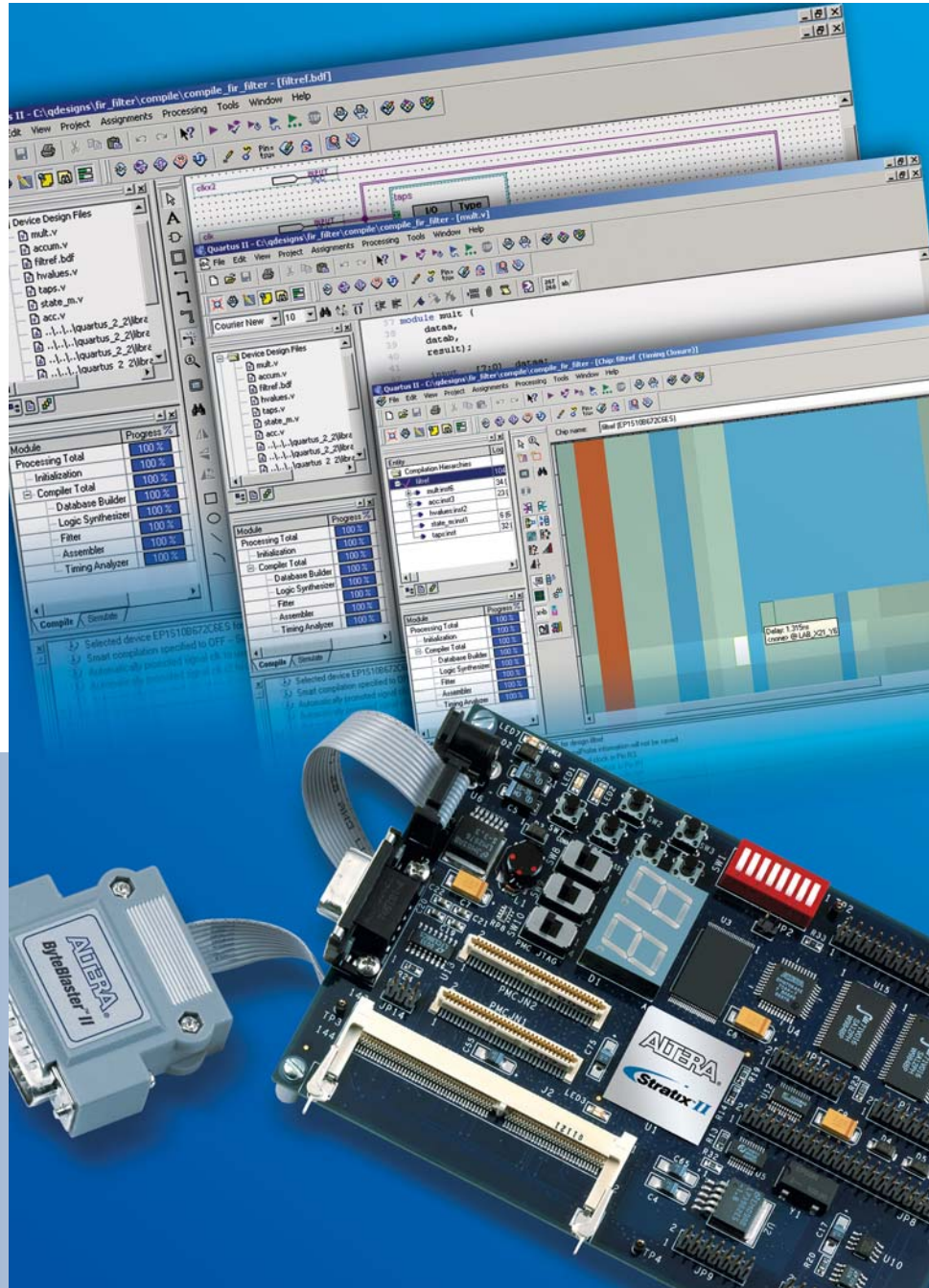




Design Software & Development Kit Selector Guide



April 2004

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Quartus II Design Software Leadership



QUARTUS® II

Altera's Quartus® II software leads the industry as the most comprehensive environment available for FPGA, CPLD, and structured ASIC designs, delivering unmatched performance, efficiency, and ease-of-use. The Quartus II software now features unique advantages in design flow methodology, system design, timing-closure methodology, in-system verification technology, and third-party EDA support.

Design Flow Methodology

Advantages of the Quartus II software's powerful, yet easy-to-use design flow include:

Up Front I/O Assignment & Validation: Accelerates design productivity, time-to-market, and ease of use by performing I/O assignment and validation up front (even before design modules are available), so printed circuit board (PCB) layout can begin earlier in the design process.

LogicLock Block-Based Design: Shortens and simplifies design and verification cycles with the LogicLock™ block-based design flow, the easiest and most flexible methodology for building and integrating systems block by block. The LogicLock methodology provides unrivaled support for team-based design.

Memory Compiler: Graphically supports “what-if” analysis by dynamically producing waveform displays of memory structure operation based on user parameterization.

Scripting Support: Allows both graphical user interface (GUI)-based and scripting-based design techniques. The Quartus II software is the only FPGA and structured ASIC implementation tool from a programmable logic device (PLD) vendor that supports an industry-standard tool command language (Tcl) scripting interface.

System Design Technology

Altera's Quartus II software is the industry's only design environment that supports Intellectual Property (IP)-based system design—including complete and automated system definition and implementation—without requiring lower-level hardware description language (HDL) or schematics. This capability enables designers to turn their concepts into working systems in minutes. The Quartus II system design tools include:

SOPC Builder: A system development tool that automates adding, parameterizing, and linking IP cores—including embedded processors, co-processors, peripherals, memories, and user-defined logic—without requiring lower-level HDL or schematics. (See Figure 1.)

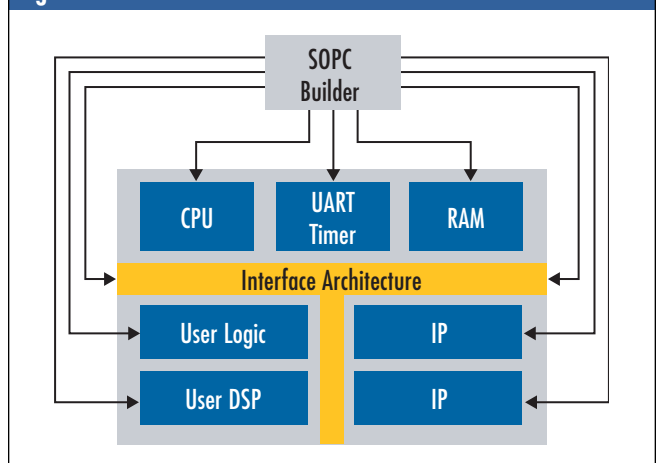
DSP Builder: Shortens digital signal processing (DSP) design cycles by helping designers create the hardware representation of a DSP design in an algorithm-friendly development environment. (Read more about DSP Builder on page 4.)

Off-the-Shelf IP Cores: The popular Nios® embedded processor and parameterized IP blocks from Altera and Altera Megafunction Partners Program (AMPPSM) partners have been rigorously tested and optimized for the highest performance in Altera® devices.

Timing-Closure Methodology

Empowered with industry-leading timing-closure methodologies, the Quartus II software delivers unmatched capability for designers to satisfy design timing requirements faster. Altera is the first programmable logic supplier to develop and deliver a comprehensive set of timing-closure methodologies as an integrated part of its existing tools suite at no additional cost.

Figure 1. SOPC Builder



Floorplan Editor: Improves analysis of timing data in the floorplan.

Chip Editor: Reduces verification time (while maintaining timing closure) by enabling small, post place-and-route design changes to be implemented in minutes.

Registered Transfer Level (RTL) Viewer: Provides a schematic representation of designs that can be used to analyze a design's structure before further behavioral simulation, synthesis, and place-and-route steps are performed.

Design Space Explorer Script: Increases performance and saves engineering time by automatically seeking out optimum performance by applying combinations of Quartus II software settings. Also supports distributed environments where multiple computers can run simultaneous compilations using different optimization settings.

Incremental Fitting Technology: Reduces compile times (while maintaining timing closure) when implementing small HDL changes by performing an incremental fitting on the new or changed logic.

Additionally, advancements to the core place-and-route technology in the Quartus II software version 4.0 deliver 50% better f_{MAX} and 20% faster compile times, when targeting Stratix™ II FPGAs, and up to 50% faster compile times, for all PLD families when using the new auto fit feature.

Third-Party EDA Support Leadership

Altera and its EDA partners collaborate to deliver seamless integration between the Quartus II software and third-party EDA software for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

Verification Solution

In addition to integrating with all of the leading third-party EDA verification tools and methodologies, the Quartus II software also provides:

- Advanced multi-clock timing-analysis capabilities
- Integrated power analysis
- The chip editor tool to implement design changes in-system in just minutes

Altera Design Software Subscription Program

Participation in the Altera Design Software Subscription Program provides complete access to Altera design software and updates for one year, and includes the following software products:

- Altera's Quartus II design software
- SOPC Builder automated system generation tool
- Model Technology™ ModelSim®-Altera simulation software

Descriptions of each software product included in Altera software subscriptions appear throughout this selector guide.

Active subscribers will be able to perform the following:

- System-level design leveraging FPGAs, CPLDs, and structured ASICs
- Embedded software development
- Synthesis
- Place-and-route
- Verification
- Device programming

If your subscription expires, your current Altera software will continue to work, but you will not receive the updates and new features offered in subsequent software releases. You can further enhance the value of your software subscription by purchasing an Altera development kit (page 10), adding the Altera DSP Builder system-level design software, or purchasing IP from Altera or an AMPP partner.

- SignalProbe™ routing to incrementally route an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer.
- The SignalTap® II embedded logic analyzer that supports the most channels, fastest clock speeds, and the largest sample depths available. It also features the most advanced triggering capabilities available in an FPGA-embedded logic analyzer

Support for Embedded Processor Designs

Nios® Altera's embedded processor solutions integrate hard and soft embedded processors, on-chip or off-chip memory, peripherals, and programmable logic on a single device. Altera's easy-to-use Nios processor sets the standard for soft embedded processors and has thousands of active customers worldwide. Altera is the first company to offer embedded processor development and debugging tools as well as programmable logic development in a single integrated environment.

DSP Builder

DSP Builder shortens DSP design cycles by helping to create a hardware representation of a DSP design in an algorithm-friendly development environment. Existing MATLAB functions and Simulink blocks can be combined with Altera DSP Builder blocks and Altera IP MegaCore® functions to link system-level design and implementation with

DSP algorithm development. DSP Builder allows system, algorithm, and hardware designers to share a common development platform.

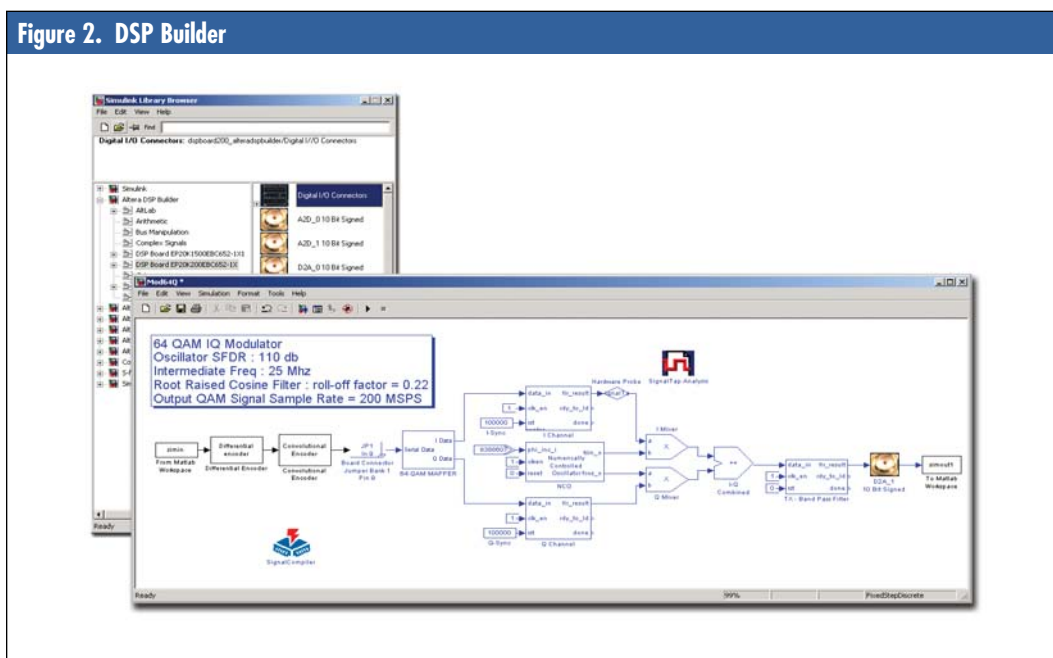
DSP system design in Altera FPGAs requires both high-level algorithms and HDL development tools. The Altera DSP Builder (see Figure 2) integrates these tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with synthesis, simulation, and Altera design software.

Free Web-Edition Design Software

You can download and license the Quartus II Web Edition software free of charge from the Altera web site. The Quartus II Web Edition software is a subset of the Quartus II software that supports devices from the MAX® II, Cyclone™, Stratix II, Stratix, Excalibur™, APEX™ II, APEX 20KE, FLEX 10K®, FLEX® 10KE, FLEX 10KA, ACEX®, FLEX 6000, MAX 7000S, MAX 7000B, MAX 7000AE, and MAX 3000A device families.

MAX+PLUS II Design Software

Altera recommends the Quartus II software or Quartus II Web Edition software for all new design starts. For legacy designs, the MAX+PLUS® II software is available on request to Altera subscription customers. The MAX+PLUS II BASELINE software is a subset of the MAX+PLUS II software and is available free from the Altera web site.



Selecting a Design Software Product

Altera subscription products are based on the operating system, network environment, and number of enabled users. Select the subscription product that best suits your needs from Table 1.

Altera Device Support

The Quartus II design software supports all of Altera's latest FPGA, CPLD, and structured ASIC device families, as shown in Table 2. The Quartus II Web Edition software supports the low- to mid-density devices listed in Table 2.

Platform Support	Benefit	Ordering Code
PC	Stand-alone, single-user	FIXEDPC
PC	Multiple-user network license (one concurrent user)	FLOATPC
PC, Solaris, HP-UX	Multiple-user network license (one concurrent user)	FLOATNET
PC, Red Hat Linux	Multiple-user network license (one concurrent user)	FLOATLNX
PC	Add additional concurrent PC users	ADD-FLOATPC
PC, Solaris, HP-UX	Add additional concurrent PC, Solaris, or HP-UX users	ADD-FLOATNET
PC, Red Hat Linux	Add additional PC or Red Hat Linux concurrent users	ADD-FLOATLNX
Same as original subscription	One-year extension for FIXEDPC, FLOATPC, FLOATNET, FLOATLNX, ADD-FLOATPC, ADD-FLOATNET licenses	RENEWAL

Note: ¹ Purchase one FLOATPC, FLOATNET, FLOATLNX, or ADD-FLOATLNX product and purchase ADD-FLOATPC, ADD-FLOATNET, or ADD-FLOATLNX products to add support for additional concurrent users on the same network.

Device	Quartus II	Quartus II Web Edition
Stratix II (All)	✓	
Stratix II EP2S15	✓	✓
Stratix (All)	✓	
Stratix EP1S10	✓	✓
Stratix GX (All) ¹	✓	
Cyclone (All)	✓	✓
HardCopy™ (All)	✓	
APEX II (All)	✓	
APEX II EP2A15	✓	✓
APEX 20K (All)	✓	
APEX EP20K30E, EP20K60E, EP20K160E, EP20K200C	✓	✓
Mercury™ (All)	✓	
FLEX 10K (All), FLEX 10KA (All)	✓	✓
FLEX EPF10K30E, EPF10K50S, EPK10K100E, EPF10K130E, EPF10K200S	✓	✓
Excalibur (All)	✓	
Excalibur EPXA1	✓	✓
ACEX (All)	✓	✓
FLEX 6000 (All)	✓	✓
MAX II (All)	✓	✓
MAX 3000A (All)	✓	✓
MAX 7000S, MAX 7000B, MAX 7000AE	✓	✓

Note: ¹ Contact your local Altera sales office to enable Stratix GX support.

Altera Design Software Features

Table 3 describes each design software feature and shows which design tool supports it.

Table 3. Software Feature Comparisons (Part 1 of 2)				
	Feature	Description	Quartus II	Quartus II Web Edition
System Level Design	SOPC Builder Support	Automates system definition and development. SOPC Builder is now installed by default with the Quartus II software.	✓	✓
	DSP Builder Support	Provides interface between the Altera design software and The Mathworks MATLAB and Simulink tools for DSP designers. DSP Builder is available from Altera.	✓	✓
Embedded Software	Embedded Software Integration	Integrates embedded software C/C++ development tools and debuggers for Altera embedded processor solutions.	✓	✓
FPGA Design	LogicLock Block-Based Design Methodology	Enables users to design and implement design modules independently and maintain performance while integrating modules into a top-level project. The LogicLock flow shortens design and verification cycles because each module is optimized only once.	✓	
	HardCopy Migration	Allows you to design directly for HardCopy devices. Includes device performance and power consumption estimates.	✓	
	RTL Viewer	Provides a schematic representation of designs that can be used to analyze a design's structure before further behavioral simulation, synthesis, and place-and-route steps are performed.	✓	
	Advanced Command Line Operation Feature Set	Includes independent synthesis, place-and-route, timing analysis, programming, and other functional modules that you can run from the command line or make files to easily customize design flows.	✓	✓
	Tcl Scripting and Synopsys Design Constraints (SDC) Support	Allows design flow automation and the ability to make device assignments using industry-standard Tcl scripts and SDC.	✓	✓
	NativeLink® Integration	Offers seamless interface for passing information and design processing between the Quartus II software and third-party EDA software.	✓	✓
	Text-Based Design Entry	Provides colored, syntax-sensitive editors for VHDL, Verilog HDL, and Altera Hardware Description Language (AHDL) development.	✓	✓
	Schematic Design Entry	Allows you to use basic graphical building blocks for creating a design.	✓	✓
	Block Design Entry	Allows you to edit design information in graphical format and automatically convert to a VHDL or Verilog file for synthesis and simulation using industry-standard tools.	✓	✓
	Library of Parameterized Modules (LPM)	Offers parameterized functions that can be used as building blocks to simplify design entry and increase performance.	✓	✓
	MegaWizard® Plug-In Manager	Provides graphical-driven tools that can be used stand-alone or within the design software to parameterize and instantiate LPM, MegaCore, and AMPP partners megafunctions.	✓	✓
	MegaCore Function Support	Offers pre-verified HDL design files for complex, system-level functions optimized for Altera device architectures.	✓	✓
Synthesis	VHDL and Verilog Synthesis	Provides Integrated VHDL and Verilog HDL synthesis.	✓	✓
	Third-Party Synthesis Support	Includes integration to third-party synthesis software from Mentor Graphics®, Synopsys, and Synplicity.	✓	✓

Table 3. Software Feature Comparisons (Part 2 of 2)

	Feature	Description	Quartus II	Quartus II Web Edition
Place-&-Route	PowerFit™ Place-and-Route	Uses your timing constraints to optimally place-and-route a design to satisfy all timing requirements.	✓	✓
	Fast Fit and Auto Fit	Reduce compile times up to 50%.	✓	✓
	Timing Closure Floorplan Editor	Displays physical timing estimates between nodes, LogicLock region connectivity in real time, displays routing congestion, and includes a graphical method for assigning logic cells and pins.	✓	✓
	Physical Synthesis	Applies re-synthesis optimizations, gate-level register re-timing, and register duplication to improve push-button performance results.	✓	
	Design Space Explorer	Increases average design performance by automatically applying combinations of netlist optimizations and advanced Quartus II software compiler settings. Supports simultaneous compilations on multiple computers.	✓	
	Chip Editor	Enables designers to view the internal structure of Altera devices and incrementally edit logic element (LE) and I/O cell configuration after place-and-route has already been performed.	✓	✓
	Incremental Fitting	Limits logic placement during the place-and-route process to new or changed logic in VHDL or Verilog source files. Accelerates compile times 40% on average while improving timing closure.	✓	✓
Verification	OpenCore® Evaluation	Enables you to compile and simulate MegaCore and AMPP parameterized functions before licensing the function.	✓	✓
	Static Timing Analysis	Allows you to determine the speed-critical and performance-limiting paths in a design and optimize critical timing paths.	✓	✓
	Functional Simulation	Allows you to simulate the logical function of a design with zero propagation delays.	✓	✓
	Timing Simulation	Allows you to simulate the logical function and worst-case timing of a fully synthesized and optimized design.	✓	✓
	ModelSim-Altera	Simulates HDL code using a VHDL or Verilog HDL testbench stimuli.	✓	
	Testbench Generation	Converts waveform simulation file to testbench file. Automatically creates a testbench template after compilation to jump-start testbench development.	✓	✓
	SignalTap II Logic Analysis	Captures and analyzes state of internal nodes or I/O signals of devices running in-system and at system speeds; now supports incremental routing of additional nodes and custom advanced trigger logic generation.	✓	✓
	SignalProbe In-System Debugging	Incrementally routes an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer.	✓	✓
	IBIS Model Generation	Outputs design-specific IBIS models to third-party software for signal integrity and EMC analysis.	✓	✓
	Third-Party Synthesis Support	Includes integration to third-party synthesis software from Mentor Graphics, Synopsys, and Synplicity.	✓	✓
	Hardware/Software Co-Simulation Support	Outputs simulation models to simulate complete systems including programmable logic, embedded processor, embedded processor software, and memory.	✓	✓
	Formal Verification	Supports third-party formal verification software that can identify functional differences between source RTL netlists and post-place-and-route netlists without the creation of test vectors.	✓	
	PowerGauge™ Power Analysis	Links power consumption estimates with user-specific design files and operating parameters.	✓	✓
Device Programming Standard Support	Standard Test and Programming Language (STAPL)	Supports the IEEE 1532 standard and the JEDEC-approved Jam™ STAPL standard for programming devices in-system via the IEEE 1149 standard Joint Test Action Group (JTAG) interface.	✓	✓

Recommended System Configurations

Listed below are the components required to operate Altera design software on Windows-based or Linux-based PCs, Sun workstations, or HP workstations. Table 4 lists the memory requirements for Altera devices.

Windows-Based or Linux-Based PC

A Pentium II 400 with 512-Mbyte system memory (faster systems provide better software performance) is required for Windows operating systems. Pentium III processors are required for Red Hat Linux operating systems.

- Operating System Software
 - Microsoft Windows XP
 - Microsoft Windows 2000
 - Microsoft Windows NT version 4.0 or later
 - Red Hat Linux Version 7.3 or 8.0
- SVGA monitor
- CD-ROM drive
- Serial port (or USB port if using Windows XP or Windows 2000) for the MasterBlaster™ download cable
- USB port for USB-Blaster™ download cable (Windows XP or Windows 2000)
- Parallel port for use with the ByteBlaster™ II or ByteBlasterMV™ download cables
- Internet Explorer 5.0 or later

Sun Workstation

- Sun Ultra workstation with color monitor running Solaris version 7 or 8
- ISO 9990-compatible CD-ROM drive
- X-Windows display
- Netscape Navigator 5.0 or later or Internet Explorer 5.0 or later
- Serial port for use with the MasterBlaster download cable

HP Workstation

- HP 9000 700/800 Workstation with color monitor running HP-UX version 11.0 with the Additional Core Enhancements (ACE) dated November 1999 or later
- ISO 9990-compatible CD-ROM drive
- X-Windows display
- Netscape Navigator 5.0 or later or Internet Explorer 5.0 or later
- Serial port for use with the MasterBlaster download cable

Altera Programming Hardware

Altera's USB-Blaster, ByteBlaster II, and MasterBlaster download cables (described in Table 5 on page 9) are available for in-circuit reconfiguration of Stratix II, Cyclone, Stratix, Stratix GX, APEX II, APEX 20K, Excalibur, FLEX 10K, ACEX, FLEX 6000, and Mercury devices, and in-system programming of MAX II, MAX 7000, MAX 3000, and MAX 9000 devices. These cables download device data directly from the Altera design software user interface or directly from a system prompt.

When used with the Quartus II software, the USB-Blaster, ByteBlaster II, and MasterBlaster configuration cables also provide communication for the SignalTap II embedded logic analyzer included in the Quartus II software. For a description of the SignalTap II embedded logic analyzer, see Table 3 on page 7.

The Altera Programming Unit (APU), used with the appropriate programming adapters, provides the hardware and software needed for programming all Altera devices. Use Table 5 to select the appropriate programming hardware for your system.

Table 4. System Memory Requirements			
Family	Device	Minimum Physical Ram	Minimum Swap Space ¹
Stratix II	EP2S15	512 Mbytes	512 MB
	EP2S30, EP2S60	1 Gbyte	1 Gbyte
	EP2S90	1.5 Gbytes	1.5 Gbytes
	EP2S130	2 Gbytes	2 Gbytes
	EP2S180	3 Gbytes	3 Gbytes
Stratix	EP1S210, EP1S20, EP1S25	512 Mbytes	512 Mbytes
	EP1S230, EP1S40, EP1S60	1 Gbyte	1 Gbyte
	EP1S280	1.5 Gbytes	1.5 Gbytes
Stratix GX	EP1SGX10C, EP1SGX10D, EP1SGX25C, EP1SGX25D, EP1SGX25F	512 Mbytes	512 Mbytes
	EP1SGX40D, EP1SGX40F	1 Gbyte	1 Gbyte
Cyclone	EP1C3, EP1C6	256 Mbytes	256 Mbytes
	EP1C12, EP1C20	512 Mbytes	512 Mbytes
MAX II	EPM240, EPM570	256 Mbytes	256 Mbytes
	EPM1270, EPM2210	512 Mbytes	512 Mbytes
APEX 20K APEX 20KE APEX 20KC	EP20K100, EP20K100E, EP20K160E, EP20K200, EP20K200C, EP20K200E, EP20K30E, EP20K60E	256 Mbytes	256 Mbytes
	EP20K300E, EP20K400, EP20K400C, EP20K400E, EP20K600C, EP20K600E	512 Mbytes	512 Mbytes
	EP20K1000C, EP20K1000E, EP20K1500C, EP20K1500E	1 Gbyte	1 Gbyte
APEX II	EP2A15, EP2A25, EP2A40	512 Mbytes	512 Mbytes
	EP2A70	1.5 Gbytes	1.5 Gbytes
Excalibur	EPXA1	256 Mbytes	256 Mbytes
	EPXA4	512 Mbytes	512 Mbytes
	EPXA10	1 Gbyte	1 Gbyte
FLEX 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, MAX 7000, MAX 3000, ACEX	All	256 Mbytes	256 Mbytes
Mercury	EP1M120	256 Mbytes	256 Mbytes
	EP1M350	512 Mbytes	512 Mbytes

Table 5. Altera Programming Hardware			
Ordering Code	Hardware	Hardware Interface	Additional Features
PL-USB-BLASTER	USB Blaster download cable	USB	Supports the SignalTap II embedded logic analyzer as well as 1.8-, 2.5-, 3.3-, and 5.0-V operation. Also supports Altera's latest low-cost serial configuration devices used with Cyclone FPGAs.
PL-BYTEBLASTER2	ByteBlaster II parallel download cable	PC parallel port	Supports the SignalTap II embedded logic analyzer as well as 1.8-, 2.5-, 3.3-, and 5.0-V operation. Also supports Altera's latest low-cost serial configuration devices used with Cyclone FPGAs.
PL-MASTERBLASTER	MasterBlaster download cable	USB/RS-232	Supports the SignalTap II embedded logic analyzer as well as 1.8-, 2.5-, 3.3-, and 5.0-V operation.
PL-APU	Altera Programming Unit (APU)	USB	Supports traditional out-of-system programming.

Altera Development Kits

Altera development kits provide a platform to quickly transition concepts into working designs by allowing application software development to begin earlier in the design flow. In addition to a high-quality development board designed around Altera's state-of-the-art FPGAs, many Altera development kits include:

- On-board memory
- Industry-standard I/O ports
- A power supply
- A one-year Quartus II software evaluation license for the PC
- The SOPC Builder system development tool
- Embedded processor C/C++ development tools
- A ByteBlasterMV or ByteBlaster II download cable
- Technical documentation
- Reference designs

Altera offers a wide range of development kits, each addressing particular discipline challenges. For example, the Altera DSP Development Kit Stratix Professional Edition is a prototyping platform that provides wireless system designers with a signal processing solution, whereas the Nios development kits cover a broad range of embedded applications. Table 6 shows a sample of development kits that are available to help speed designs to market.

Quartus II Development Kit Evaluation Licenses

Altera development kits and a number of third-party development kits now include a one-year evaluation license to use the Quartus II software on PCs. These evaluation licenses include complete Quartus II software feature and device support for one full year.

Development kit customers can also upgrade to a full Quartus II subscription for up to half off the subscription list price. Upgrading to a subscription provides:

- A perpetual license file for the Quartus II software
- One year of software updates
- ModelSim-Altera simulation software (includes a 15-month license)
- Choice of operating-system support

More information on the Altera Design Software Subscription Program can be found on page 3.

Third-Party Solutions

Several third-party solutions complement Altera's design software and development tools. Third-party vendor support includes synthesis and verification tools, programming hardware, and development tools for Excalibur device design.

ACCESS Program & Partners

ACCESS Program partners include EDA vendors who have developed design entry, HDL synthesis and simulation, design rule checker, formal verification, static timing analysis, signal-integrity-analysis, and other complementary products that support Altera FPGAs and CPLDs. Altera design software users can take advantage of the latest EDA tools and methodologies available through the ACCESS Program partners. Table 7 on page 12 summarizes some of the vendors and tools that support the Quartus II design software.

Third-Party Programming Hardware

A number of third-party companies supply hardware to program and configure Altera PLDs. Third-party programming hardware suppliers include:

- Data I/O
- BP Microsystems
- System General Company

Third-Party Support for Embedded Processor Design

Altera software subscriptions include third-party development tools to support the Nios embedded processor (see Table 8 on page 12).

More Information on the Altera Web Site

For more information on Altera's comprehensive design solutions—including software, development kits, design partners, and third-party support—refer to the Altera web site at www.altera.com.

Table 6. Altera & Altera Partner Development Kits			
Development Kit	Altera Device Featured on Board	Applications	Ordering Code or Partner URL
Nios Development Kit, Cyclone Edition	Cyclone EP1C20	Systems development with Nios and Cylone in one complete package.	NIOS-DEVKIT-1C20
Nios Development Kit, Stratix Edition	Stratix EP1S10	Systems development with Nios and Stratix in one complete package.	NIOS-DEVKIT-1S10
Nios Development Kit, Stratix Professional Edition	Stratix EP1S40	Same as the Nios Stratix Edition but with a much larger FPGA.	NIOS-PROKIT-1S40
DSP Development Kit, Stratix Edition	Stratix EP1S25	Provides a complete DSP development platform.	DSP-BOARD/S25
DSP Development Kit, Stratix Professional Edition	Stratix EP1S80	Same as the DSP Stratix Edition but with Altera's largest FPGA.	DSP-BOARD/S80
PCI Development Kit, Stratix Edition	Stratix EP1S25	A flexible, low-cost FPGA development board in a PCI short card form factor.	PCI-BOARD/S25
PCI High-Speed Development Kit, Stratix Professional Edition	Stratix EP1S60	Same as the PCI Stratix Edition but with Stratix EP1S60 device.	PCI-BOARD/S60
Parallax Cyclone SmartPack	Cyclone EP1C3	Cyclone Smart Pack is designed to give engineers the opportunity to explore the features of the Cyclone device family.	www.parallax.com
Parallax Stratix SmartPack	Stratix EP1S10 or EP1S25	Stratix Smart Pack is designed to give engineers the opportunity to explore the features of the Stratix device family.	www.parallax.com
MJL Stratix Development Kit	Stratix EP1S25	General-purpose platform for Stratix device embedded systems development.	www.mjl.com
Microtronix Stratix Development Kit	Stratix EP1S25	Microtronix provides a full range of features and software that is flexible enough to enable development for almost any application.	www.microtronix.com
Rapid Technology Stratix High-Speed Development Kit	Stratix EP1S10	A flexible and powerful Stratix development platform ideal for analyzing high-speed LVDS I/O and DSP algorithm development.	www.rapid-technology.com
El Camino DIGILAB SX High-End Prototyping System	Stratix EP1S30 to EP1S80	An ideal low-cost, high-performance programmable platform for prototyping and verification.	www.elca.de
El Camino DIGILAB XA Development Board	Excalibur EPXA4 or EPXA10	This kit provides customers involved in network processing a number of user-definable network interfaces. It can be used as an evaluation board, a prototyping tool, or as a standard product.	www.elca.de
Rowe Engineering Q5 Series	Up to 4 Stratix EP1S25F780 devices	The Q5 board, designed for customers in communications and optical system design, leverages the high-speed LVDS channels in Stratix allowing for 840 Mbps transfer rate on a multitude of inputs.	www.roweengineering.net
Colorado Electronic Product Design (CEPD) CAS10 Stratix Development Board	Stratix EP1S10	Prototyping board that offers features that significantly improve the design and testing of advanced DSP systems.	www.cepdinc.com
Avvida Tsunami PCI-Based Image Processing Solution	Stratix EP1S25 and up	PCI plug-in card for imaging and high-bandwidth applications.	www.avvidasystems.com
Gidel Stratix PROCStar Kit	Up to 3 Stratix EP1S25 devices	Prototyping and real-time emulation of high-bandwidth, high-density applications such as DSP, imaging, video processing, aerospace, and military systems.	www.gidel.com
Arrow Maximum Overdrive Kit	MAX EPM7128A	An easy-to-use, low-cost entry point to Altera's industry-leading MAX 7000 CPLDs.	www.arrow.com/alteramax
Future Electronics Cyclone-Nios-Kit	Cyclone EP1C12	An easy, inexpensive way to evaluate Altera's low cost Cyclone FPGA family.	www.futureelectronics.com

Table 7. Altera & Altera Partner Development Kits		
Design Flow	Vendor	Tool Name
Design Entry and/or Synthesis	Mentor Graphics	Precision, LeonardoSpectrum™
	Synopsys	Design Compiler, FPGA Compiler II
	Synplicity	Synplify, Synplify Pro, Amplify
Verification	Aldec	Active HDL, Riviera
	Altium	nVisage, Protel
	Celoxica	Nexas PDK
	Cadence	Conformal LEC, Incisive, Verilog-XL, NC Verilog, NC VHDL
	Mentor Graphics	Tau, XTK
	Model Technology	ModelSim, ModelSim-Altera
	Summit	Visual Elite, Riviera Elite
	SynaptiCAD	VeriLogger Pro
	Synopsys	LEDA, PrimeTime, Scirocco, VSS, VCS
	Synplicity	Identify

Table 8. Vendors & Tools that Support Nios Processor Design		
Design Flow	Vendor	Tool Name
Development and Debug Tools	Red Hat	GNUPro development tools for Excalibur devices and the Nios processor
	Mentor Graphics	XRAY debugger for Excalibur devices code lab EDE and code lab debug for the Nios processor
	Sophia Systems	WatchPoint debugger tool for the Nios processor
	Viosoft Corp.	Arriba! IDE for the Nios processor
System Integration Tools	Beach Solutions	EASI-Integrator for Excalibur devices
Operating System Support	Accelerated Technology	Nucleus PLUS RTOS for the Nios processor and Excalibur devices
	Shugyo Design Technologies	KROS operating system for the Nios processor
	Micrium	mC-OS-II RTOS for the Nios processor
	MiSPO Co. Ltd.	NORTi Compact Edition for the Nios processor
	Microtronix Datacom Ltd.	mClinux operating system for the Nios processor
	OSE Systems	OSE RTOS for Excalibur devices
Real-Time Trace Tools	Microtronix Datacom Ltd.	Nios OCD Solutions Kit



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