

Cyclone V FPGA Family Package and I/O Selector Guide



Cyclone V FPGA Features

The following features, packages, and I/O matrices give you an overview of our devices. To get the full story, check out our online selector guide: www.altera.com/selector.

		Cyclone® V E FPGAs (1.1 V)				
		5CEA2	5CEA5	5CEA8	5CEB5	5CEB9
Core Fabric	LEs	25,000	48,000	75,000	150,000	300,000
	M10K memory blocks (Kb)	1,560	3,120	4,620	6,160	12,760
	MLAB	25% of ALMs can be configured as MLABs				
	PLLs	4	4	4	4	4
	Global clock networks	16	16	16	16	16
Hard IP	DSP blocks	39	78	132	220	406
	PCI Express® hard IP blocks	-				
	Memory controllers	1	1	2	2	2
Interconnect	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels (875 Mbps receive, 840 Mbps transmit)	48	100	100	122	122
	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2				

Cyclone V FPGA Features Cont.

		Cyclone V GX FPGAs (1.1 V), 3.125-Gbps Transceivers				
		5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9
Core Fabric	LEs	25,000	50,000	75,000	150,000	300,000
	M10K memory blocks (Kb)	1,200	2,920	4,620	6,160	12,760
	MLAB	25% of ALMs can be configured as MLABs				
	PLLs	5	6	6	7	8
	Global clock networks	16	16	16	16	16
Hard IP	DSP blocks	40	70	132	220	406
	PCI Express hard IP blocks	1	1	1	1	1
	Memory controllers	1	2	2	2	2
Interconnect	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels (875 Mbps receive, 840 Mbps transmit)	48	100	100	122	122
	Transceiver (SERDES) channels	3	6	6	9	12
	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2				

		Cyclone V GT FPGAs (1.1 V), 5G Transceivers		
		5CGTD3	5CGTD5	5CGTD8
Core Fabric	LEs	75,000	150,000	300,000
	M10K memory blocks (Kb)	4,620	6,160	12,760
	MLAB	25% of ALMs can be configured as MLABs		
	PLLs	6	7	8
	Global clock networks	16	16	16
Hard IP	DSP blocks	132	220	406
	PCI Express hard IP blocks	2	2	2
	Memory controllers	2	2	2
Interconnect	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3		
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS		
	LVDS channels (875 Mbps receive, 840 Mbps transmit)	100	122	122
	Transceiver (SERDES) channels	6	9	12
	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2		

Cyclone V Series Package and I/O Matrices

Cyclone V E, GX, and GT FPGAs (1.1 V), Up to 5G Transceivers

	Cyclone V E, GX, and GT FPGAs (1.1 V), Up to 5G Transceivers								
	EQFP (E)	UBGA (U)	FBGA (F)						
	144 pin 22 x 22 (mm) 0.5-mm pitch	484 pin 19 x 19 (mm) 8.0-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch	324 pin 19 x 19 (mm) 1.0-mm pitch	484 pin 23 x 23 (mm) 1.0-mm pitch	672 pin 25 x 25 (mm) 1.0-mm pitch	896 pin 31 x 31 (mm) 1.0-mm pitch	1,152 pin 35 x 35 (mm) 1.0-mm pitch	
5CEA2	90	300	140		300				
5CEA5	90	300	140		300				
5CEA8		260			260	360			
5CEB5					260	345	488		
5CEB9						345	488		
5CGXC3		194 3	97 3	114 3	194 3				
5CGXC4		238 6		120 6	238 6	360 6			
5CGXC5		238 6		120 6	238 6	360 6			
5CGXC7					230 6	345 9	488 9		
5CGXC9						345 9	488 9	688 12	
5CGTD3		238 6			238 6	360 6			
5CGTD5					230 6	345 9	488 9		
5CGTD8						345 9	488 9	688 12	

636
12 Values on top indicate available user I/O pins; values at the bottom indicate the 3.125-Gbps or 5G transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.