

# MAX CPLD Series Package & I/O Matrix



- Device available in commercial temperature. Contact Altera for industrial temperature.
- Device available in commercial and industrial temperatures.
- Device available in commercial and industrial, and qualified to extended temperatures.
- 36 Number indicates available user I/O pins.
- Vertical migration (Same V<sub>CC</sub>, GND, ISP, and input pins).

		MAX <sup>®</sup> II 3.3 V, 2.5 V, 1.8 V				MAX 3000A 3.3 V				MAX 7000B 2.5 V				MAX 7000AE 3.3 V				MAX 7000S 5.0 V								
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Density & Speed	Macrocells <sup>1</sup>	192	440	980	1,700	32	64	128	256	512	32	64	128	256	512	32	64	128	256	512	32	64	128	160	256	512
	Logic Elements (LEs)	240	570	1,270	2,210	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Pin-to-Pin Delay (ns) <sup>2</sup>	4.7, 6.2, 7.6	5.5, 7.1, 8.8	6.3, 8.2, 10.1	7.1, 9.2, 11.3	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10	3.5, 5.0, 7.5	3.5, 5.0, 7.5	4.0, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	7.5, 10, 12	5.0, 6.0, 7.5, 10	5.0, 6.0, 7.5, 10	6.0, 7.5, 10, 15	6.0, 7.5, 10, 15	7.5, 10, 15	7.5, 10, 15
PLCC (L) <sup>3</sup>	44-Pin					34	34				36				36	36				36	36					
	84-Pin																	68				68	68	64		
TQFP (T) <sup>4</sup>	44-Pin					34	34				36	36				36	36				36	36				
	100-Pin	80	76				66	80				68	84	84			68	84	84				68	84	84	
	144-Pin		116	116				96	116				100	120	120											
PQFP (Q or R) <sup>5</sup>	100-Pin																								84	
	160-Pin																							100	104	124
	208-Pin								158	172				164	176				164	176						164
BGA (B) <sup>6</sup>	256-Pin													212						212						
FBGA (F) <sup>7</sup>	100-Pin	80	76									68	84				68	84	84							
	256-Pin		160	212	204			98	161	208				100	164	212			100	164	212					
	324-Pin				272																					
UBGA (U) <sup>8</sup>	49-Pin										36	41														
	169-Pin													141	141											
MBGA (M) <sup>9</sup>	100-Pin <sup>2</sup>	80	76																							
	256-Pin <sup>2</sup>		160	212																						

- <sup>1</sup> Typical equivalent macrocells for MAX II devices
- <sup>2</sup> Package not available for MAX IIG devices
- <sup>3</sup> Plastic J-lead chip carrier
- <sup>4</sup> Thin quad flat pack
- <sup>5</sup> Plastic quad flat pack
- <sup>6</sup> Ball-grid array (1.27 mm)
- <sup>7</sup> FineLine BGA® (1.0 mm)
- <sup>8</sup> Ultra FineLine BGA (0.8 mm)
- <sup>9</sup> Micro FineLine BGA (0.5 mm)

Package Statistics	PLCC		TQFP			PQFP			BGA	FBGA			UBGA		MBGA	
Number of Pins	44	84	44	100	144	100	160	208	256	100	256	324	49	169	100	256
Nominal Length x Width (mm)	18 x 18	30 x 30	12 x 12	16 x 16	22 x 22	17 x 23	31 x 31	31 x 31	27 x 27	11 x 11	17 x 17	19 x 19	7 x 7	11 x 11	6 x 6	11 x 11
Maximum Surface Area (mm) <sup>1</sup>	312	921	149	262	493	399	986	952	740	125	296	369	52	125	36	121
Maximum Height (mm)	4.57	4.57	1.2	1.2	1.6	3.4	4.1	4.1	2.7	1.7	3.5 <sup>1</sup>	3.5 <sup>1</sup>	1.55	2.2	1.2	1.2
Nominal Lead Pitch (mm)	1.27	1.27	0.8	0.5	0.5	0.65	0.65	0.5	1.27	1	1	1	0.8	0.8	0.5	0.5
Maximum Lead Width (mm)	0.53	0.53	0.45	0.27	0.27	0.4	0.4	0.27	0.9	0.7	0.7	0.7	0.6	0.6	0.35	0.35

<sup>1</sup> Altera's maximum height specification is 2.6 mm. The 3.5 maximum height specification shown reflects the JEDEC specifications.

# MAX CPLD Series Features



		MAX II 3.3 V, 2.5 V, 1.8 V				MAX 3000A 3.3 V					MAX 7000B 2.5 V					MAX 7000AE 3.3 V					MAX 7000S 5.0 V							
		EPM240/G	EPM570/G	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM3032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S		
Features	User Flash Memory (Kbit)	8				-					-					-					-							
	Boundary Scan JTAG	✓				-					✓					✓					-	-	✓	✓	✓	✓	✓	✓
	JTAG ISP	✓				-					✓					✓					-							
	Fast Input Registers	✓				-					✓					✓					-							
	Programmable Register Power-Up	✓				-					✓					✓					-							
	Programmable Ground Pins	✓				-					✓					✓					-							
	Open-Drain Outputs	✓				-					✓					✓					-							
	Programmable Pull-Up Resistors	✓				-					✓					-					-							
	Bus Hold	✓				-					✓					-					-							
	JTAG Translator	✓				-					-					-					-							
	Real-Time ISP	✓				-					-					-					-							
	0.5-mm BGA Packages <sup>1</sup>	✓				-					-					-					-							
Core Voltage & I/O Options	Core Voltage (V)	1.8				3.3					2.5					3.3					5.0							
	MultiVolt Core (V)	3.3, 2.5, 1.8				-					-					-					-							
	MultiVolt I/O (V)	3.3, 2.5, 1.8, 1.5				5.0, 3.3, 2.5					3.3, 2.5, 1.8					5.0, 3.3, 2.5					-	5.0, 3.3	5.0, 3.3	5.0, 3.3	5.0, 3.3	5.0, 3.3		
	I/O Power Banks	2	2	4	4	1					2					1					1							
	Maximum I/O Pins	80	160	212	272	34	66	98	161	208	36	68	100	164	212	36	68	100	164	212	36	68	100	104	124	164		
	Maximum Output Enables	80	160	212	272	6	6	6	6	10	6	6	6	6	10	6	6	6	6	10	6							
	Transistor-to-Transistor Logic (TTL) (5.0-V Tolerance)	-	-	✓ <sup>2</sup>	✓ <sup>2</sup>	✓					-					✓					✓							
	LVTTL/LVCMOS	✓				✓					✓					✓					-	✓	✓	✓	✓	✓	✓	
	32-Bit, 66-MHz PCI Compliant	-	-	✓	✓	-					-					-					-							
	GTL+/SSTL-2, SSTL-3, All Class I & Class II	-				-					✓					-					-							
	Schmitt Triggers	✓				-					-					-					-							
	Programmable Slew Rate	✓				✓					✓					✓					✓							
Programmable Drive Strength	✓				-					-					-					-								

<sup>1</sup> Package not available for EPM2210/G device  
<sup>2</sup> An external series resistor must be used for 5.0-V tolerance