

This document provides late-breaking information about device support in the Altera® Quartus® II software version 10.1 SP1. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about new features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

- “Device Support and Pin-Out Status” on page 1
- “Memory and Disk Space Recommendations” on page 2
- “Timing and Power Models” on page 5
- “Changes in Device Support” on page 6

## Device Support and Pin-Out Status

This section contains information about the status of device support in the Quartus II software version 10.1 SP1.

### Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

**Table 1. Devices with Full Support**

Device Family	Devices	
MAX® V	5M40ZE64	5M80ZE64
	5M160ZE64	

### Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 2](#) that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

**Table 2. Devices with Advance Support**

Device Family	Devices	
Cyclone® IV GX	EP4CGX30CF23	EP4CGX50
	EP4CGX75	
MAX V	5M40ZM64	5M80ZM64
Stratix® V	5SGXA5	5SGXA7

## Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 3](#) that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

**Table 3. Devices with Initial Information Support**

Device Family	Devices	
Stratix V	5SGXA3	5SGXA4
	5SGXB5	5SGXB6
	5SGSB7	5SGSB8

## Memory and Disk Space Recommendations

A full installation of the Altera Complete Design Suite requires approximately 8.2 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your **TEMP** directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of **.sof** files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

[Table 4](#) lists the memory required to process designs targeted for Altera devices.

**Table 4. Memory and Disk Recommendations**

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria® GX	EP1AGX20	512 MB	512 MB
	EP1AGX35, EP1AGX50, EP1AGX60	1.0 GB	1.5 GB
	EP1AGX90	1.5 GB	2.0 GB

**Table 4. Memory and Disk Recommendations (Continued)**

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria II GX	EP2AGX45	1.0 GB	1.5 GB
	EP2AGX65	1.5 GB	2.0 GB
	EP2AGX95, EP2AGX125, EP2AGX190	3.0 GB	4.0 GB
	EP2AGX260	4.0 GB	6.0 GB
Arria II GZ	EP2AGZ225	3.0 GB	4.0 GB
	EP2AGZ300	4.0 GB	6.0 GB
	EP2AGZ350	N/A	8.0 GB
Cyclone	All	512 MB	512 MB
Cyclone II	EP2C5, EP2C8, EP2C20	512 MB	512 MB
	EP2C35, EP2C50	1.0 GB	1.5 GB
	EP2C70	1.5 GB	2.0 GB
Cyclone III	EP3C5, EP3C10, EP3C16, EP3C25, EP3C40	512 MB	512 MB
	EP3C55, EP3C80	768 MB	1.0 GB
	EP3C120	1.5 GB	2.0 GB
Cyclone III LS	EP3CLS70, EP3CLS100	1.5 GB	2.0 GB
	EP3CLS150, EP3CLS200	3.0 GB	4.0 GB
Cyclone IV E	EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40	512 MB	512 MB
	EP4CE55, EP4CE75	768 MB	1.0 GB
	EP4CE115	1.0 GB	1.5 GB
Cyclone IV GX	EP4CGX15, EP4CGX22, EP4CGX30	512 MB	512 MB
	EP4CGX50, EP4CGX75	1.0 GB	1.5 GB
	EP4CGX110, EP4CGX150	1.5 GB	2.0 GB
HardCopy® II	HC210	1.5 GB	2.0 GB
	HC220, HC230, HC240	3.0 GB	4.0 GB
HardCopy III	HC325	N/A	8.0 GB
	HC335	N/A	12.0 GB
HardCopy IV	HC4E25	N/A	8.0 GB
	HC4GX15	N/A	12.0 GB
	HC4E35, HC4GX25	N/A	16.0 GB
	HC4GX35	N/A	20.0 GB

**Table 4. Memory and Disk Recommendations (Continued)**

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
MAX	All	512 MB	512 MB
MAX II	All	512 MB	512 MB
MAX V	All	512 MB	512 MB
Stratix	EP1S10, EP1S20	512 MB	512 MB
	EP1S25, EP1S30, EP1S40, EP1S60	1.0 GB	1.5 GB
	EP1S80	1.5 GB	2.0 GB
Stratix GX	EP1SGX10	512 MB	512 MB
	EP1SGX25, EP1SGX40	1.0 GB	1.5 GB
Stratix II	EP2S15	512 MB	512 MB
	EP2S30	1.0 GB	1.5 GB
	EP2S60, EP2S90	1.5 GB	2.0 GB
	EP2S130, EP2S180	3.0 GB	4.0 GB
Stratix II GX	EP2SGX30, EP2SGX60	1.0 GB	1.5 GB
	EP2SGX90	1.5 GB	2.0 GB
	EP2SGX130	3.0 GB	4.0 GB
Stratix III	EP3SL50, EP3SE50, EP3SL70	1.0 GB	1.5 GB
	EP3SE80	1.5 GB	2.0 GB
	EP3SL110, EP3SE110, EP3SE150, EP3SL200	3.0 GB	4.0 GB
	EP3SE260, EP3SL340	4.0 GB	6.0 GB
Stratix IV	EP4SGX70	1.5 GB	2.0 GB
	EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2	3.0 GB	4.0 GB
	EP4SGX290	4.0 GB	6.0 GB
	EP4SGX360, EP4S100G3, EP4S100G4	N/A	8.0 GB
	EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5	N/A	12.0 GB
Stratix V	5SGXA3	4.0 GB	6.0 GB
	5SGXA4	N/A	8.0 GB
	5SGXA5, 5SGXB5	N/A	12.0 GB
	5SGXA7, 5SGXB6, 5SGSB7	N/A	16.0 GB
	5SGSB8	N/A	20.0 GB

## Timing and Power Models

Table 5 lists a summary of timing and power model status in the current version of the Quartus II software.

**Table 5. Devices with Timing and Power Models**

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Arria II GZ	All	Final – 10.1	Final – 10.1
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	(All 1.0V)	Final – 10.0 SP1	Final – 10.0 SP1
	(All 1.2V)	Final – 10.0	
Cyclone IV GX	EP4CGX15	Final – 10.1	Preliminary
	EP4CGX22	Preliminary	
	EP4CGX30		
	EP4CGX50		
	EP4CGX75		
	EP4CGX110	Final – 10.1	
EP4CGX150			
HardCopy III	(All)	Preliminary	Preliminary
HardCopy IV E	(All)	Preliminary	Preliminary
HardCopy IV GX	(All)	Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		
MAX V	(All)	Preliminary	Preliminary

**Table 5. Devices with Timing and Power Models (Continued)**

Device Family	Device	Timing Model Status	Power Model Status
Stratix III	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	
Stratix IV	EP4SE230	Final – 9.1 SP1	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4	Final – 10.0	
	EP4S100G5		
	EP4SGX70		
	EP4SGX110	Final – 10.0	Final – 10.1
	EP4SE820	Final – 10.0 SP1	
Stratix V	(All)	Preliminary	Preliminary

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, Cyclone III, HardCopy II, MAX, MAX II, Stratix, Stratix II, Stratix II GX, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 8.1 and earlier.

## Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed.

## Change Notifications

This section provides notifications for changes to devices.

### MAX V pin name change

For the MAX V ordering code 5M160Z-M100C4, one of the pins in the package `ddb_maxv2mbga100_pkg.ddb` was incorrectly named, and has been correctly renamed.

Applies to: MAX V devices

### Arria II GX power model updated

For Arria II GX devices, the power model is updated to reduce static power consumption. This is a change to a finalized power model.

Applies to: Arria II GX devices

### Arria II GX VCO frequency change

The maximum frequency of a PLL VCO in Arria II GX devices is updated to 1.4 GHz. Designs with a PLL VCO frequency higher than 1.4 GHz must rerun the Fitter to recalculate the valid PLL settings.

Applies to: Arria II GX devices

### Arria II GX new DLL range

The frequency range specification of the Delay Lock Loop (DLL) in Arria II GX devices is updated after further characterization.



For more information, refer to the [Errata Sheet for Arria II GX](#).

Applies to: Arria II GX devices

## Device Support Not Fixed

This section provides details for device support issues that have not yet been fixed.

### Gate-level simulation flow for Stratix V designs

The generation of EDA simulation netlist files for post-synthesis or post-fit gate-level simulation is not supported in the Quartus II software version 10.1 SP1.

Applies to: Stratix V devices

### MAX 7000 S Programmer error

For MAX 7000 S devices, performing blank-check operations in the Programmer causes internal errors when using any other devices in the same JTAG chain.

Applies to: MAX 7000 S devices

## Device Support Fixed

This section provides details for device support issues that have been fixed.

### Final timing model change – Arria II GX LVPECL maximum data rate

The Arria II GX LVPECL maximum data rate is increased from 350 MHz to the LVDS data rate, which is a minimum of 500 MHz.

Applies to: Arria II GX devices



For more information, refer to the [Arria II GX Device Handbook](#).

### Final timing model change – Arria II GX LVDS timing parameters

The Arria II GX sampling window for the LVDS SERDES is updated for speed grades 3 and 4 from 750 ps to 300 ps, for speed grade 5 from 750 ps to 350 ps, and for speed grade 6 from 750 ps to 400 ps. To see the improved RSKM value, re-run the TimeQuest Timing Analyzer.

The Arria II GX TCCS for the LVDS SERDES is updated for speed grades 3 and 4 from 100 ps to 150 ps, for speed grade 5 from 100 ps to 175ps, and for speed grade 6 from 100 ps to 200 ps. To see the updated TCCS number, re-run the TimeQuest Timing Analyzer.

Applies to: Arria II GX devices



For more information, refer to the [Arria II GX Device Handbook](#).

### Final timing model change – Cyclone III LVDS maximum speed increase

The Cyclone III LVDS maximum speed clock frequency is increased from 370 MHz to 402.5 MHz. This issue was fixed in the Quartus II software version 10.1.

Applies to: Cyclone III, C7 devices

### Stratix IV and HardCopy IV incorrect VCM programming

For Stratix IV and HardCopy IV devices, prior to the release of the Quartus II software version 10.1, Altera incorrectly programmed the VCM (input common mode voltage) of dedicated HSSI refclk pins with a value of 0.82 V, when the industry specification is 1.1 to 1.2 V. To use the previous setting, you must use the .ini file available from Altera.

Applies to: Stratix IV and HardCopy IV devices

### Arria II GX incorrect timing delay values

Arria II GX devices with a speed grade of 6 exceed the maximum data rate specified in the device datasheet. In the Quartus II software version 10.0 and earlier, the data rate limit is not enforced during the compilation flow.

Applies to: Arria II GX devices

### Final timing model change — Stratix III DDR input functional failure

Stratix III DDR input registers fail to capture edge-aligned input data correctly while the TimeQuest Timing Analyzer shows positive slack when you use the corner clock pin and corner PLL.

The final timing model was changed for Stratix III devices by updating the delay for a path from the corner clock pin to the corner PLL. Designs utilizing the affected path on the affected Stratix III parts must rerun the TimeQuest Timing Analyzer. If new timing violations occur, you must rerun the Fitter.

This issue was fixed in the Quartus II software version 10.0 SP1.

Applies to: Stratix III devices, including EP3SL200F1517, EP3SE260F1517, EP3SL340F1517, EP3SL340F1760

### PCI Express Compiler cannot generate files for Gen1 protocol

The PCI Express Compiler v10.0 did not support IP and MegaWizard generation or regeneration of PCIe® Gen1 x4 or x8 designs targeting the Stratix IV and HardCopy IV device families.



For more information, refer to Knowledge Database solution [rd07012010\\_723](#).

This issue is fixed in the Quartus II software versions 10.0 SP1 and later.

Applies to: Stratix IV and HardCopy IV devices

### Cyclone IV GX incorrect simulation

In versions of the Quartus II software versions 10.0 and earlier, for Cyclone IV GX devices, when simulating a design containing an altlvds megafunction, an incorrect result could occur when the **Enable bitslip control** option was turned on.

Applies to: Cyclone IV GX devices prior to the Quartus II software version 10.1

