

These release notes for the PCI Express Compiler v7.1 contain the following information:

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## System Requirements

The PCI Express Compiler has the same system requirements as the Quartus® II software.



For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for UNIX & Linux* on the Altera® website.

## New Features & Enhancements

The following list outlines new features and enhancements in this release:

- Support for the Arria™ GX device family
- SOPC Builder interface
- Enhanced design methodology with the new Incremental Compilation module (ICM)
- Enhanced Simple and Chaining DMA example designs

## Errata Fixed in This Release

The following erratum was fixed in this release:

Incorrect Default Constraints for Projects Targeted for Devices Other Than Stratix II GX Can Cause Timing Issues

For existing up-to-date errata, refer to the *PCI Express Compiler v 7.1 Errata Sheet* on the Altera website.

## Contacting Altera

Although every effort has been made to ensure that this version of the PCI Express Compiler works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera website at [www.altera.com](http://www.altera.com). You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Information Type	USA & Canada	All Other Locations
Technical support	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	<a href="http://www.altera.com">www.altera.com</a>	<a href="http://www.altera.com">www.altera.com</a>
Altera literature services	<a href="mailto:literature@altera.com">literature@altera.com</a>	<a href="mailto:literature@altera.com">literature@altera.com</a>
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	<a href="ftp://ftp.altera.com">ftp.altera.com</a>	<a href="ftp://ftp.altera.com">ftp.altera.com</a>

## Revision History

[Table 2](#) shows the revision history for the PCI Express Compiler version 7.1.

Version	Date	Revision
7.1	May 2007	The following enhancements were made: <ul style="list-style-type: none"> <li>• Support for the Arria GX device family</li> <li>• SOPC Builder interface</li> <li>• Enhanced design methodology with new Incremental Compilation module</li> <li>• Enhanced Simple and Chaining DMA example designs</li> </ul>
7.0	March 2007	The following enhancement was made: <ul style="list-style-type: none"> <li>• Support for the Cyclone<sup>®</sup> III device family</li> </ul>
6.1	December 2006	The following enhancement was made: <ul style="list-style-type: none"> <li>• Support for the Stratix<sup>®</sup> III device family</li> </ul>

**Table 2. PCI Express Compiler v7.1 Revision History**

Version	Date	Revision
2.1.1	June 2006	<p>The following enhancements were made:</p> <ul style="list-style-type: none"> <li>● The Stratix II GX ALT2GXB Vod/pre-emphasis settings changed to improve the margins in meeting the Transmitter Compliance Eye Diagram.</li> <li>● PHY Support logic provides better timing margins in Cyclone® II devices.</li> <li>● The example design DMA now handles out-of-order read completions.</li> <li>● The AER Header Log registers have been enhanced for PCI-SIG read only compliance test</li> <li>● The &lt;variation&gt;_phy_support module added cfg_msicsr, cfg_pmcsr, and cfg_prmcsr ports.</li> <li>● Example design now sends the correct completion for zero length read requests.</li> </ul>
2.1.0	April 2006	<ul style="list-style-type: none"> <li>● Additional Transaction layer support for x1 MegaCore function to operate at 62.5 MHz or 125 MHz.</li> <li>● Added support for Advanced Error Reporting (AER) and ECRC generation and checking in the x8 MegaCore function (previously only supported in x4 and x1)</li> <li>● Additional Rx Buffer configuration options that optimize your application's performance with minimal resource utilization.</li> <li>● Enhanced flow control algorithm improves throughput when both PCI Express link directions are heavily loaded</li> <li>● Support additional custom external PHY modes</li> <li>● Support for compliance with <i>PCI Express Specification v1.1</i></li> </ul>
2.0.0	October 2005	<ul style="list-style-type: none"> <li>● Added Stratix II GX, HardCopy® II, and Cyclone II device support</li> <li>● Added x8 support</li> </ul>
1.0.0	April 2005	<ul style="list-style-type: none"> <li>● Initial Publication</li> </ul>



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