

These release notes for the PCI Compiler version 6.1 contain the following information:

- [New Features & Enhancements](#)
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- [Contact Altera](#)
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For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for Solaris & Linux* on the Altera

website www.altera.com/literature/lit-qts.jsp.

New Features & Enhancements

This is a maintenance release. The following list outlines the new feature in this release:

- Added preliminary support for Stratix® III devices.

Errata Fixed in This Release

No errata were fixed in this maintenance release.



For existing up-to-date errata, refer to the PCI Compiler version 6.1 errata sheet on the following errata page of the Altera website:

www.altera.com/literature/es/es_pci_compiler_61.pdf

Contact Altera

Although every effort has been made to ensure that this version of the PCI Compiler works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera website at www.altera.com. You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Table 1. Contacting Altera

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Revision History [Table 2](#) shows the revision history for the PCI Compiler version 6.1.

Table 2. PCI Compiler Revision History

Version	Date	Revision
6.1	December 2006	<ul style="list-style-type: none"> • Maintenance release; updated documentation and screen shots to reflect release version. • Removed installation instructions from the release notes.

Table 2. PCI Compiler Revision History

Version	Date	Revision
4.1.1	April 2006	<ul style="list-style-type: none"> ● Maintenance release; updated documentation and screen shots to reflect release version. ● Fixed the default installation path in the documentation. ● Removed installation instructions from the PCI Compiler User Guide. ● Moved the reference design and timing information from the release notes to the user guide.
4.1.0	October 2005	<ul style="list-style-type: none"> ● Added preliminary support for Stratix II GX and HardCopy II device families. ● Updated support for Stratix II, MAX II, and Cyclone II device families. ● Reduced device utilization for PCI-Avalon Bridge ● Fixed the following MegaWizard Plug-In Manager flow problems: <ul style="list-style-type: none"> - The CIS pointer default value was made to be 0x00000000 instead of 0x00000001 ● Fixed the following SOPC Builder flow problems: <ul style="list-style-type: none"> -The prefetchable write transactions were made to disconnect at BAR boundary. - Fixed a configuration address translation bug that prevented the selection of <code>idsel=AD[31]</code> - Fixed the issue in which for 32-bit master read transactions, byte enables from the Avalon side were not being passed to the PCI side. - Corrected the issue where <code>intan</code> was asserted after <code>reset</code> if the Control register module is not implemented. ● Fixed the following issues that affect both flows: <ul style="list-style-type: none"> - The <code>pci_mt64</code> did not end the PCI master transactions immediately following the <code>lm_lastn</code> assertion in the case of a 32-bit PCI target response to a 64-bit write request and the PCI Target is asserting random wait states. - In the case of an Address parity error detected by the PCI core, the PCI core used to also enable the <code>perrn</code> drivers although it does not assert <code>devseln</code>. - Fixed protocol violation where <code>stopn</code> was asserted after the end of the transaction in the case of wait states on <code>irdyn</code>. - Fixed protocol violation where <code>framen</code> was not deasserted immediately after detecting <code>stopn</code> asserted during 64-bit master write transaction to 32-bit target with target wait states. - Fixed a protocol violation where <code>framen</code> was asserted for one cycle during single cycle DAC memory read transaction.



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