

These release notes for the Triple Speed Ethernet MegaCore Function v7.1 contain the following information:

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## System Requirements

The Triple Speed Ethernet MegaCore Function has the same system requirements as the Quartus II software.



For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for UNIX & Linux Workstations*.

## New Features & Enhancements

The following list outlines the new features and enhancements in this release:

- Preliminary support for Arria™ GX device family
- Run-time configurable IP header alignment to 32-bit boundaries on transmit and receive datapaths
- Optional Memory Block Type Selection for MAC data FIFO
- Optional GMII-to-SGMII Bridge Logic
- Enables efficient sharing of GX transceivers by providing an option to export the power-down signal
- MAC FIFO status, Pause Frame Generation and Magic Packet signals are available as ports in addition to being available via the control register space

## Errata Fixed in This Release

No errata were fixed in this release.



For existing up-to-date errata, refer to the *Triple Speed Ethernet MegaCore Function v7.1 Errata Sheet* on the errata page on the Altera website at [www.altera.com/literature/lit-es.jsp](http://www.altera.com/literature/lit-es.jsp).

## Contact Altera

Although every effort has been made to ensure that this version of the Triple Speed Ethernet MegaCore function works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera world-wide website at [www.altera.com](http://www.altera.com). You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Information Type	USA & Canada	All Other Locations
Technical support	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>	<a href="http://www.altera.com/mysupport/">www.altera.com/mysupport/</a>
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	<a href="http://www.altera.com">www.altera.com</a>	<a href="http://www.altera.com">www.altera.com</a>
Altera literature services	<a href="mailto:literature@altera.com">literature@altera.com</a>	<a href="mailto:literature@altera.com">literature@altera.com</a>
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	<a href="ftp://ftp.altera.com">ftp.altera.com</a>	<a href="ftp://ftp.altera.com">ftp.altera.com</a>

## Revision History

[Table 2](#) shows the revision history for the Triple Speed Ethernet MegaCore function.

Version	Date	Revision
7.1	May 2007	<ul style="list-style-type: none"> <li>• Preliminary support for Arria™ GX device family.</li> <li>• Run-time configurable IP header alignment to 32-bit boundaries on transmit and receive datapaths.</li> <li>• Optional Memory Block Type Selection for MAC data FIFO, GMII-to-SGMII Bridge Logic and sharing of GX transceivers.</li> <li>• MAC FIFO status, Pause Frame Generation and Magic Packet signals available as ports in addition to being available via the control register space.</li> </ul>
7.0	March 2007	Preliminary support for Cyclone® III devices.
6.1	December 2006	First release of the MegaCore function.



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