

These release notes for the DDR and DDR2 SDRAM Controller Compiler version 7.1 contain the following information:

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System Requirements

The DDR and DDR2 SDRAM Controller Compiler has the same system requirements as the Quartus® II software.



For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for UNIX & Linux Workstations*.

New Features & Enhancements

The following list outlines new features and enhancements in this release:

- Full support for Stratix® II GX devices

Errata Fixed in This Release

No errata were fixed in this release.



For existing up-to-date errata, refer to the *DDR and DDR2 SDRAM Controller Compiler v7.1 Errata Sheet* on the Altera® website at www.altera.com/literature/es/es_ddr_ddr2_sdram_71.pdf.

Contacting Altera

Although every effort has been made to ensure that this version of the DDR and DDR2 SDRAM Controller works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera world-wide website at www.altera.com. You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Table 1. Contacting Altera

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Nontechnical customer service	800-767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Revision History

[Table 2](#) shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

Table 2. DDR & DDR2 SDRAM Controller Revision History

Version	Date	Revision
7.1	May 2007	See “New Features & Enhancements” on page 1 .
7.0	March 2007	Maintenance release.
6.1	December 2006	Maintenance release.
3.4.1	June 2006	Support for Cyclone® II A devices
3.4.0	April 2006	<ul style="list-style-type: none"> • Datapath includes round-trip delay model • Support for clock generation using dedicated PLL outputs • Improved support for fed-back clock • Full support for Cyclone II devices
3.3.1	November 2005	Maintenance release.
3.3.0	October 2005	<ul style="list-style-type: none"> • Custom control of on-die termination (ODT) settings for DDR2 SDRAM • Support for eight banks • Each data strobe (DQS) signal supports four or eight data bits (DQ) on Stratix II devices • Full support for Stratix® II devices in DDR2 SDRAM • Preliminary support for HardCopy® II and Stratix II GX devices • Improved Cyclone II constraints for push-button 167-MHz performance • Improved timing analysis scripts and constraints



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