

About Altera WiMAX Solutions

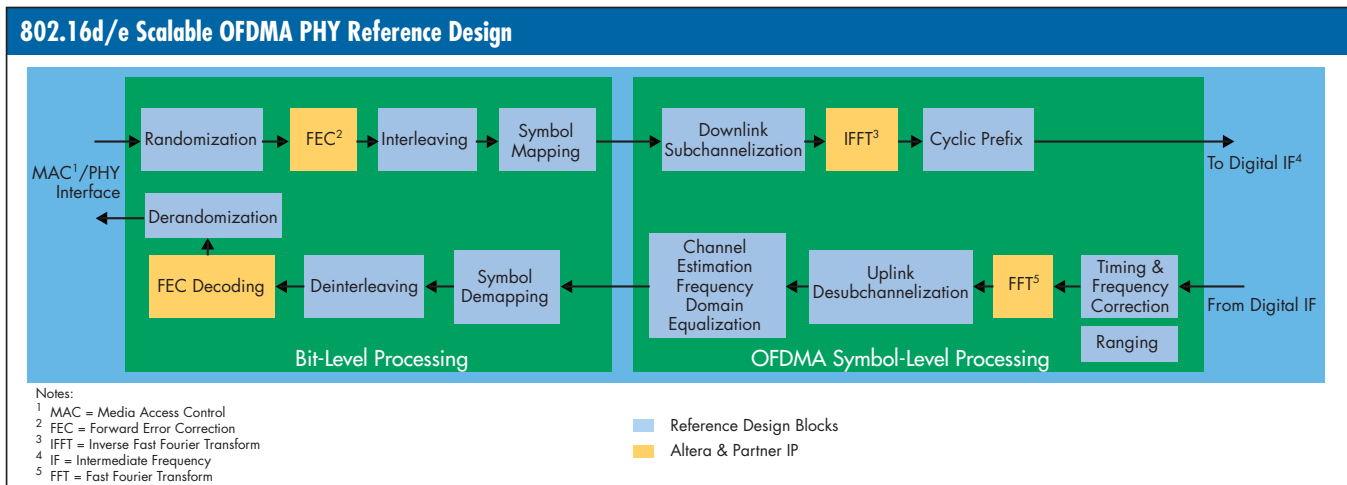
Altera is your trusted partner in wireless system design. You can rely on Altera's expertise in the wireless market to deliver the right solutions for your WiMAX design challenges. To find the wireless solutions that appear here, as well as many other reference designs, intellectual property (IP) functions, and additional support for wireless design, please visit our web site at www.altera.com/end-markets/wireless/overview/wir-overview.html or contact your local sales representative.

802.16d/e Baseband PHY Reference Design

Altera's 802.16d/e PHY reference design demonstrates how you can use Stratix® II and Cyclone™ II FPGAs for both fixed- and mobile-WiMAX basestation designs. The reference design will accelerate your time to market by providing the necessary building blocks for both bit-level and symbol-level processing.

Features

- The reference design is based on scalable OFDMA PHY.
- Building blocks for both uplink and downlink functionality include OFDMA subchannelization, time and frequency synchronization, channel estimation, and ranging.
- The deliverables include fixed-point MATLAB models and synthesizable register transfer level (RTL) with test benches for Cyclone II and Stratix II FPGAs.



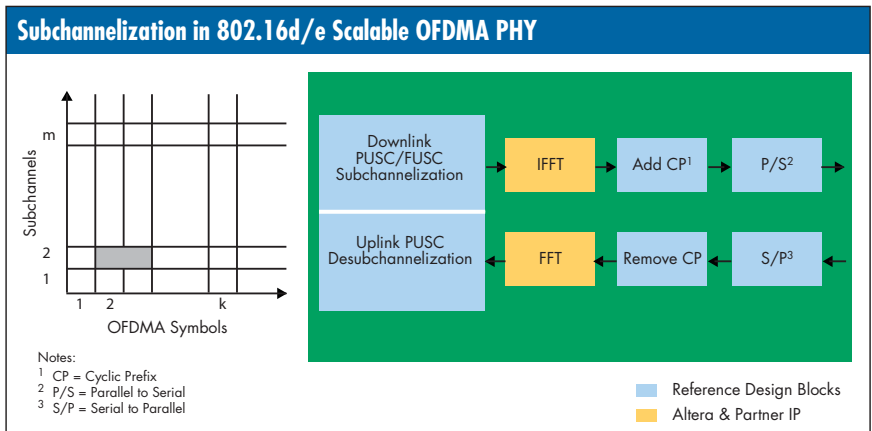
Scalable OFDMA Subchannelization Reference Design

Altera's scalable OFDMA subchannelization reference design demonstrates how you can use Stratix II and Cyclone II FPGAs with embedded processors to efficiently integrate both control- and data-plane functionality involved in the complex 802.16d/e subchannelization protocol.

- The highly parameterizable design is optimized for efficient use of Stratix II and Cyclone II FPGA resources.
- The reference design can be easily modified to support designs based on the Super 3G standard.

Features

- 128, 256, 512, 1K, and 2K FFT sizes address variable bandwidths from 1.25 to 20 MHz.
- The design features both uplink and downlink subchannelization, including partially used subchannelization (PUSC) and fully used subchannelization (FUSC) schemes.
- Both fixed and variable pilots and cyclic prefix insertion schemes are supported.



WiMAX MAC Layer Implementation Support

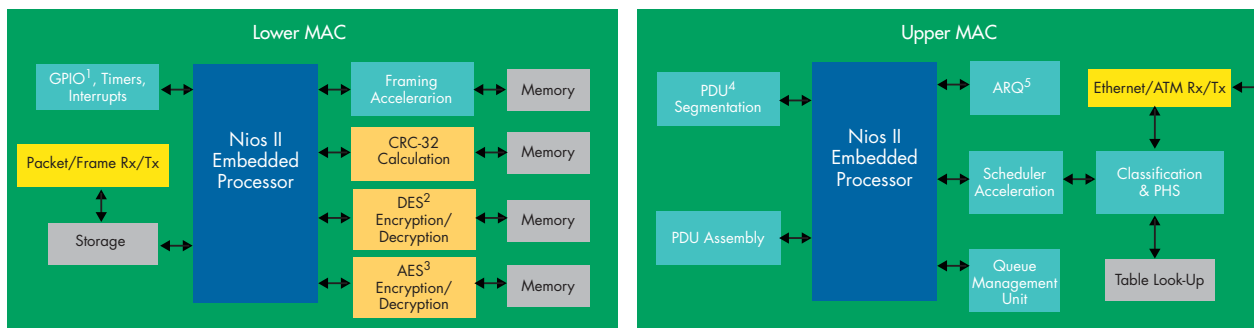
Altera offers the building blocks necessary to quickly create customized WiMAX MAC layer implementation on Stratix II and Cyclone II FPGAs with Nios® II embedded processors.

Features

- Nios II processor-based cyclic redundancy check (CRC)-algorithm acceleration reference design demonstrates the execution time improvement using custom instructions and custom peripherals.
- AES and DES encryption/decryption IP cores are optimized for Altera® FPGA families.

- Upper MAC data-plane functions, including segmentation, classification, and scheduling can be efficiently implemented in FPGA logic or embedded processors.
- Control-plane functionality, including system control and monitoring, can be implemented in software on the Nios II embedded processor.
- FPGA implementation of MAC enables low-cost tailor-made MAC processing while providing the flexibility of software programmable and hard-wired options.
- Altera HardCopy® II structured ASICs further lower the cost while maintaining the flexibility offered by the Nios II embedded processor.

Lower MAC & Upper MAC Implementation With Nios II Embedded Processor



- Notes:
- ¹ GPIO = General Purpose I/O
 - ² DES = Data Encryption Standard
 - ³ AES = Advanced Encryption Standard
 - ⁴ PDU = Protocol Data Unit
 - ⁵ ARQ = Automatic Repeat-Request

- FPGA Logic
- Altera & Partner IP

Altera & AMPP Partner IP Cores for WiMAX

Altera's complete portfolio of FEC, FFT/IFFT, and digital IF processing cores for WiMAX are optimized for implementation on Stratix II and Cyclone II FPGAs.

Features

- Highly parameterizable Reed-Solomon and Viterbi FEC cores support input parameters including constraint and traceback lengths, number of soft bits, and order of polynomial.
- Highly scalable Turbo Convolutional and Turbo Product cores offer throughputs in excess of 100 Mbps and are fully compatible with WiMAX specifications including support for Hybrid-ARQ.
- FFT/IFFT MegaCore® IP functions address the wide range of FFT sizes in the 802.16d/e standard and are optimized to exploit the TriMatrix™ memory and digital signal processing (DSP) blocks in Stratix II FPGAs.
- Finite impulse response (FIR) compiler and numerically controlled oscillator (NCO) compiler cores enable the rapid creation of optimized filter architectures and digital oscillators required for digital up and down conversion.

| Altera Wireless Ecosystem IP Functions | |
|--|------------------------------|
| Altera MegaCore IP | Partner IP |
| Viterbi Decoder | Turbo Convolutional* |
| Reed-Solomon Compiler | Turbo Product* |
| FFT/IFFT Compiler | LDPC* |
| FIR Compiler | Complete 802.16d PHY and MAC |
| NCO Compiler | Complete RF Module |

* Altera Megafunction Partners Program (AMPPSM) Partner