

About Altera Cellular Infrastructure Solutions

Altera is your trusted partner in wireless system design. You can rely on Altera's expertise in the wireless market to deliver the right solutions for your cellular baseband design challenges. To find the wireless solutions that appear here, as well as many other reference designs, intellectual property (IP) functions, and additional support for wireless design, please visit our website at www.altera.com/end-markets/wireless/overview/wir-overview.html or contact your local sales representative.

3GPP Release 6—Achieve Less Than \$1 Cost per Channel

Altera offers a complete portfolio of low-cost Cyclone™ II and high-density Stratix® II FPGAs, HardCopy® II structured ASICs, optimized IP cores, and reference designs to efficiently implement 3rd Generation Partnership Project (3GPP) release 6, channel card functionality, including high-speed downlink packet access (HSDPA) and high-speed uplink packet access (HSUPA).

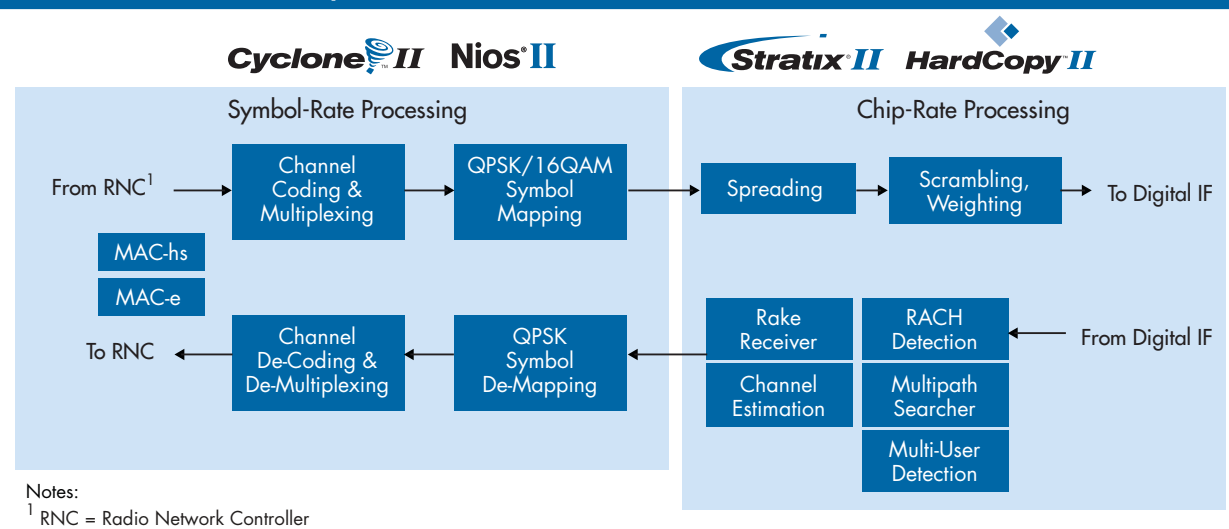
Features

- Altera has undertaken a comprehensive architecture study of the 3GPP release 6 standard, including the new HSUPA functionality, and offers the most compelling and cost-effective solution that can achieve a cost per channel target of less than US\$1.
- Stratix II FPGAs with embedded TriMatrix™ memory architecture and a new, innovative logic structure, Adaptive Logic Modules

(ALMs), maximize logic efficiency and performance. Stratix II FPGAs are well suited for implementing correlations and memory-intensive chip-rate processing, while retaining flexibility for future upgrades.

- HardCopy II structured ASICs dramatically reduce costs to lower than US\$1 per channel and have up to 70 percent lower power consumption than Stratix II FPGAs, while ensuring a seamless migration path from the FPGA, including pin-to-pin compatibility, with minimal customer intervention.
- Cyclone II FPGAs have been built from the ground up for the lowest cost and are well suited for implementing bit-level processing, including channel coding and modulation.
- Nios® II embedded processors, along with custom instructions, can be used to efficiently implement media access control (MAC)-hs and MAC-e functionality within the FPGA, further reducing board cost and size.

3GPP Release 6—Channel Card Implementation



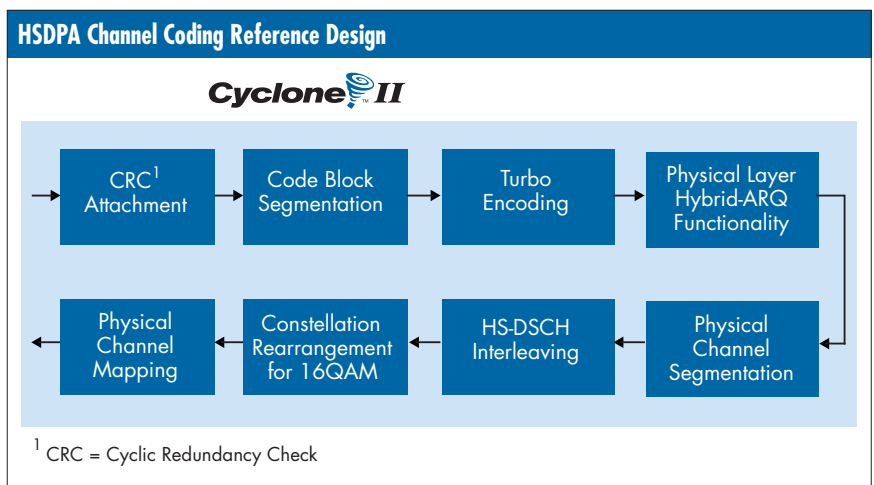
HSDPA Channel Coding Reference Design

Altera's HSDPA channel coding reference design demonstrates the cost effectiveness of Cyclone II FPGAs in implementing parallel multi-channel bit-level processing, including turbo encoding and

hybrid automatic repeat-request (ARQ) functionality with minimum latency. (Continued on reverse.)

Features

- The reference design supports up to 15 high-speed downlink shared channel (HS-DSCH) codes with a maximum data rate of 14.4 Mbps and latency <1.5ms.
- The entire channel coding chain is implemented using <60 percent logic elements (LEs), and <35 percent memory in a low-cost Cyclone II EP2C8 FPGA.
- The design also comes with a Linkport interface and external memory interface (EMIF) interfaces to function as a digital signal processing (DSP) co-processor.

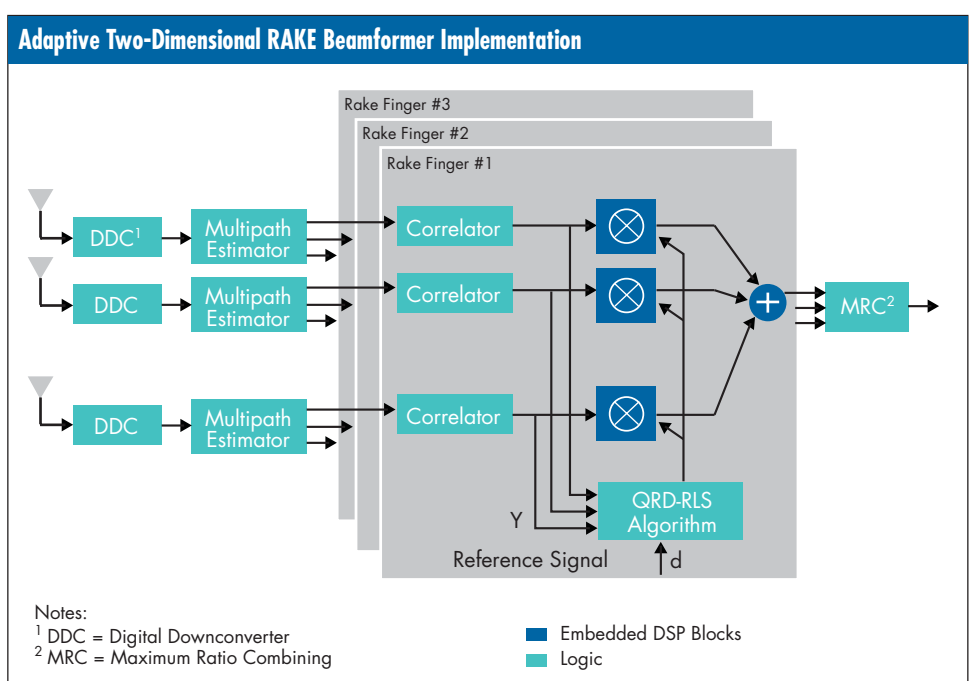


Beamforming & MIMO Implementation

Altera offers easy-to-use tools such as DSP Builder along with building-block IP functions to quickly implement advanced techniques such as beamforming, multiple-input multiple-output (MIMO), and multi-user detection.

Features

- Altera offers matrix decomposition and inversion IP cores such as QR-Decomposition-Based Recursive Least Squares (QRD-RLS), singular value decomposition (SVD), and Cholesky decomposition that are required to implement beamforming, MIMO, and multi-user detection.
- Stratix II FPGAs with embedded DSP blocks and Nios® II embedded processors enable efficient implementation of complex multiplications in hardware.
- The Alamouti space time decoder reference design for a 2 x 2 antennas system can also be scalable to support additional antenna configurations.



Altera & AMPP Partner IP Cores

Altera offers a complete portfolio of Forward Error Correction (FEC), fast Fourier transform (FFT)/inverse fast Fourier transform (IFFT) and digital intermediate frequency (IF) processing IP cores, optimized for implementation on Stratix II and Cyclone II FPGAs.

Features

- The highly parameterizable Reed-Solomon and Viterbi FEC cores support input parameters including constraint and traceback lengths, number of soft bits, and order of polynomial.
- Highly scalable turbo convolutional encoder and decoder cores, decoder throughputs in excess of 10 Mbps, are fully compatible with 3GPP specifications.

- FFT/IFFT MegaCore® functions address a wide range of FFT sizes for the Super 3G standard and are optimized to exploit the TriMatrix™ memory and DSP blocks in Stratix II FPGAs.

Altera Wireless Ecosystem IP Functions	
Altera MegaCore IP	Partner IP
Viterbi Decoder	3GPP Turbo Encoder*
Reed-Solomon Compiler	3GPP Turbo Decoder*
FFT/IFFT Compiler	
FIR Compiler	
NCO Compiler	

* Altera Megafunction Partners Program (AMPPSM) Partner