

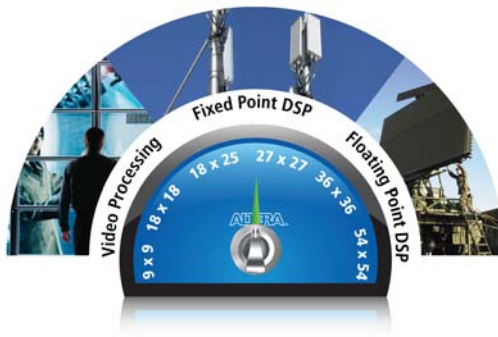


Enabling High-Performance, High-Precision Signal Processing

28-nm Variable-Precision DSP Block Architecture

More than ever, digital signal processing (DSP) applications need high performance and high precision, in the greater than 18-bit range. That's why the DSP capabilities of FPGAs are ideal. In our 28-nm Stratix® V FPGAs, you can take advantage of our new variable-precision DSP blocks to support a variety of functions:

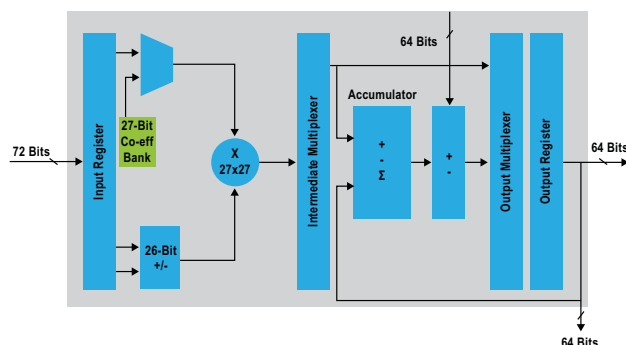
- High-precision multiply accumulate
- High-precision finite impulse response (FIR) filters
- High-precision fast Fourier transforms (FFTs)
- Floating-point FFTs
- Floating-point matrix inversion



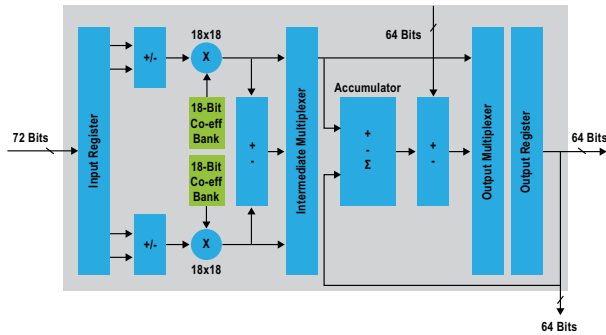
Better System Performance, Less Power

The variable-precision DSP block provides native support for signal processing of varying precisions—for example, 9x9, 18x18, 27x27, and 18x36—in a sum or independent mode. Freed from FPGA architecture restrictions, you'll be able to apply the optimum precision at each stage of the DSP datapath. You'll also benefit from increased system performance and reduced power consumption.

High-Precision Mode



18-Bit Precision Mode



The block, backwards compatible with Stratix III and Stratix IV FPGAs, offers advantages unavailable in competitive offerings:

- In high-precision mode using only one block, you can implement single-precision floating-point operations, such as mantissa multiplication.
- Cascade each variable-precision DSP block with other blocks to further extend the range of precisions it can support—and without any loss in precision.
- Efficiently implement asymmetric complex multipliers of increasing precision to support FFT bit growth.
- Cascade four variable-precision DSP blocks, to create 27x27 complex multiplier operation for floating-point FFT algorithms. Also, our FFT Compiler MegaCore® IP function efficiently supports single-precision floating point from an easy-to-use GUI.

Variable-Precision DSP Advantage

Multiplier Size	Competing DSP Architecture	Altera 28-nm Advantage
Native support for 27x27 multiply mode		✓
Variable-precision multiplier size: 27x27, 18x36, or (dual) 18x18		✓
Efficient implementation of floating-point signal processing		✓
Coefficient register banks within the DSP block		✓
Efficient 18x25 complex multiply for FFTs	✓	✓
Accumulator size	48 bits	64 bits
Width of the cascade bus	48 bits	64 bits
Pre-adder support for symmetric filters	✓	✓
Support for systolic FIR filters	✓	✓

Want to Dig Deeper?

For more information about how you can take advantage of the variable-precision DSP blocks in Stratix V FPGAs, contact your local Altera® sales representative or FAE, or visit www.altera.com/dsp

Altera Corporation

101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters

Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 94 602 000

Altera Japan Ltd.

Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.

Unit 11-18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2945 7000

