

# Altera's 40-nm FPGA transceivers: meeting system bandwidth, power, and BER requirements

Stratix® IV GX and GT FPGAs offer a robust solution for high-speed serial connectivity. The integrated transceivers are architected to deliver excellent jitter performance while minimizing power and maintaining noise immunity. Key advantages of the 40-nm devices include:

- 48 transceivers architected to have the highest system bandwidth and power efficiency
- Lowest jitter for extended bit-error ratio (BER) for greater product reliability
- Greater board design flexibility
- Integrated transceivers up to 11.3 Gbps

## Highest system bandwidth and power efficiency

It's important for transceivers to minimize power consumption, since this directly affects system cost and cooling requirements. The Stratix IV GX transceiver is architected to deliver the highest system bandwidth at the lowest power for a wide range of applications and protocols. In comparison to Stratix IV GX transceivers, the nearest competing devices deliver 48 percent higher power at 6 Gbps (see Table 1).

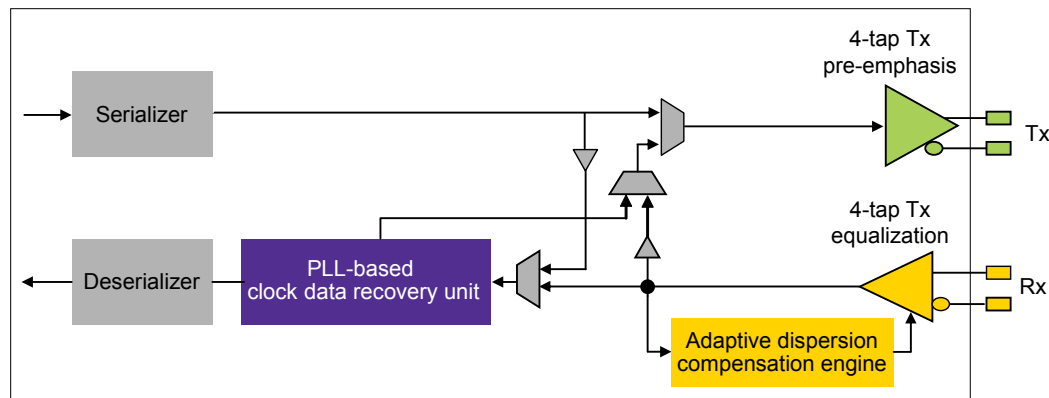
**Table 1. PMA transceiver power / channel of Altera 40-nm device vs. nearest competitor**

Data rate	Stratix IV GX/GT FPGA	Nearest competitor
3.125 Gbps	100 mW	100 mW (par)
6.5 Gbps	135 mW	200 mW (+48%)
8.5 Gbps	165 mW	N/A (no 8.5-Gbps support)
10.3 Gbps	190 mW	N/A
11.3 Gbps	200 mW	N/A

## Lowest jitter enables extended BER for greater product reliability

The physical media attachment (PMA) is an embedded macro dedicated to receiving and transmitting off-chip high-speed serial data streams. The PMA channel consists of full duplex paths (transmit and receive) with I/O buffers, programmable output voltage, pre-emphasis and equalization, clock data recovery (CDR), and serializer/deserializer (SERDES) blocks.

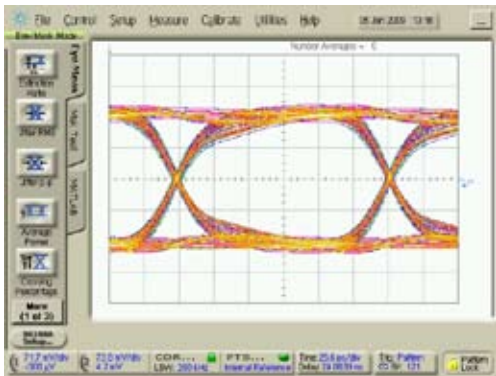
### Stratix IV GX transceiver PMA block



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Stratix IV GX transceivers use advanced power supply regulation and filtering techniques to reduce transmitter jitter and improve receiver jitter tolerance. This allows the transceivers to exhibit superior BER performance when used in real system links. On-chip voltage regulators for both transmit and receive phase-locked loops (PLLs), careful isolation of sensitive analog circuitry, and extensive use of on-die and on-package decoupling capacitors all contribute to a robust power distribution scheme for the transceivers while delivering exceptionally clean power to the analog circuits. The eye diagram shows the operation of the transmitter at 6.25 Gbps. Architectural innovations in the transceiver power distribution network enable the reduced output jitter and vertical noise displayed in the diagram.

### Altera 40-nm output waveform



### Greater board design flexibility

- The low jitter of the Stratix IV GX transceivers allows for flexibility in tradeoffs between channel costs and system performance (BER).
- Our adaptive dispersion compensation engine (ADCE) delivers Plug & Play Signal Integrity and the ability to change the position of backplane cards on the fly. You no longer have to manually reconfigure your backplane equalization settings. You can design systems with truly universal cards that plug into multiple card positions in system backplanes.
- Stratix IV GX FPGAs utilize the proven dynamic reconfiguration technology in Stratix II GX devices. This allows you to dynamically reconfigure transmit pre-emphasis and receiver equalization settings and to switch data rates or protocols in backplane applications, without affecting the FPGA core.

## Simulation models, tools, and resources

- HSPICE models\* – Full circuit simulation for the most accuracy and flexibility
- Verilog Analog Mixed Signal (AMS)\* – Behavioral model for quick, accurate simulation, simulated in a Synopsys HSPICE environment
- Pre-emphasis and equalization link estimator (PELE)\*: Tool for finding the optimal pre-emphasis and equalization settings for your transceiver channel
- [Pin connection guidelines](#) – Includes examples on minimizing power supplies required to power up Stratix IV FPGAs
- [Early power estimator \(EPE\)](#) – Spreadsheet analysis that estimates your design's power consumption
- [White paper - Altera at 40 nm: Jitter, Signal Integrity, Power, and Process-Optimized Transceivers](#)
- [Board Design Resource Center](#) - Board design-related resources for Altera® devices

\* These models/tools available through your Regional Support Center (RSC)

Table 2. Jitter comparison between Stratix IV GX FPGA and the nearest competitor's device at 6.5 Gbps

6G jitter component	40-nm Stratix IV GX FPGA RJ = 1.2 ps rms		Competitive device RJ = 2.41 ps rms <sup>1</sup>	
BER	1E-12	1E-17	1E-12	1E-17
Random jitter @ BER	16.8	20.4	33.6	40.8
Deterministic jitter	15.7		24.8	
TJ = $\sigma$ *RJ	32.5ps	36.1ps	58.3ps	65.6ps
TJ (UI)	0.21 UI	0.23 UI	0.37 UI	0.41 UI <sup>2</sup>
CEI 6G spec	0.30 UI	0.30 UI	0.30 UI	0.30 UI

Notes:

<sup>1</sup>Source: <http://www.techonline.com/learning/webinar/210601383>

<sup>2</sup>TJ does not meet CEI 6G transmit jitter specification

### Want to dig deeper?

For more information about how the jitter superiority and low power consumption of Stratix IV GX FPGAs can benefit your design, contact your local FAE or Altera sales representative, or visit [www.altera.com/stratix4](http://www.altera.com/stratix4).

**Altera Corporation**  
 101 Innovation Drive  
 San Jose, CA 95134  
 USA  
[www.altera.com](http://www.altera.com)

**Altera European Headquarters**  
 Holmers Farm Way  
 High Wycombe  
 Buckinghamshire  
 HP12 4XF  
 United Kingdom  
 Telephone: (44) 1 94 602 000

**Altera Japan Ltd.**  
 Shinjuku i-Land Tower 32F  
 6-5-1, Nishi-Shinjuku  
 Shinjuku-ku, Tokyo 163-1332  
 Japan  
 Telephone: (81) 3 3340 9480  
[www.altera.co.jp](http://www.altera.co.jp)

**Altera International Ltd.**  
 Unit 11-18, 9/F  
 Millennium City 1, Tower 1  
 388 Kwun Tong Road  
 Kwun Tong  
 Kowloon, Hong Kong  
 Telephone: (852) 2945 7000  
[www.altera.com.cn](http://www.altera.com.cn)

