



Boost Your Productivity with System-Level Design

Qsys System Integration Tool

The Qsys system integration tool, available in the Quartus® II software v11.0, takes system-level design to a new level. Simply put, Qsys gets you to finished product faster and more easily.

The Qsys interconnect, based on network-on-a-chip (NoC) technology, achieve nearly double the f_{MAX} versus its predecessor, the SOPC Builder system interconnect fabric. By enabling faster FPGA-based system development and design reuse compared to SOPC Builder, Qsys will save you valuable time and effort. Using the tool, you'll also gain automatic pipelining capabilities and the ability to control the tradeoffs between f_{MAX} and latency.

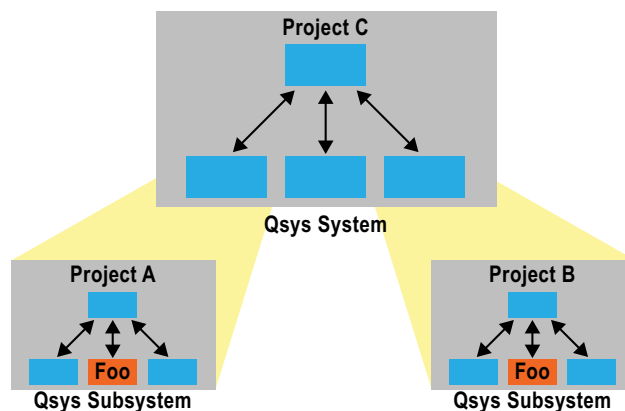
You'll find Qsys useful for various types of applications in areas including high-speed interface protocols, external memories, video and image processing, and embedded.

Meet Your Next-Generation System Design Needs

Qsys takes what SOPC Builder brought to system-level design, and delivers much more:

- Faster development with support for hierarchical design. A hierarchical design flow enables scalable designs, supports team-based design, and maximizes design reuse. See Figure 1.
- Faster verification with automatic testbench generation and the availability of a verification IP suite. Also bring your board up faster by sending read/write transactions into a live system for debug.
- IP management capabilities, provide designers access to a wide variety of Qsys Compliant IP cores and facilitate design reuse of the designer's IP and Qsys systems.
- Support for industry-standard interfaces, so you can connect IP cores of different interfaces. Supported interfaces in Quartus II software v11.0 include our Avalon® open-standard bus. See Figure 2.

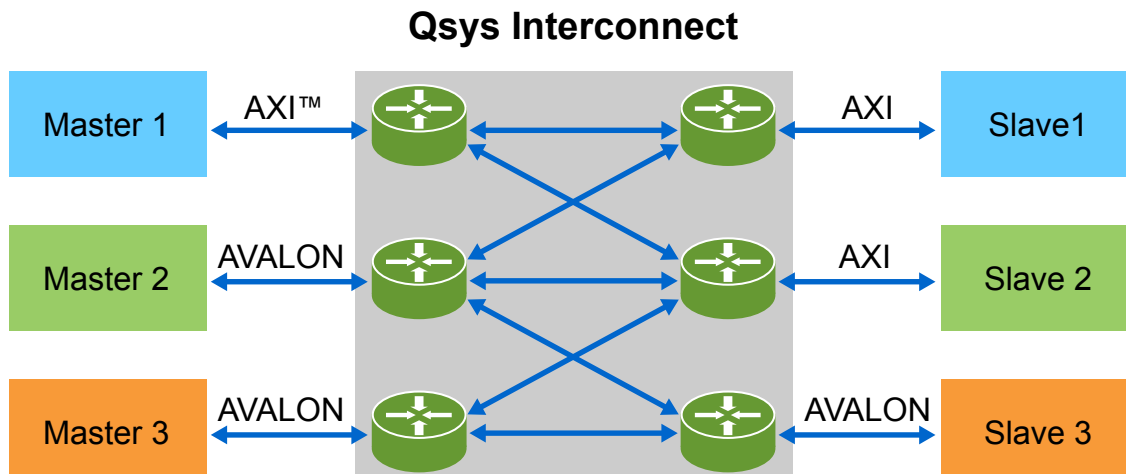
Figure 1: Hierarchical Design



Qsys Advantage: Hierarchy Support

- Fewer Components = Fast GUI
- Fewer Components = Manageable
- Enables System to Scale

Figure 2: Mixed Industry-Standard Interfaces



Connect IP cores of different interfaces using Qsys. AXI will be supported in a future version, as will additional interfaces.

Migration Flow from SOPC Builder to Qsys

Qsys offers a migration flow to convert SOPC Builder designs to Qsys. For more information, refer to **AN632: SOPC Builder to Qsys Migration Guidelines**

Want to Dig Deeper?

To learn more about Qsys, visit www.altera.com/qsys to:

- View Qsys webcasts
- View short Qsys online video demos
- Download the Qsys tutorial
- Read the white paper: **Applying the Benefits of Network on a Chip Architecture to FPGA System Design (PDF)**

And much more!

Altera Corporation

101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters

Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 94 602 000

Altera Japan Ltd.

Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.

Unit 11-18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2945 7000

