



Altera's 28-nm, Power-Efficient Transceivers

Altera® transceivers have a proven track record of meeting system bandwidth, power, and bit-error rate (BER) requirements. You'll find the same technology leadership advantages in our 28-nm Stratix® V FPGA transceivers.

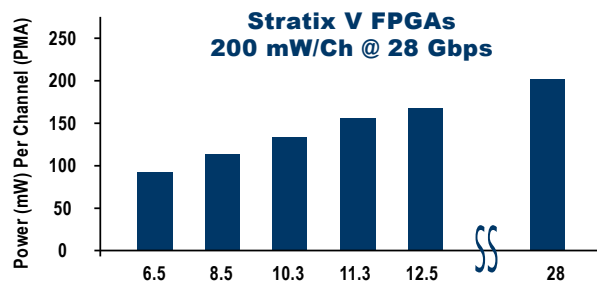
Stratix V FPGAs feature up to 66 full-duplex transceiver channels (physical media attachment (PMA) and physical coding sublayer (PCS)) and transceivers at data rates from 600 Mbps to 28 Gbps.

Providing up to 825 Gbps of transceiver bandwidth, Stratix V FPGAs deliver the highest system bandwidth at the lowest power consumption for a wide range of applications and protocols. In addition, the transceivers are compliant with a range of protocols, and are equipped with a variety of signal conditioning features to support backplane, optical module, and chip-to-chip applications.

Transceiver PMA Features

Feature	Stratix V FPGA
Data rates	20 Gbps – 28 Gbps (GT); 600 Mbps – 12.5 Gbps (GT and GX); 600 Mbps – 12.5 Gbps (GS)
Backplane support	Up to 12.5 Gbps, including 10GBASE-KR
Optical module support	10G form-factor pluggable (XFP), small form-factor pluggable (SFP+), quad small form-factor pluggable (QSFP), CXP, 100G pluggable (CFP), 100G form-factor pluggable
Architecture	Independent transmit/receive channels; full PMA+PCS on all channels
Receive clocking	Analog PLL-based CDR per receive channel
Transmit clocking	fPLL (up to 3.75 Gbps); CMU (full range); programmable LC (3.25 - 12.5 Gbps, 20 - 28 Gbps)
Continuous time linear equalization (CTLE)	Receiver 4-stage linear equalization for high-attenuation channels
Adaptive dispersion compensation engine (ADCE)	Adaptive engine that automatically adjusts CTLE to compensate for changes over time
Decision feedback equalization (DFE)	Receiver 5-tap digital equalizer to minimize losses and crosstalk
Phase-locked loop (PLL-) based clock recovery	Superior jitter tolerance versus phase interpolation techniques
Transmit equalization (pre-emphasis)	Transmit driver 4-tap pre-emphasis and de-emphasis for protocol compliance under lossy conditions

Transceiver PMA Power Per Channel



Lowest Jitter for Best-in-Class Reliability

Stratix V transceivers provide best-in-class system reliability with the lowest jitter. Transmit and receive advanced equalization capabilities fully support 10GBASE-KR backplanes at the lowest BER.

With careful die/package co-design, the transceivers won't be impacted by core and I/O noise, which ensures optimal signal and power integrity.

Clocking Flexibility

Reference clocks are derived from off-chip oscillators, or generated on chip with the precise frequency synthesis capabilities of the new fractional PLLs (fPLLs). fPLLs synthesize fractional multiple clock frequencies from a single reference clock source, and replace multiple reference oscillators in multi-protocol or multi-rate applications.

Providing more independent channels than ever before, each transmit channel can be clocked by:

- An LC oscillator, which provides very low random jitter, in the range of sub-pico-seconds (RMS).
- A ring oscillator derived from a clock multiplication unit (CMU) channel, which can also be used as a transceiver.
- The new fPLL, a PLL in the core fabric that also replaces external voltage-controlled crystal oscillators (VCXOs) on the board.

EyeQ Feature Examines Transceiver Link Quality

After board layout, it's challenging to measure the quality of the transceiver link in your design at high data rates. Stratix V FPGAs feature the updated EyeQ eye viewer, which completely reconstructs the vertical and horizontal eye opening after equalization and clock recovery in the receiver. The EyeQ on-die instrumentation can be used non-invasively to tune for ideal equalization coefficient settings, or to debug a transceiver link when combined with dynamic reconfiguration.

Transceiver Simulation and Link Analysis

Altera offers a comprehensive suite of simulation tools and models to help you optimize the transceiver for your application. For a higher level system circuit simulation on Altera devices, tap into our transceiver HPSICE models and behavioral IBIS-AMI models for complete link analysis and board design

Our pre-emphasis and equalization link estimator (PELE) provides optimal transmit and receive equalization coefficients. Our link analysis tool estimates the jitter performance on characterized data to ensure that a high-speed serial link will interoperate at the target BER.

Want to Dig Deeper?

Learn more about Stratix V transceiver technology by meeting with your local Altera sales representative or FAE, or visiting www.altera.com/stratix5.

Key Protocol Support

Standard	Electrical Serial Line Rate
OIF/CEI 28G-SR	25/28 Gbps
IEEE 802.3ba 40G/100G 10GBASE-R/10GBASE-KR	10.3125 Gbps
OIF SFI-S/SFI-5.2 (40G)	9.95 to 11.1 Gbps
10G Interlaken	10.6921 Gbps
SONET/SDH OC-192 (10G/40G)	9.95 Gbps
SFP+	8.5 to 11.32 Gbps
XFP	9.95328 to 11.32 Gbps
OIF/CEI 11G-SR and LR	9.95 to 11.1 Gbps
OTU2/OTU3/OTU4	10.709/10.7545/11.2 Gbps
10G SDI	10.6921 Gbps
QDR InfiniBand	10 Gbps
PCI-E 3.0/2.0/1.0	8/5/2.5 Gbps
Interlaken	4.976 to 6.375 Gbps
SRIO 2.0+	1.25, 2.5, 3.125, 5 to 6.25
SATA 3.0/SAS 2.0	6 Gbps
QPI	4, 4, 8, 6.4, 8 Gbps
HyperTransport™ 3.0+	0.4, 2.4, 2.8, 3.2 Gbps
HighGig+, HighGig2+	3.75, 6.25 Gbps
Fibre Channel (8G/4G)	8.5 Gbps/4.25 Gbps
OIF/CEI 6G-SR	4.976 to 6.375 Gbps
XAUI	3.125 Gbps
SFI-4.2 (10G)/SFI-5.1 (40G)	3.125 Gbps

Stratix V transceiver FPGAs address all of the protocols listed in the table above, including hardened implementations of PCI Express Gen3/Gen2/Gen1, CEI-6G, XAUI, and Gigabit Ethernet.

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