Arria GX Development Board

Reference Manual

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

About this Manual

Revision History

The table below displays the revision history for the chapters in this reference manual.

Chapter	Date	Version	Changes Made
1	October 2007	1.0.0	• First publication.

This reference manual provides comprehensive information about the Altera® Arria™ GX development board.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Information Type	Contact *Note (1)*
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
Technical training services	custrain@altera.com
Product literature	www.altera.com/literature
Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. Overview

Introduction

This document describes the hardware features of the Arria™ GX development board, including detailed pinout information to enable designers to create custom FPGA designs that interface with all components of the board.

For information on setting up and powering up the Arria GX development board and using the kit's demo software, please refer to the *Arria GX Development Kit Getting Started User Guide*.

General Description

The Arria GX development board provides a hardware platform for developing and prototyping high-performance PCI Express (PCIe)-based designs as well as to demonstrate the Arria GX device's embedded transceiver and memory interface circuitry.

With up to 8-integrated transceiver channels and support for high-speed, low latency memory access via a DDR2 SDRAM memory interface, the Arria GX development board provides a fully-integrated solution for multi-channel, high-performance applications, while also using limited board space.

The Arria GX transceivers are optimized for endpoint and bridging applications. Through the use of Altera® MegaCore® functions (or other intellectual property [IP] cores) and expansion connectors, you can enable the inter-operability of the Arria GX device's transceivers with third-party application specific semiconductor products (ASSP) for either point-to-point switching or bridging applications.

To simplify the design process, Altera provides a PCIe reference design—available from the Altera website—for use as either a design starting point or as an experimental platform. The PCIe reference design has been verified by Altera engineers and is distributed with the *Arria GX Development Kit* (ordering code: DK-DEV-1AGX60N).

The Arria GX development board is a PCI-Special Interest Group (SIG) compliant board.

The Arria GX development board has the following main features:

- Arria GX EP1AGX60 chip in a 780-pin flip-chip FineLine BGA® (FBGA) package
- PCIe x4 interface
- An Altera High Speed Mezzanine Card (HSMC)
- 32-MByte x 16 DDR2 SDRAM operating at 233 MHz
- Two user push-button switches (and one that is also used as a global reset)
- Eight user LEDs
- One octal user DIP switch
- Re-programmability with dedicated circuitry to perform the following Arria GX configuration schemes: fast passive parallel (FPP), passive serial (PS), and compressed FPP

Board Component Blocks

The board features the following component blocks:

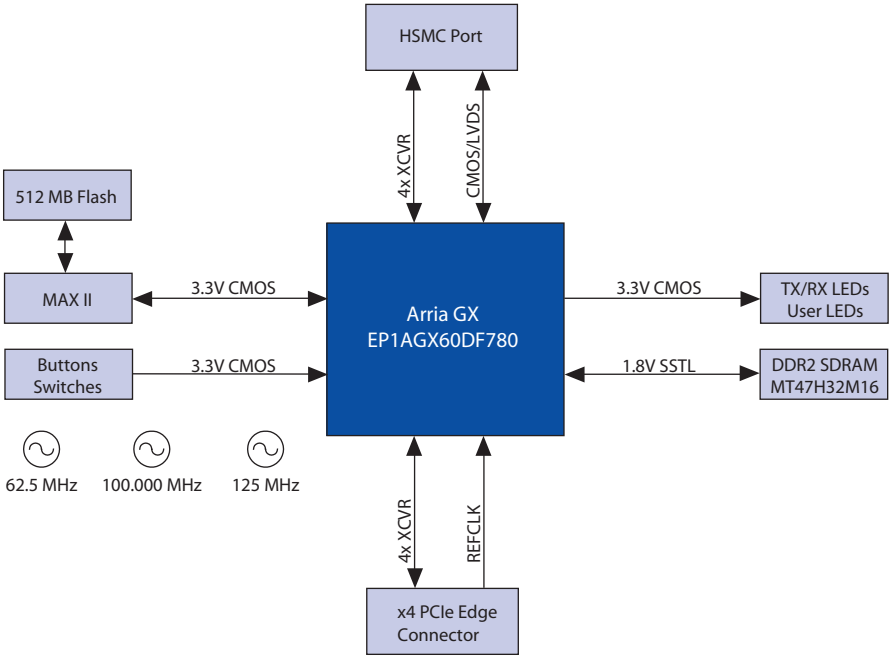
- 780-pin Altera Arria GX EP1AGX60 FPGA
  - 60K logic elements (LEs)
  - Eight transceiver channels
  - 128 18 X 18 multiplier blocks
  - Four phase locked loops (PLLs)
  - 395 user I/Os
- Transceiver interfaces
  - x4 PCI Express edge connector
  - One HSMC with four transceivers
- FPGA configuration circuitry
  - JTAG interface
  - MAX® II CPLD and 16-bit page mode flash memory
- Clocking circuitry
  - The Arria GX development board uses three clock oscillators on the transceivers and user logic to support all Arria GX device protocols:
    - 62.5 MHz
    - 100.00 MHz
    - 125.00 MHz
  - PCI Express clock input
  - SMA connector for external clock input and output
- General user and configuration interfaces
  - LEDs:
    - Two LEDs indicating PCIe x1 or x4 mode
    - One transmit and one receive (TX/RX) LED for the PCIe transceiver interface
    - One transmit and one receive (TX/RX) LED for the HSMC transceiver interface

        - One HSMC present LED
        - Eight user LEDs
        - One configuration done LED
        - One power LED
        - Power good status LEDs
      - Push-buttons:
        - One user reset push-button
        - One configuration push-button
        - Two general user push-buttons
      - DIP switches:
        - One user DIP switch
        - One configuration DIP switch
      - Two slider switches for JTAG chain control
  - Power supply
    - PCI Express power input
    - External IBM laptop compatible DC input
    - Power multiplexer that allows the load to be shared by both the external supply and by the PCIe slot.
    - Temperature sensing device and fan control circuit
  - Mechanical
    - PCI Express short form factor (four 3.76 "x 6.600")

Block Diagram

Figure 1–1 shows the functional block diagram of the Arria GX development board.

Figure 1–1. Arria GX Development Board Block Diagram



Handling the Board

When handling the board it is important to observe the following precaution:

CAUTION

Static Discharge Precaution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precaution when touching the board.

2. Board Components

Introduction

This chapter introduces all the important components on the Arria™ GX development board. Figure 2–1 illustrates all component locations and Table 2–1 describes component features.

The chapter is divided into the following sections:

- Featured device
- Configuration
- Clocking circuitry
- User interface components
- Off-chip memory
- Standard communication ports
- Power supply
- Temperature sensor
- Heat sink and fan

A complete set of board schematics, a physical layout database, and GERBER files for the Arria GX development board are installed in the *Arria GX Development Kit* documents directory.

For information on powering up the development board and installing the demo software, refer to the *Arria GX Development Kit Getting Started User Guide*.

Board Overview

This section provides an overview of the Arria GX development board, including an annotated board image and component descriptions.

Figure 2–1 shows the top view of the Arria GX development board.

Figure 2–1. Top View of the Arria GX Development Board

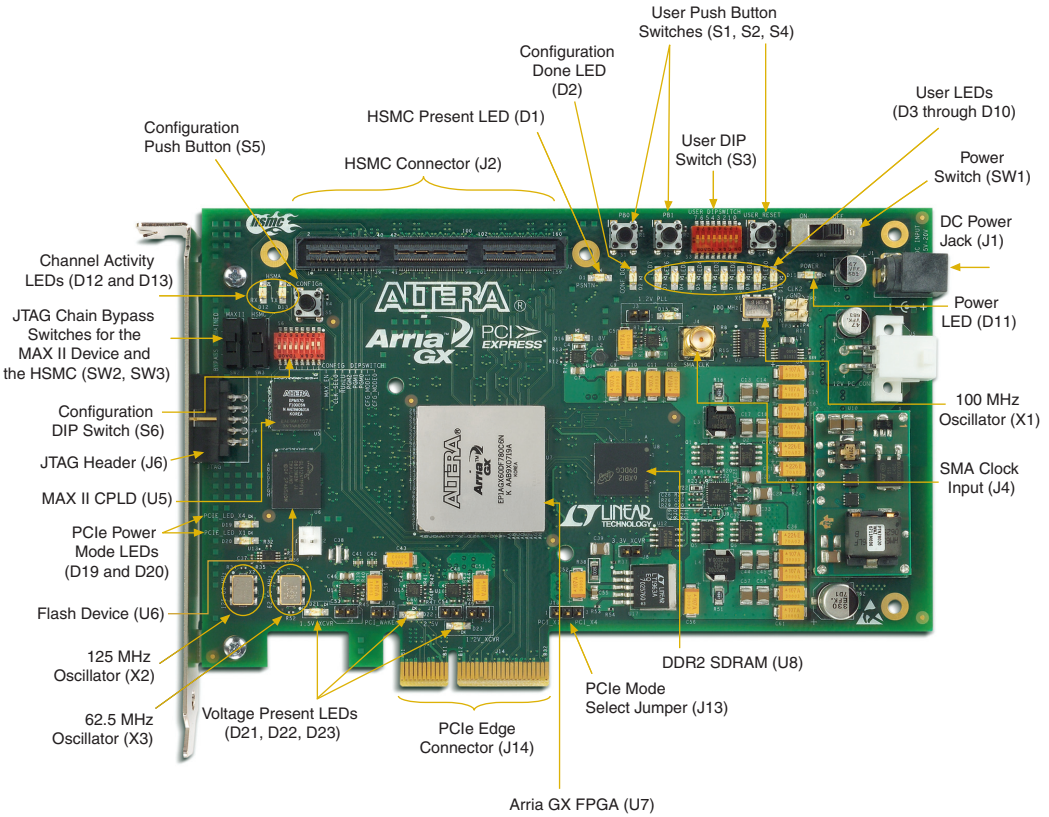


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Board Components & Interfaces (Part 1 of 2)

Board Reference	Name	Description
Featured Device		
U7	Arria GX FPGA	EP1AGX60D FPGA in a 780-pin flip-chip FineLine BGA® (FBGA) package.
Configuration Status and Setup Elements		
S6	Board configuration DIP switch	DIP switch that controls the FPGA and MAX II device configuration settings.
D19 and D20	PCIe mode LEDs	Yellow LEDs that display PCIe x1 or x4 mode.
D2	Configuration done LED	Green LED that displays configuration status.
D12 and D13	Channel activity LEDs	Yellow LEDs that indicate the RX and TX activity on HSMC Port A.
D11	Power LED	Blue LED indicates when power is applied to the board.
D21, D22, D23	Voltage present LEDs	Green LEDs that indicate the presence of 1.5 V, 2.5 V, and 1.2 V power.
S5	Configuration push button	Push button to reconfigure the Arria GX device.
SW2, SW3	JTAG chain bypass switches	Switches to include or exclude HSMC Port A and MAX II from the JTAG chain.
D1	HSMC present LED	Green LED indicates when an HSMC card is connected.
J6	JTAG header	10-pin header for JTAG-based FPGA communication.
Clocks		
X1	100 MHz	100-MHz oscillator
X2	125 MHz	125-MHz oscillator
X3	62.5 MHz	62.5-MHz oscillator
J4	SMA clock input	SMA connector that allows the provision of an external clock.
General User Input/Output		
S1, S2, S4	User push-button switches	User-defined push-button switches.
D3-D10	User LEDs	Eight user-defined LEDs.
S3	User DIP switch	User-defined DIP switches.
Memory Devices		
U8	DDR2 SDRAM	32 M x16 of DDR2 SDRAM
U6	Flash	512 Mbits of flash memory

Table 2–1. Board Components & Interfaces (Part 2 of 2)

Board Reference	Name	Description
Components and Interfaces		
J14	PCIe edge connector	A x4 (4 channel) PCI Express edge connector for insertion into PCI Express-based host platforms.
J13	PCIe mode select jumper	Indicates to the host controlling the Arria GX development board if the card is operating in either PCIe x1 or PCIe x4 mode.
J2	HSMC interface	High speed mezzanine connector allows for the connection of HSMC daughter cards.
Power		
J1	DC power jack	DC input connector for the board
SW1	Power switch *(1)*	Slide switch that enables power to the board.

Note to Table 2–1:
(1) Power switch is bypassed when the board is plugged into a PCI slot.

Featured Device

The *Arria GX Development Kit* features the EP1AGX60DF780 FPGA (U7) in a 780-pin flip-chip FineLine BGA® (FBGA) package. Table 2–2 lists some Arria GX device features.

Table 2–2. Arria GX Features

Architectural Feature	Results
The Altera® low-cost, protocol-specific, transceiver-based FPGA	• Provides a low-cost, transceiver-based design solution for the most popular high-speed serial interfaces • Provides optimum jitter performance across the entire operating range of 1.25 Gbps to 2.5 Gbps • Provides best-in class signal integrity performance
Innovative clock management system	• Clock signals are automatically routed to the appropriate destination • Greatly simplifies high-speed board designs

I/O & Clocking Resources

This section lists specific I/O and clocking resources available on EP1AGX60DF780 device.

Figure 2–2 illustrates the available I/O mapping on the EP1AGX60DF780 device.

Figure 2–2. Arria GX Device I/O Mapping Resources

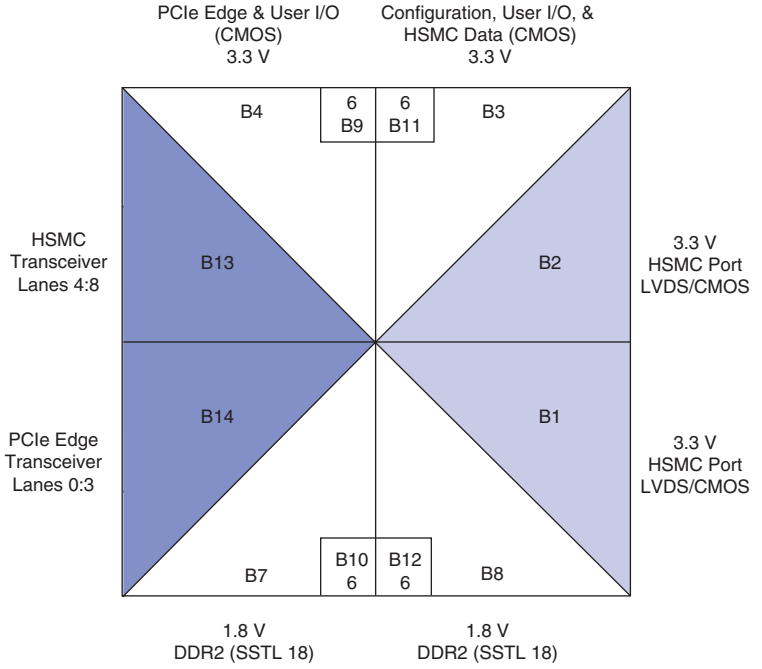
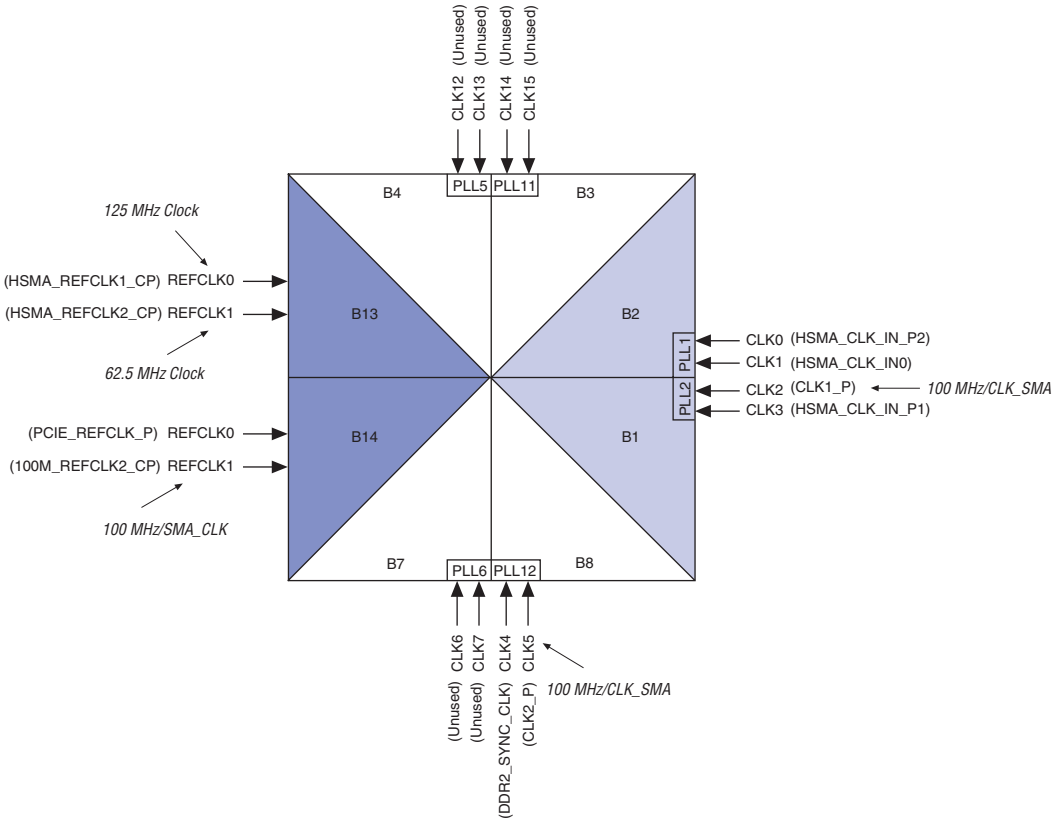


Figure 2–3 illustrates the clocking resources for the EP1AGX60DF780 device. The parenthetical text refers to board-level signals as they relate to specific clock pin names noted in both the *Quartus® II Development Software Handbook* and the *Arria GX Device Handbook*.

Figure 2–3. Arria GX Device Clocking Resources



Configuration Schemes

The Arria GX device is configured using the on-board MAX II complex programmable logic device (CPLD) and a 16-bit page-mode flash memory device.

The 512 Mb flash memory device can hold eight designs, where each design is 16,951,824 bits in size for the EP1AGX60DF780 device plus 32 MBytes for other storage.

This section discusses:

- JTAG chain configuration
- Flash memory configuration
- MAX II configuration controller
- Configuration push button

Table 2–3 shows the Arria GX development board's configuration parts list.

Table 2–3. Arria GX Development Board's Configuration Parts List

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Web Site
U5	MAX II CPLD	Altera	EPM570F100C5N	www.altera.com
U6	512 Mbit flash memory	Spansion LLC	S29GL512N	www.spansion.com
J6	JTAG connector	Molex	70247-1051	www.molex.com
SW2,SW3	Slider switch (SPDT) for JTAG chain MAX II and HSMC bypass/chain selection.	E-switch	EG1903-ND	www.e-switch.com
S6	8-position DIP switch for configuration setting.	C&K Components/ITT Industries	TDA08H0SK1	www.ittcannon.com

Figure 2–4 shows the Arria GX configuration scheme.

Figure 2–4. Arria GX Configuration Scheme

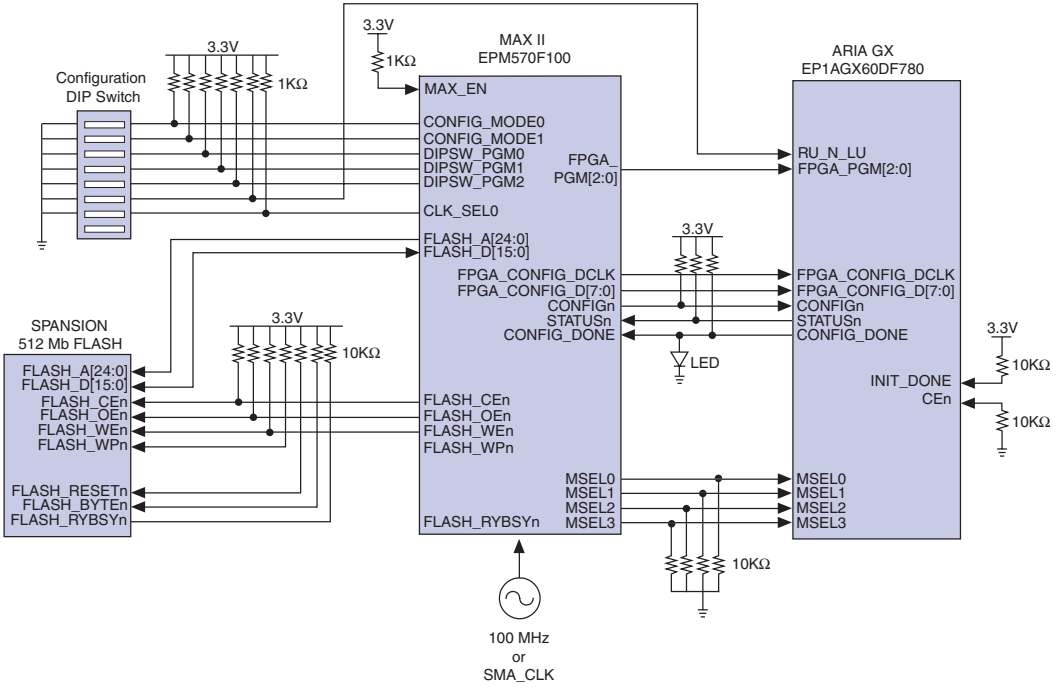


Table 2–4 lists the supported configuration modes and settings. The `MSEL[3:0]` bits are set using the MAX II device. The `CFG_MODE[1:0]` pins must be set on the configuration DIP switch.

Table 2–4. Supported Configuration Modes & Settings, Note (1)

Configuration Scheme	FPGA MSEL Settings (from MAX II Device)				DIP Switch Settings	
	MSEL-3	MSEL-2	MSEL-1	MSEL-0	CFG_MODE-1	CFG_MODE-0
Fast passive parallel (FPP)	0	0	0	0	0	0
Remote system upgrade FPP, *(2)*	0	1	0	0	0	1
FPP with decompression	1	0	1	1	1	0

Table 2–4. Supported Configuration Modes & Settings, Note (1)

Configuration Scheme	FPGA MSEL Settings (from MAX II Device)				DIP Switch Settings	
	MSEL-3	MSEL-2	MSEL-1	MSEL-0	CFG_MODE-1	CFG_MODE-0
RSU with FPP decompression	1	1	0	0	1	1
JTAG *(3)*	N/A	N/A	N/A	N/A	N/A	N/A

Notes to Table 2–4:
(1) The MSEL bits are auto-generated by the MAX II device's configuration design.
(2) Remote system upgrade uses FPGA PGM [2:0] outputs page select pins.
(3) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

Two single-pole, double throw switches are used to select JTAG chain options, refer to "JTAG Chain Configuration" on page 2–9 for more information.

JTAG Chain Configuration

The simplest way to configure the Arria GX device is with the JTAG configuration scheme. The JTAG configuration scheme requires just the USB-Blaster™ cable and the Quartus® II Software.

To setup JTAG configuration, connect one end of the USB-Blaster cable to the computer's USB port and the other end to the 10-pin JTAG header on the board. To download a design file to the Arria GX device, use the Quartus II Programmer.

For information on the Quartus II Programmer, refer to *Quartus II Development Software Handbook*.

The board's JTAG chain is connected to the Arria GX device and optionally the MAX II CPLD, as well as the HSMC expansion connector. The MAX II and HSMC slots are by-passable so that devices on the mezzanine card can be optionally addressed through JTAG.

The MAX II device and HSMC interface can be by-passed or chained together via board references SW2 and SW3 respectively.

To configure the Arria GX device, you must perform the following steps:

1. Set up a new JTAG chain (including both the MAX II CPLD and the Arria GX device)

2. Set SW2 and SW3 to add or remove either the HSMC expansion connector or MAX II device from the JTAG chain.

Figure 2–5 shows the JTAG chain connections.

Figure 2–5. JTAG Chain Connections

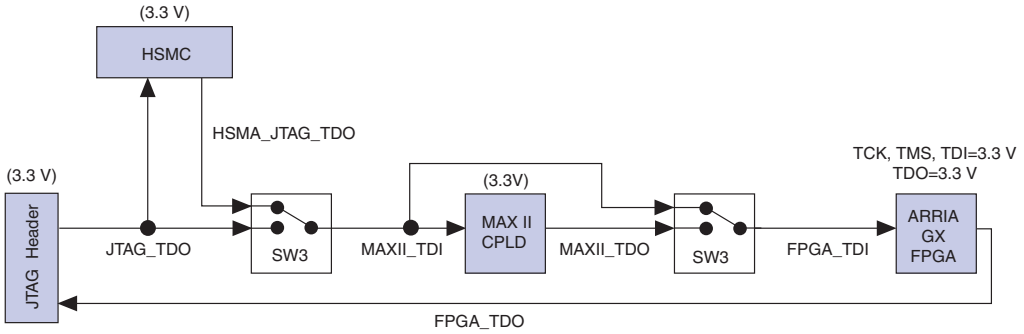


Table 2–5 shows the JTAG chain signals.

Table 2–5. JTAG Chain I/O Signals *Note (1)*

Signal Name	Description
JTAG_TCK	JTAG clock (USB-Blaster output)
JTAG_TMS	JTAG mode select (USB-Blaster output)
JTAG_TDO	Data input (USB-Blaster output)
FPGA_TDO	Data output (USB-Blaster input)
HSMA_TDO	HSMC data output
MAXII_TDI	MAX II data input
MAXII_TDO	MAX II data output
FPGA_TDI	Arria GX device data input
FPGA_TDO	Arria GX data output (USB Blaster input)

Note to Table 2–5:
(1) All signals are LVTTL.

For more information about programming Altera devices, refer to the Altera Configuration Handbook.

Flash Memory Configuration

A 512-Mb Spansion flash memory device is used to store configuration files for the FPGA as well as any other necessary data. The target device is a Spansion S29GL512N in a BGA package, which supports CFI flash commands.

The flash memory map is determined by the MAX II CPLD design, which is based on the Parallel Flash Loader (PFL) megafunction. The PFL megafunction takes up to eight Quartus II programmer object files (**.pof**) and stacks them into a single image to be written to flash memory using the Quartus II Programmer and a USB-Blaster cable. This is done via the JTAG header and the MAX II CPLD to flash memory.

Table 2–6 lists an example flash memory map. The sizes of various blocks may change based on the settings used, such as the compression setting, in the Quartus II Programmer. The PFL Option Bits are used by the MAX II CPLD design to store the address of the POF files.

Table 2–6. Example Flash Memory Map

Memory Block	Address
PFL option bits (Not negotiable in address and size)	0x3FF0000 0x3FF0080
User space (16MB-32MB)	0x03FF.FFEF 0x0200.0000
FPGA design 7	0x01FF.FFFF 0x01C0.0000
FPGA design 6	0x01BF.FFFF 0x0180.0000
FPGA design 5	0x017F.FFFF 0x0140.0000
FPGA design 4	0x013F.FFFF 0x0100.0000
FPGA design 3	0x00FF.FFFF 0x00C0.0000
FPGA design 2	0x00BF.FFFF 0x0080.0000
FPGA design 1	0x007F.FFFF 0x0040.0000
FPGA design 0 *(default)*	0x003F.FFFF 0x0000.0000

Table 2–7 lists the required signals for the flash memory. Flash signals are routed from the Spansion flash device to the MAX II device. The required signals are then routed from the MAX II device to the Arria GX device (see Figure 2–4). Signal directions are relative to the MAX II device as far as direction and signaling standard.

Table 2–7. Flash Interface I/O

MAX II Pin Numbers	Schematic Signal Name	Description	Signal Type
K2,K3,H4,J4,K4, J5,K5,K6, J6,K7, K8,H7,J8,H8,K10, J9,H9,J10,H10,G8 G9,G10,F10,F9	FLASH_A(24:0)	Address bus	3.3-V CMOS out (25 bit)
C2,B1,C1,D3,D2, D1,E3,F2,F3,F1, G1,H1,G2,G3,K1, J3	FLASH_D(15:0)	Data bus	3.3-V CMOS in/out (16 bit)
F2	FLASH_CEn	Chip enable	3.3-V CMOS out
B5	FLASH_RESETn	Reset	N/A (Tie to VCC)
G2	FLASH_OEn	Output enable	3.3-V CMOS out
A5	FLASH_WEn	Write enable	3.3-V CMOS out
B4	FLASH_WPn	Write protect	N/A (Tie to VCC)
A4	FLASH_RDYBSYn	Ready/not busy	No connect (Tie to VCC)
F7	FLASH_BYTEn	Byte/word select	N/A (Tie to VCC)
	VIO	I/O power	3.3-V
	VCC	Core power	3.3-V
	VSS	Ground	Ground

Table 2–8 shows configuration file sizes for the Arria GX device.

Table 2–8. Configuration File Sizes

Device	Configuration File Size (Mb)
EP1AGX60DF780C6N	16,951,824

Table 2–9 lists the flash memory component reference and manufacturing information.

Table 2–9. Flash Memory Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U6	Flash memory	Spansion	S29GL512N	www.spansion.com

MAX II CPLD Configuration Controller

The MAX II CPLD is primarily used for FPGA configuration and flash programming. The target MAX II device is an EPM570 in a 100 ball FBGA. The PFL megafunction is the basis for the MAX II CPLD design.

The MAX II CPLD is part of the board's JTAG chain and can be programmed using the Quartus II Programmer and a USB-Blaster cable. The same JTAG interface is also used to program flash images.

Table 2–10 lists the required MAX II CPLD signals and the corresponding PFL megafunction design I/O requirements. Signal directions are relative to the MAX II CPLD as far as direction and signaling standard.

Table 2–10. MAX II CPLD Signals & I/O Requirements (Part 1 of 2)

MAX II Pin Numbers	Schematic Signal Name	Description	Signal Type
C9	FPGA_CONFIG_DCLK	Configuration clock	3.3-V CMOS out
A7,A6,B6,A5,B5,A4, B4,C4	FPGA_CONFIG_D(7:0)	Configuration data bus	3.3-V CMOS out
D8	CONF_DONE	FPGA CONF_DONE pin connection	3.3-V CMOS in
D9	CONFIGn	FPGA nCONFIG pin connection	3.3-V CMOS out
B10	STATUSn	FPGA nSTATUS pin connection	3.3-V CMOS in
K2,K3,H4,J4,K4, J5,K5,K6,J6,K7,K8, H7,J8,H8,K10,J9, H9,J10,H10,G8,G9, G10,F10,F9	FLASH_A(24:0)	Flash address bus	3.3-V CMOS out
C2,B1,C1,D3,D2, D1,E3,F2,F3,F1, G1,H1,G2,G3,K1,J3	FLASH_D (15:0)	Flash data bus	3.3-V CMOS in/out
F2	FLASH_CEn	Flash chip enable	3.3-V CMOS out

Table 2–10. MAX II CPLD Signals & I/O Requirements (Part 2 of 2)

MAX II Pin Numbers	Schematic Signal Name	Description	Signal Type
G2	FLASH_OEn	Flash output enable	3.3-V CMOS out
A5	FLASH_WEn	Flash write enable	3.3-V CMOS out
A1,B2	CONFIG_MODE(1:0)	Configuration mode input	3.3-V CMOS in
A3,A2,B3,C3	MSEL(3:0)	FPGA mode select output	3.3-V CMOS out
E2	MAX_EN	Enables operation for PFL	3.3-V CMOS in
A9,B6,A8	FPGA_PGM(2:0)	Remote configuration page select	3.3-V CMOS in
C8,B9,A10	DIPSW_PGM(2:0)	DIP switch configuration page select	3.3-V CMOS in
E1,E2	MAXII_CLK_IN	100-MHz clock input	3.3-V CMOS in
J1	TMS	JTAG mode select	N/A
H2	TDI	JTAG data in	N/A
J2	TDO	JTAG data out	N/A
H3	TCK	JTAG clock	N/A
	VCCIO1	I/O bank 1 power	3.3 V
	VCCIO2	I/O bank 2 power	3.3 V
	VCCINT	Core power	3.3 V
	GNDIO	I/O GND	GND
	GNDINT	Core GND	GND

Configuration Push Button (S5)

Board reference S5 is a push-button with a direct connection to the Arria GX device's CONFIGn signal that—upon pressing to drive low—forces a reconfiguration of the FPGA from the on board flash memory. The Arria GX device's pin name associated with the CONFIGn signal is V16.

Pushing the S5 switch causes the FPGA to reload a configuration from the on-board flash device.

Clocking Circuitry

Three oscillators of 62.5 MHz, 100 MHz, and 125 MHz are used to clock the Arria GX transceivers and user logic.

When the board is not plugged into a host, the 100-MHz oscillator is used to support the transceiver reference clock for PCIe applications. Figure 2–6 shows the oscillator driving through a four-output LVDS buffer to a variety of loads. The buffer can either be driven from the 100-MHz oscillator or from the SMA clock input for custom frequencies or "frequency sweeping" of F_{MAX} performance.

The CLK_SEL0 pin on the board configuration DIP switch controls what clock feeds the buffer. See "Configuration DIP Switch (S6)" on page 2–19.

The 62.5 MHz and 125 MHz oscillators ensure that all protocols supported by the Arria GX device are provided for.

Table 2–11 lists the Arria GX development board's clocking parts list.

Table 2–11. Arria GX Development Board's Clocking Parts List

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Web Site
X3	62.5 MHz LVDS oscillator	Pletronics	LV7745DEV-62.50M	www.pletronics.com
X2	125.00 MHz LVDS oscillator	Pletronics	LV7745DEV-125.000M	www.pletronics.com
X1	100.00 MHz LVDS oscillator	Pletronics	LV7745DEV-100.000M	www.pletronics.com
J4	SMA for external clock input	Lighthorse Technologies Inc.	LTI-SASF546-P26-X1	www.rfconnector.com
U2	1-to-4 differential-to-LVDS clock buffer	IDT	ICS8543	www.idt.com
U4	1-to-2 differential-to-single ended clock buffer	IDT	ICS83026	www.idt.com

Figure 2–6 shows the oscillator clocking diagram.

Figure 2–6. Oscillator Clocking Diagram

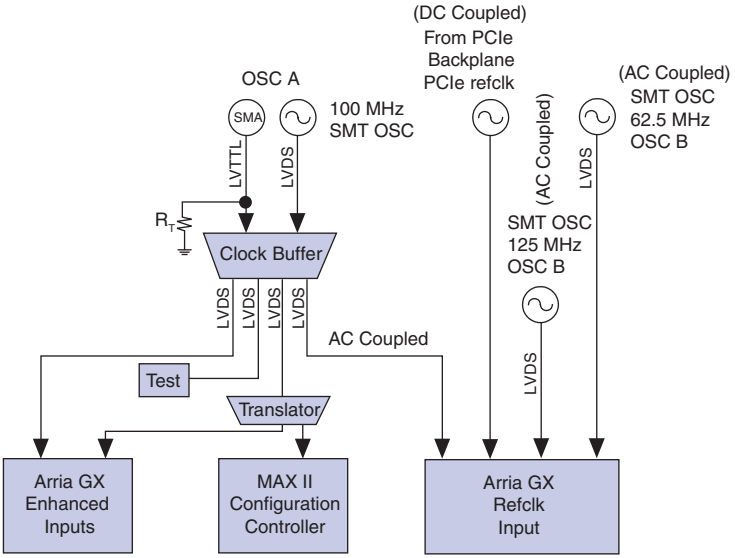


Table 2–12 lists the board's clock distribution system.

Table 2–12. Arria GX Development Board Clock Distribution (Part 1 of 2)

Source	Schematic Signal Name	I/O Standard	Arria GX Pin Number	MAX II Pin Number
100 MHz (X1) oscillator or SMA clock input (J4) *(1)*	CLK1_P	Not terminated LVDS	U28	
	CLK1_N		U27	
	CLK2_P*(2)*	LVDS		
	CLK2_N*(2)*			
	100M_REFCLK_P	Not terminated LVDS	AB4	
	100M_REFCLK_N		AB5	
	CLK2	3.3 V	AC15	
	MAXII_CLK_IN	3.3 V		E1
62.5 MHz oscillator (X3)	HSMA_REFCLK2_P	LVDS	G4	
	HSMA_REFCLK2_N		G5	

Table 2–12. Arria GX Development Board Clock Distribution (Part 2 of 2)

Source	Schematic Signal Name	I/O Standard	Arria GX Pin Number	MAX II Pin Number
125 MHz oscillator (X2)	HSMA_REFCLK1_P	LVDS	J1	
	HSMA_REFCLK1_N		J2	

Notes to Table 2–12:
(1) Select between using the 100 MHz oscillator or the SM_CLK using CLK_SEL on the configuration DIP switch (S6). Pin 7 in the 0n position selects SMA_CLK.
(2) CLK2_P and CLK2_N are connected to TP3 and TP4 respectively.

General User Interfaces

To allow you to fully leverage the I/O capabilities of the Arria GX device for debugging, control, and monitoring purposes, the following general user interfaces are available on the board:

- Push buttons
- User DIP switch
- User LEDs
- Board-specific DIP switch
- Board-specific LEDs
- Status LEDs

Push Button Switches (S1, S2, S4)

Board references S1, S2, and S4 are push-buttons allowing general user I/O interfaces to the Arria GX device.

The push buttons connect directly to user I/O pins for user programming. Although the USER_RESET push button's purpose is programming, its special label is intended to encourage its use as a logic reset signal for FPGA designs so that user designs are reset in a consistent manner.

All push buttons are a logic 1 until depressed.

Table 2–13 lists the board references, schematic signal names and corresponding Arria GX pin numbers.

Table 2–13. Push-Button Switch Signal Names and Functions (Part 1 of 2)

Board Reference	Schematic Signal Name	Arria GX Pin Number
S1	USER_PB0	A19

Table 2–13. Push-Button Switch Signal Names and Functions (Part 2 of 2)		
Board Reference	**Schematic Signal Name**	**Arria GX Pin Number**
S2	USER_PB1	B19
S4	USER_RESET	AE17

Pin AE17 is the DEV_CLRn pin; when enabled in the Quartus II software, it will reset all Arria GX device registers. The USER_RESET push button is board reference S4. Pin AE17 can also be used as a standard input.

User-Defined DIP Switch (S3)

Board reference S3 is an eight-pin DIP switch. The DIP switches in S3 are user-defined, and are provided for additional FPGA input control. Each pin can be set to a logic 0 by setting it to the closed position, and each pin can be set to logic 1 by setting it to the open position.

Table 2–14 lists the DIP switch settings, schematic signal name, and corresponding Arria GX device's pin number.

Table 2–14. User-Defined DIP Switch Pin-Out (S3)		
S3 Switch	**Schematic Signal Name**	**Arria GX Device Pin**
1	USER_DIPSW0	C21
2	USER_DIPSW1	A21
3	USER_DIPSW2	B20
4	USER_DIPSW3	C20
5	USER_DIPSW4	B23
6	USER_DIPSW5	C23
7	USER_DIPSW6	B25
8	USER_DIPSW7	C25

User LEDs (D9 Through D16)

The board provides eight user-defined LEDs. A logic 0 driven to an LED turns it On; a logic 1 driven to an LED turns it Off.

Table 2–15 lists the schematic signal name and the corresponding Arria GX device's pin number.

Table 2–15. User-Defined LED Pin-Out

Board Reference	Schematic Signal Name	Arria GX Device Pin Number
D9	USER_LED0	A12
D10	USER_LED1	A11
D11	USER_LED2	C13
D12	USER_LED3	B13
D13	USER_LED4	A13
D14	USER_LED5	B14
D15	USER_LED6	C14
D16	USER_LED7	C12

Configuration DIP Switch (S6)

The configuration DIP switch is used to set up specific board functions, such as FPGA bootstrap settings, configuration, or clock selection setup. In the On position, the selected signal is driven to logic 0. In the Off position, the selected signal is driven to a logic 1.

Table 2–16 shows the configuration DIP switch (S6) signal names and descriptions.

Table 2–16. Configuration DIP Switch Signal Name, Description, MAX II Device Pin Number (Part 1 of 2)

Schematic Signal Name	Description	MAX II Device Pin Number
CONFIG_MODE0	Configuration mode - bit 0	A1
CONFIG_MODE1	Configuration mode - bit 1	B2
DIPSW_PGM0	Configuration file page select - bit 0	C8
DIPSW_PGM1	Configuration file page select - bit 1	B9
DIPSW_PGM2	Configuration file page select - bit 2	A10
RUnLU	Remote/local configuration mode	Connected to ACI6 of the Arria GX device.

Table 2–16. Configuration DIP Switch Signal Name, Description, MAX II Device Pin Number (Part 2 of 2)		
Schematic Signal Name	**Description**	**MAX II Device Pin Number**
CLK_SEL0	Local oscillator / SMA input select (on = local oscillator)	C7
MAX_EN	Enables the PFL	F2

Board-Specific LEDs

This section describes the board-specific LEDs. In addition to the user-defined LEDs, the board provides a set of 4 yellow LEDs (2 per interface). These board-specified LEDs display FPGA transceiver channel activity (or traffic) for both TX and RX signals.

Table 2–17 shows the channels needing TX and RX LEDs.

Table 2–17. FPGA Transceiver Interface LEDs		
Number	**Transceiver Interface Indicator**	**LED Color**
1	PCIe edge connector (L0x1, L0x4)	Yellow
2	HSMC interface (TX & RX)	Yellow

Status and Channel Activity LEDs

The board provides status and channel activity LEDs, which indicate successful configuration, power-on status, connection to the HSMC expansion connector, etc.

Tables 2–18 lists the board status LEDs.

Table 2–18. Board Status LEDs		
Board Reference Number	**Transceiver Interface Indicators**	**Color**
D1	HSMC present	Green
D2	CONF_DONE	Green
D11	POWER_ON	Blue
D21, D22, D23	Power_Good	Green

Table 2–19 lists the four channel activity LEDs (two per interface).

Table 2–19. Channel Activity LEDs

Board Reference Number	Transceiver Interface Indicators	Color
D20, D19	PCI edge connector (L0x1, L0x4)	Yellow (two per channel)
D13, D12	HSMC (TX & RX)	Yellow (two per channel)

Off-Chip Memory

This section describes the board's DDR2 SDRAM off-chip memory interface support, providing signal type, and signal connectivity relative to the Arria GX device.

Table 2–20 shows a summary of the required number of pins to support the 233 MHz DDR2 device available in a 32M x16 data configuration.

Table 2–20. DDR2 Description, Signal Type, Schematic Signal Name & Arria GX Pin Number (Part 1 of 2)

Description	Signal Type	Schematic Signal Name	Arria GX Pin Number
Address (row and column)	SSTL_18 out (15 bits)	DDR2_A(14:0)	AH9, AF10, AH11, AG10, AF7, AF13, AH13, AG8, AH7, AH12, AH10, AF12, AF11, AF9, AE7
Bank address	SSTL_18 out (3 bits)	DDR2_BA(1:0)	AF8, AH8
Data	SSTL_18 in/out (16 bits)	DDR2_DQ(15:0)	AF26, AH25, AG26, AH26, AF22, AH24, AF24, AH23, AG22, AH21, AH22, AF21, AF18, AH20, AF19, AH18
Data strobe	SSTL_18 DQS in/out (2 bits)	DDR2_DQS(1:0)	AG23, AH19
Data write mask (byte enables)	SSTL_18 out (2 bits)	DDR2_DM(1:0)	AF25, AF20
Write enable	SSTL_18 out	DDR2_WEn	AG11
Row address strobe	SSTL_18 out	DDR2_RASn	AH16
Column address strobe	SSTL_18 out	DDR2_CASn	AG16
Differential output clocks (two DDR loads per p/n pair)	Diff. SSTL_18 out (2 bits)	DDR2_CKp(0) DDR2_CKn(0)	AH15 AH14

Table 2–20. DDR2 Description, Signal Type, Schematic Signal Name & Arria GX Pin Number (Part 2 of 2)

Description	Signal Type	Schematic Signal Name	Arria GX Pin Number
Resynchronization timing feedback clock	SSTL_18 out SSTL_18 in	DDR2_SYNC_CLKOUT DDR2_SYNC_CLKIN	AG14 AH17
Clock enable	SSTL_18 out	DDR2_CKE	AE14
Chip select (enables command decoder)	SSTL_18 out	DDR2_CSn	AG13
On-die termination control pin	SSTL_18 out	DDR2_ODT	AE11
SSTL reference voltage	N/A	Vref	AB14, AC10, AD17, AD19, AD22, AD8
Core supply	1.8 V	VDD	N/A *(1)*
I/O supply	1.8 V	VDDQ	N/A *(1)*
DLL supply	1.8 V	VDDL	N/A *(1)*
Core GND	Ground	VSS	N/A *(1)*
I/O GND	Ground	VSSQ	N/A *(1)*
DLL GND	Ground	VSSL	N/A *(1)*

Notes to Table 2–20:
(1) This is a power pin that is not connected to the Arria GX device. For power connection information, refer to the Micron MTA47H32M16 8 Meg X 16 x 4 DDR2 data sheet.

Table 2–21 lists the DDR2 component reference and manufacturing information.

Table 2–21. DDR2 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U8	DDR2 SDRAM	Micron Technology, Inc.	MT47H32M16	www.micron.com

Standard Communication Ports

The board supports the following communication ports discussed in this section:

- PCIe edge connector interface
- High-speed Mezzazine card interface
- JTAG interface

PCI Express Edge Connector Interface (J14)

The board features a x4 (four channel) PCIe edge connector, which operates at 2.5 Gb/s nominal rate using the FPGA transceivers from one transceiver block.

The PCIe mode select jumper (J13) indicates—to the host controlling the Arria GX development board—whether the card is operating in PCIe x1 or PCIe x4 mode. The J13 jumper is necessary because in some systems the `prsnt` pins are the only PCIe interface indicators of supported bus width of the installed card. Some computers may require that the jumper be installed to operate in the PCIe x1 mode.

The PCIe signals have differential traces terminated on the receive-side using internal termination resistors in the Arria GX device receiver pins. Table 2–22 lists the PCIe edge connector pin-out, descriptions, and signal type. Signal directions are relative to the Arria GX device..

Table 2–22. PCIe Edge Connector Pin-Out (Part 1 of 2)

Schematic Signal Name	Description	Signal Type
PCIE_TX_P(3:0) PCIE_TX_N(3:0)	Transmitter differential pairs	1.2 V PCML (4 TX channels)
PCIE_RX_P(3:0) PCIE_RX_N(3:0)	Receiver differential pairs	1.2 V PCML (4 RX channels)
PCIE_PRSNT2n_X1	Hot plug present detect 1	N/A (jumper to PCIE_PRSNT1n)
PCIE_PRSNT2n_X4	Hot plug present detect 1	N/A (jumper to PCIE_PRSNT1n)
PCIE_SMBCLK	SMBus clock (optional)	LVTTL out (open-drain)
PCIE_SMBDAT	SMBus data (optional)	LVTTL in/out (open-drain)
TRST#	JTAG reset (optional)	N/A
TCK	JTAG clock (optional)	N/A
TDI	JTAG data in (optional)	N/A
TDO	JTAG data out (optional)	N/A
TMS	JTAG test mode select (optional)	N/A
PCIE_WAKEn	Link reactivation signal	LVTTL out (isolate with a jumper)

Table 2–22. PCIe Edge Connector Pin-Out (Part 2 of 2)		
Schematic Signal Name	**Description**	**Signal Type**
PCIE_PERSTn	Fundamental reset	LVTTL out
PCIE_REFCLKp PCIE_REFCLKn	Reference clock input	REFCLK in
12V		Power
3.3V		Power
3.3VAUX		Power
GND		Ground

High-Speed Mezzanine Connector Interface

The high-speed mezzanine connector (HSMC) is an Altera-developed specification, which allows users to expand the functionality of the development board through the addition of daughter cards (HSMC cards).

The HSMC interface specification allows for up to eight transceiver channels, a full SPI 4.2 interface (18 LVDS channels), and SMBus management signals. The LVDS channels can be used for CMOS signaling as well as LVDS. Due to limited transceiver resources, four transceiver channels route to the HSMC interface.

For more information about the Altera HSMC interface, refer to the HSMC specifications on the Altera website, **www.altera.com**.

Table 2–23 lists the HSMC interface component reference and manufacturing information.

Table 2–23. HSMC Interface Component Reference and Manufacturing Information				
Board Reference	**Description**	**Manufacturer**	**Manufacturer Part Number**	**Manufacturer Website**
J2	High speed mezzanine connector	Samtec	ASP-122953-01	www.samtec.com

Table 2–24 lists HSMC interface pin-out as well as corresponding Arria GX device pin numbers.

Table 2–24. HSMC Interface Pin-Out (Part 1 of 2)

Description	Type	Schematic Signal Name	Arria GX Device Pin Number
Transceiver transmit channels	1.5 V PCML (4 TX channels)	HSMA_TX_P(3:0) HSMA_TX_N(3:0)	N4, L4, C4, E4 N5, L5, C5, E5
Transceiver receive channels	1.5 V PCML (4 RX channels)	HSMA_RX_P(3:0) HSMA_RX_N(3:0)	N1, L1, E1, G1 N2, L2, E2, G2
Data bus	2.5 V LVCMOS in/out (4 bits)	HSMA_D(3:0)	A24, A23, A26, A25
	2.5 V LVCMOS in/out (17 bits) or LVDS (17 TX channels-p)	HSMA_TX_D_P(16:0)	F24, E26, G24, H23, K24, G26, H26, J25, K26, M25, P25, Y25, AA26, AA23, AB22, AB24, AC25
	2.5 V LVCMOS in/out (17 bits) or LVDS (17 TX channels-n)	HSMA_TX_D_N(16:0)	F23, E25, G23, H22, J23, G25, H25, J24, K25, M24, P24, Y24, AA25, AA22, AB21, AB23, AC24
	2.5 V LVCMOS in/out (17 bits) or LVDS (17 RX channels-p)	HSMA_RX_D_P(16:0)	C28, D28, E28, F27, G28, H28, L28, N28, R28, V28, Y28, Y27, AB28, AC28, AC27, AE28, AF28
	2.5 V LVCMOS in/out (17 bits) or LVDS (17 RX channels-n)	HSMA_RX_D_N(16:0)	C27, D27, F28, F26, G27, J28, M28, P28, T28, W28, AA28, Y26, AB27, AD28, AC26, AE27, AF27
Clock output 0	2.5 V LVCMOS clock output	HSMA_CLKOUT0	A15
Clock output 1	2.5 V LVCMOS in/out (2 bits) or LVDS clock out	HSMA_CLKOUT_P1 HSMA_CLKOUT_N1	AC23 AC22
Clock output 2	2.5 V LVCMOS in/out (2 bits) or LVDS clock out	HSMA_CLKOUT_P2 HSMA_CLKOUT_N2	AE26 AE25
Clock input 0	2.5 V LVCMOS clock in	HSMA_CLKIN0	T25
Clock input 1	2.5 V LVCMOS in/out (2 bits) or LVDS clock in	HSMA_CLKIN_P1 HSMA_CLKIN_N1	U26 U25
Clock input 2	2.5 V LVCMOS in/out (2 bits) or LVDS clock in	HSMA_CLKIN_P2 HSMA_CLKIN_N2	R26 R25

Table 2–24. HSMC Interface Pin-Out (Part 2 of 2)

Description	Type	Schematic Signal Name	Arria GX Device Pin Number
Management serial data line	2.5 V LVCMOS in/out	HSMA_SDA	A20
Management serial clock line	2.5 V LVCMOS out	HSMA_SCL	A18
JTAG clock	N/A (part of chain)	JTAG_TCK	V17
JTAG mode select	N/A (part of chain)	JTAG_TMS	W19
JTAG data out	N/A (part of chain)	HSMA_JTAG_TDO	V19 *(1)*
JTAG data in	N/A (part of chain)	JTAG_TDI	N/A
Power	12 V	12V	N/A
Power	3.3 V	3.3V	N/A
Ground	Ground	GND	N/A

Note to Table 2–24:
(1) When the MAX II device is bypassed, the HSMA_JTAG_TDO signal is connected to Arria GX device pin V19.

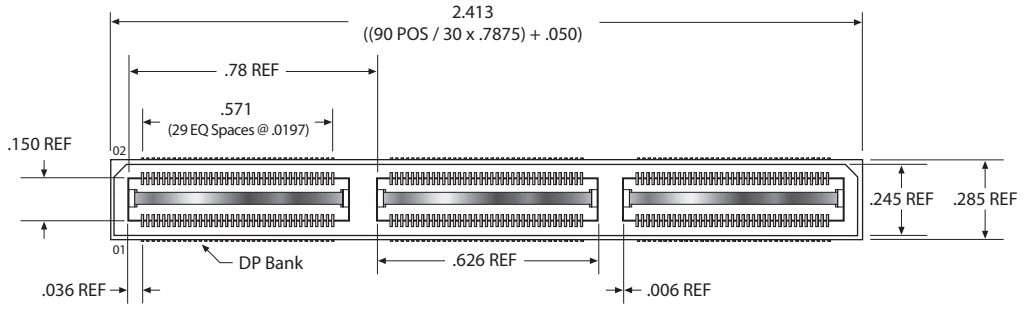
Table 2–25 shows the minimum power levels that the Arria GX development board guarantees from on-board power supplies. The power rails are delivered via designated pins on the HSMC interface.

Table 2–25. Minimum Guaranteed Power Levels

Voltage	Current Rating	MAX Wattage
12 V	1.0 A	12.0 W
3.3 V	2.0 A	6.6 W

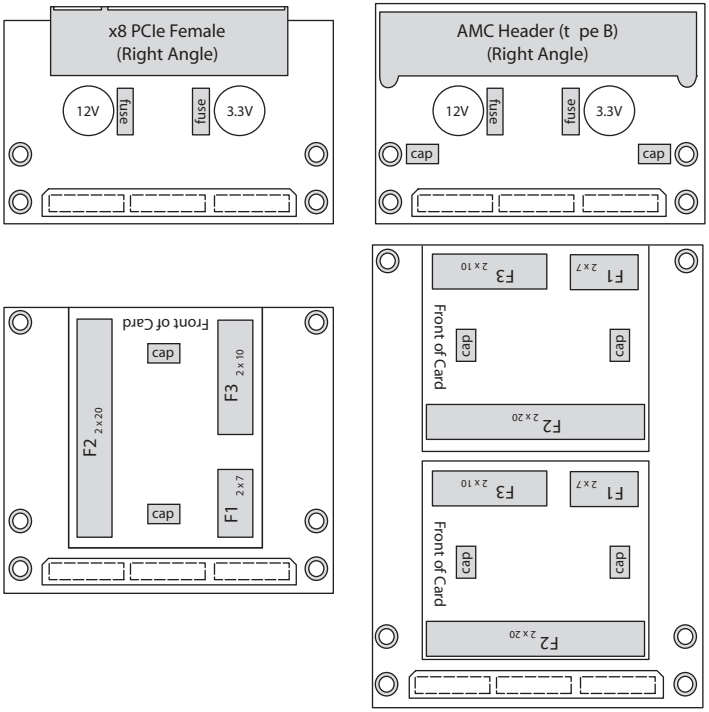
The Arria GX development board uses a Samtec connect to interface to HSMC daughter boards. Figure 2–7 shows the Samtec ASP-122952-01 used on the Arria GX development board. The socket is placed in the "minimum keep-out board-edge layout" style.

Figure 2–7. Samtec ASP Socket Connector



For illustration purposes, Figure 2–8 shows example mezzanine cards. The top-left is a x8 PCIe female adapter (right-angle) and the top-right is an AMC header (type B) adapter. The lower two figures are Altera daughter card (PROTO1) adapters, which are typically 3″ wide and can vary in length.

Figure 2–8. Example Mezzanine Cards



JTAG Interface

The board provides a right-angle, 10-pin JTAG header. The JTAG header protrudes through the front panel of the PCIe card, which positions it well for internal accessibility while the box is closed. Pin 1 is located on the side nearest the SFP connectors.

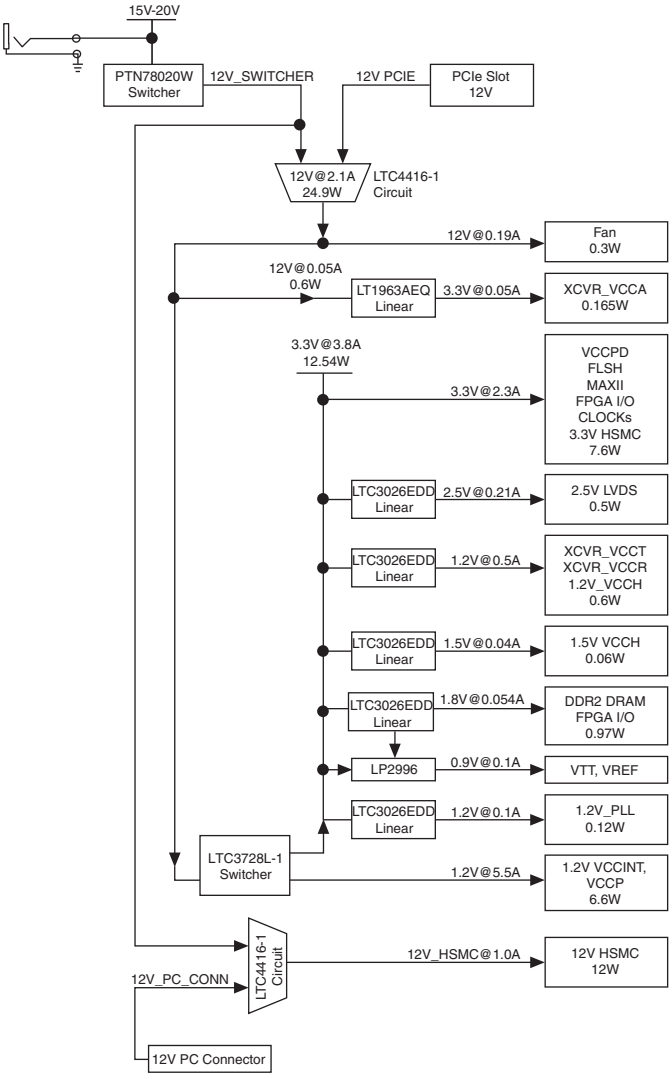
The JTAG header can be used for JTAG-based FPGA programming as well as communication to a standard computer using a USB-Blaster download cable. The default USB-Blaster driver that Quartus II software installs for JTAG programming and SignalTap debugging.

For more information on the JTAG chain, refer to "JTAG Chain Configuration" on page 2–9.

Power Supply

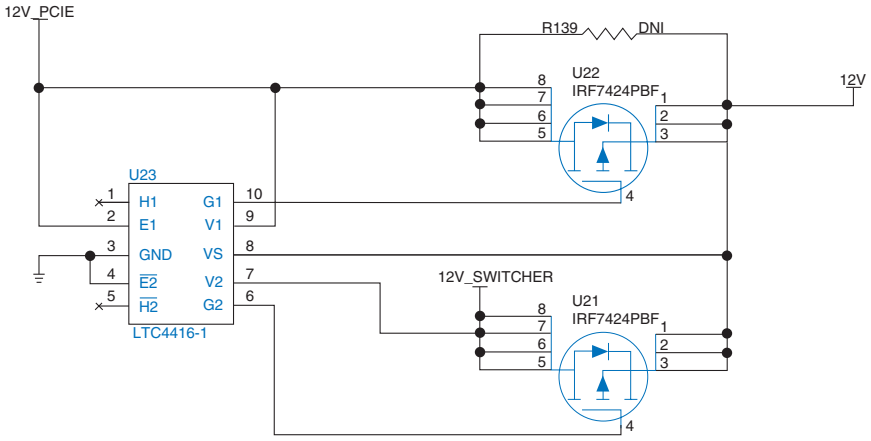
The main source of power comes from either the 12 V PCI Express motherboard (12V_PCIE) or from a DC input jack and subsequent laptop-style DC power supply (12V_SWITCHER). The nominal input spec is from 15 V to 20 V DC on the jack. Similarly, the 12 V HSMC power can be supplied from the DC input jack (12V_SWITCHER) or from a 12 V connection supplied by a PC (12V_PC_CONN). Figure 2–9 shows the power distribution system.

Figure 2–9. Arria GX Development Board's Power Distribution System



Switching between power being delivered by the PCIe slot or through the AC adapter is managed using the LTC4416 multiplexer. A similar multiplexer is used to select 12 V power for the HSMC being supplied by the PC or an AC adapter. Figure 2–10 shows the configuration for this power multiplexer.

Figure 2–10. Configuration for the Power Multiplexer



Temperature Sensor

This board has a two-wire SMBus interface to a National Semiconductor temperature sensing device (LM95235), which is a low-bandwidth A/D converter that measures small voltage changes across a temperature diode on the die of the Arria GX device. The device can be programmed to automatically turn on a cooling fan at a specified temperature. A stuffing resistor is available to turn the fan on regardless of the LM95235 setting. Table 2–26 describes the National Semiconductor device.

Table 2–26. Arria GX Thermal Solutions Parts List

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Web Site
U13	Remote diode temperature sensor	National Semiconductor	LPM95235	www.national.com

Heat Sink and Fan

The Dynatron SCP1 heat sink unit provides heat dissipation for the Arria GX device. The fan uses 190mA at 12 V and can dissipate 25 W of heat with no additional air flow in a lab-bench type environment. The 12 V is delivered through a two-pin 100-mil header.