

Chapter 14, *Using Altera Enhanced Configuration Devices* replaces AN 218: *Using Altera Enhanced Configuration Devices*.

## Introduction

Altera's latest enhanced configuration devices address the need for a high-density configuration solution by combining industry-standard flash memory with a feature-rich configuration controller. A single-chip configuration solution provides designers with several new and advanced features that significantly reduce configuration times. This application note discusses the hardware and software implementation of enhanced configuration device features such as concurrent and dynamic configuration, data compression, clock division, and an external flash memory interface. Enhanced configuration devices include EPC4, EPC8, and EPC16 devices.

## Concurrent Configuration

Configuration data is transmitted from the enhanced configuration device to the SRAM-based device on the DATA lines. The DATA lines are outputs on the enhanced configuration devices, and inputs to the SRAM-based devices.

These DATA lines correspond to the Bit<sub>n</sub> lines in the **Convert Programming Files** window in the Altera® Quartus® II software. For example, if you specify a SRAM Object File (.sof) to use Bit<sub>0</sub> in the Quartus II software, that .sof will be transmitted on the DATA[0] line from the enhanced configuration device to the SRAM-based device.

Enhanced configuration devices can concurrently configure a number of devices with a variety of supported configuration schemes.

### Supported Schemes & Guidelines

By using enhanced configuration devices, there are several different ways to configure Altera® SRAM-based programmable logic devices (PLDs):

- 1-bit passive serial (PS)
- 2-bit PS
- 4-bit PS
- 8-bit PS
- Fast passive parallel (FPP)

Additionally, you can use these configuration schemes in conjunction with the dynamic configuration option (previously called page mode operation) for sophisticated configuration setups.

FPP configuration mode uses the eight `DATA [7..0]` lines from the enhanced configuration device, which can be used to configure Stratix™, Stratix GX, and APEX™ II devices. To decrease configuration time, FPP configuration provides eight bits of configuration data per clock cycle to the target device.



For more information on configuration schemes, refer to the *Enhanced Configuration Devices Data Sheet, Application Note 116: Configuring SRAM-Based LUT Devices*, or [Chapter 13, Configuring Stratix & Stratix GX Devices](#).

### Concurrent Configuration Using $n$ -Bit PS Modes

The  $n$ -bit ( $n = 1, 2, 4,$  and  $8$ ) PS configuration mode allows enhanced configuration devices to concurrently configure SRAM-based devices or device chains. In addition, these devices do not have to be the same device family or density; they can be any combination of Altera SRAM-based devices. An individual enhanced configuration device `DATA` line is available for each targeted device. Each `DATA` line can also feed a daisy chain of devices.

The Quartus II software only allows the selection of  $n$ -bit PS configuration modes. However, you can use these modes to configure any number of devices from 1 to 8. When configuring SRAM-based devices using  $n$ -bit PS modes, use [Table 14–1](#) to select the appropriate configuration mode for the fastest configuration times.



Mode selection has an impact on the amount of memory used, as described in “Calculating the Size of Configuration Space” on page 14–18.

**Table 14–1. Recommended Configuration Using n-Bit PS Modes**

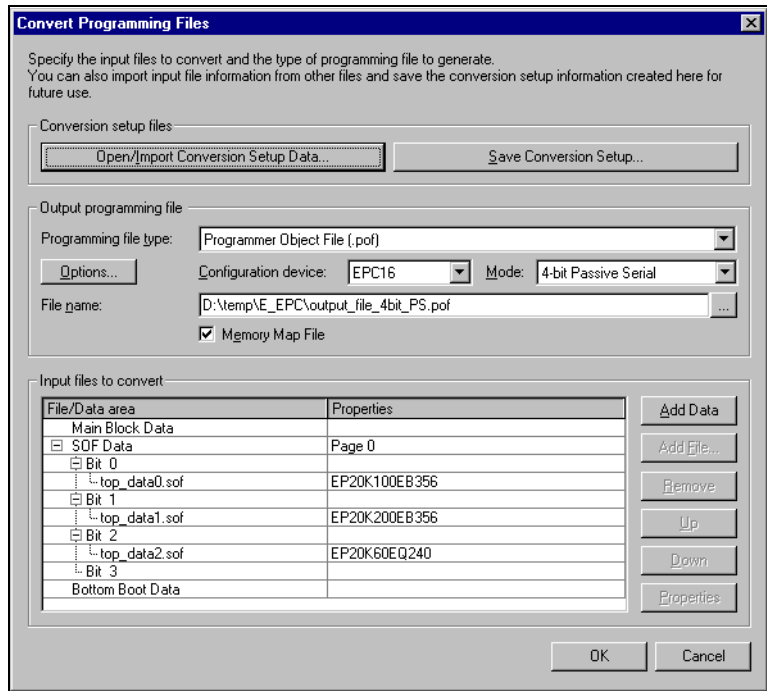
Number of Devices (1)	Recommended Configuration Mode
1	1-bit PS
2	2-bit PS
3	4-bit PS
4	4-bit PS
5	8-bit PS
6	8-bit PS
7	8-bit PS
8	8-bit PS

**Note to Table 14–1:**

- (1) Assume that each DATA line is only configuring one device, not a daisy chain of devices.

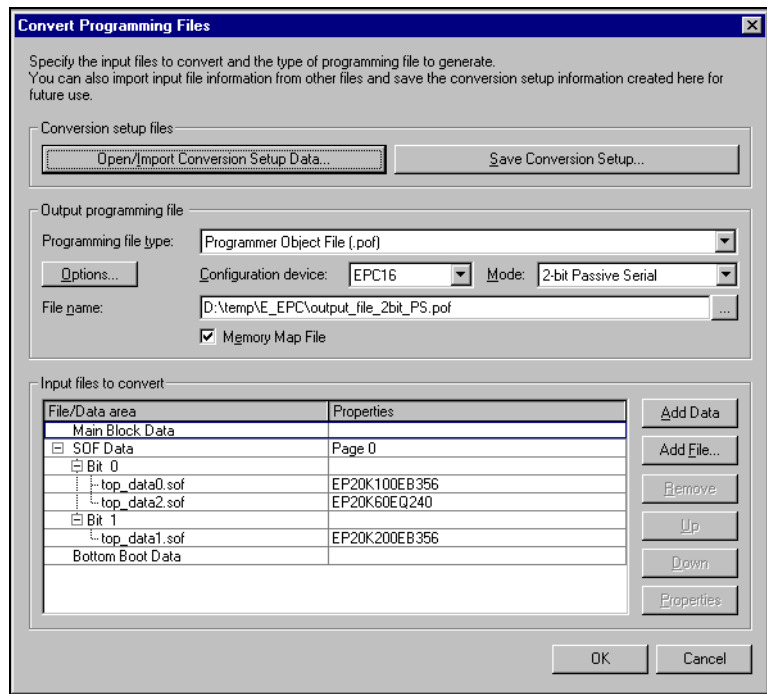
For example, if you configure three SRAM-based devices, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding .sof data will be transmitted from the configuration device to the SRAM-based PLD. For DATA3, you can leave the corresponding Bit3 line blank in the Quartus II software. On the printed circuit board (PCB), leave the DATA3 line from the enhanced configuration device unconnected. Figure 14–1 shows the Quartus II Convert Programming Files window (Tools menu) setup for this scheme.

**Figure 14–1. Software Settings for Configuring Devices Using n-Bit PS Modes**



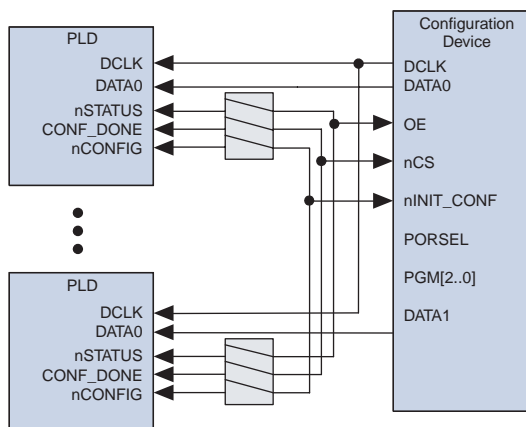
Alternatively, you can daisy chain two SRAM-based devices to one DATA line while the other DATA lines drive one device each. For example, you could use the 2-bit PS mode to drive two SRAM-based devices with DATA Bit0 (EP20K100E and EP20K60E devices) and the third device (the EP20K200E device) with DATA Bit1. This 2-bit PS configuration scheme requires less space in the configuration flash memory, but may increase the total system configuration time. See [Figure 14–2](#).

**Figure 14–2. Setup for Daisy Chaining Two SRAM-Based Devices to One DATA Line**



## Design Guidelines

For debugging, Altera recommends keeping the control lines such as `nSTATUS`, `nCONFIG`, and `CONF_DONE` between each PLD and the configuration device separate. You can keep control lines separate by using a switch to manage which control signals are fed back into the enhanced configuration device. Figure 14–3 shows an example of the connections between the enhanced configuration device and the targeted PLDs.

**Figure 14–3. Example of Using Debugging Switches for Control Lines**

## Dynamic Configuration (Page Mode) Implementation Overview

Pages in enhanced configuration devices allow you to organize and store various configurations for entire systems that use one or more Altera PLDs. This dynamic configuration (or page mode) feature allows systems to dynamically reconfigure their PLDs with different configuration files.

You can use different pages to store configuration files that support different standards (e.g., I/O standards, memory). Alternatively, the different pages can place the system in different modes. For instance, page 0 could contain a configuration file (.sof) for the PLD that only processes data packets; page 1 could contain a configuration file for the same PLD that processes data and voice packets.

With the ability to dynamically switch pages, you can also configure Altera devices with various revisions for debugging without having to reprogram the configuration device. For example, you can configure a device that is on “stand-by” to perform another function and then reconfigure it back with the original configuration file.

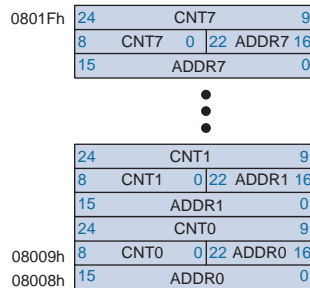
A page is a section of the flash memory space that contains configuration data for all PLDs in the system. One page stores one system configuration regardless of the number of PLDs in the system. The size of each page is dynamic and can change each time the enhanced configuration device is reprogrammed. Enhanced configuration devices support a maximum of eight pages of configuration data, or eight system configurations. The number of pages is also limited to the density of the configuration device.



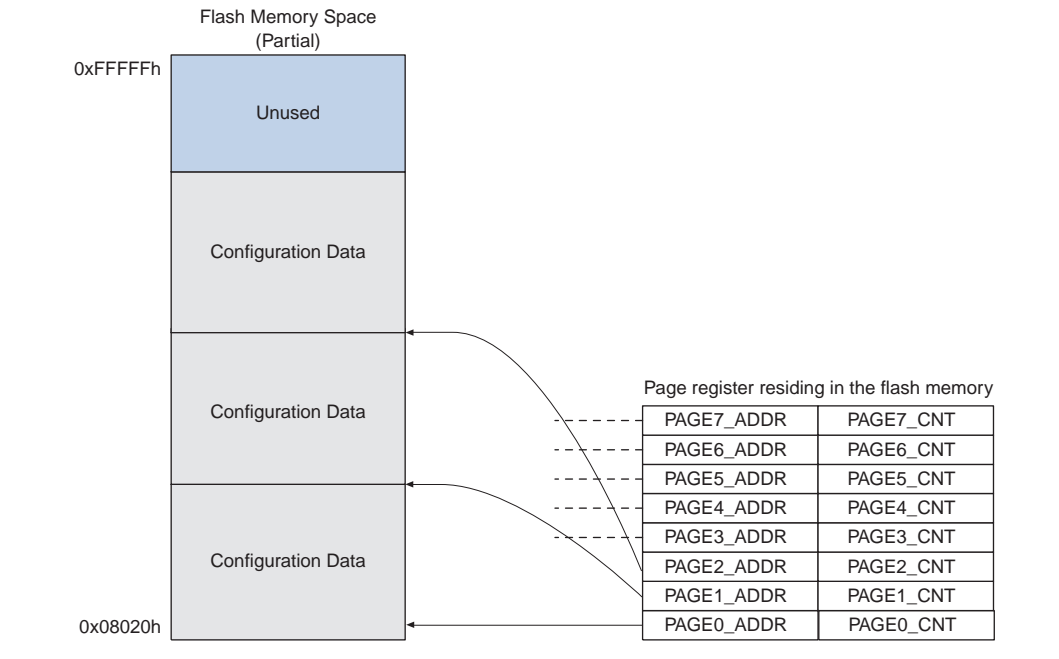
The number of pages required in a system is not dependent on the number of PLDs in the system, but depends on the number of unique system configurations.

External page mode input pins `PGM[2..0]` determine which page to use during PLD configuration, and page pointers determine the data location. Each page pointer consists of a starting address register and a length count register. The word-addressable starting address register (23 bits) is used to determine where the page begins in the flash memory. The count register (25 bits) determines the length of the page counted in nibbles (group of 4 bits equaling half of a byte). [Figure 14-4](#) shows a block diagram of the option-bit space and its address locations.

**Figure 14-4. Option-Bit Memory Map**



For instance, a page for the EPC16 configuration device must start between word addresses `0x08020h` and `0xFFFFFh` and cannot overlap with other pages. See [Figure 14-5](#) for an EPC16 page mode example using three pages.

**Figure 14–5. EPC16 Page Mode Implementation Example**

During configuration, different pages are selected by the `PGM[2..0]` pins. These pins are used to select one out of eight pages (or eight system configurations). `PGM[2..0]` pins are sampled once before the configuration data is sent to the target PLDs.

Within each page, you can store as many configuration files as your system needs. There is no limitation to the length of a page except for the physical limitation determined by the size of the flash memory (e.g., `0xFFFFFFFFh` for EPC16 devices). However, all pages must be contiguous.

### Software Implementation (Convert Programming Files)

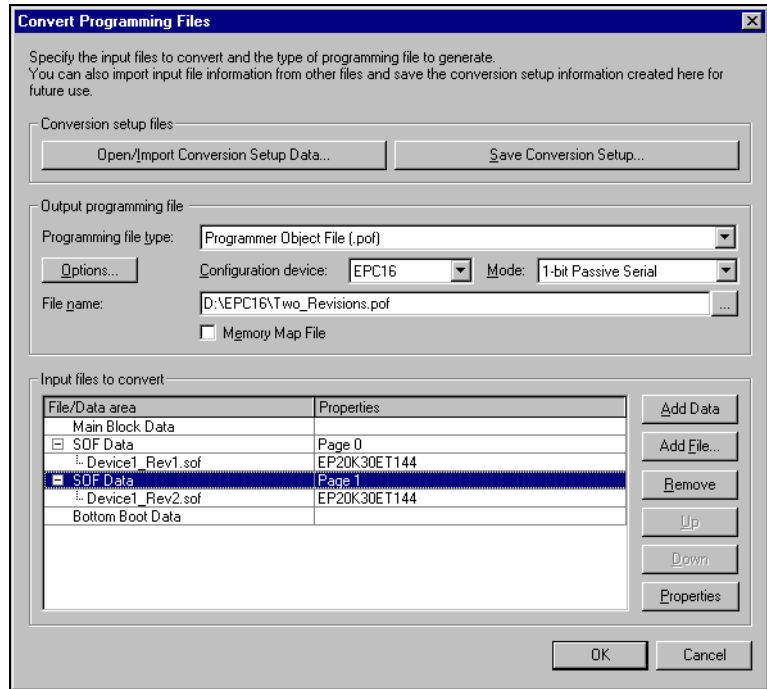
The **Convert Programming Files** window (Tools menu) in the Quartus II software allows you to create enhanced configuration device programmer object files (`.pof`) and enable the dynamic configuration feature.



Passive parallel asynchronous (PPA) and passive parallel synchronous (PPS) configuration modes are not supported by enhanced configuration devices. If you choose one of these modes, the Quartus II software reports an error message when the enhanced configuration device's **.pof** is generated.

In the **Convert Programming Files** window, there are **SOF Data** entries (**.sof**), located in the **Input files to convert** dialog box. Each **SOF Data** entry refers to a unique system configuration. [Figure 14–6](#) shows the setup for a system that has one APEX device and uses two pages, 0 and 1. Each of the two pages has a different version of the configuration file for the same APEX device.

**Figure 14–6. Using Page Mode Example**



To set which page pointer(s) will point to a particular page or **SOF Data** entry, select **SOF Data** and click **Properties**. Clicking **Properties** launches the **SOF Data Properties** window where you can select page pointers to point to the **SOF Data** chosen. If you do not use the **SOF Data Properties** window to make changes, the default page is 0. Each **SOF Data** entry for

your configuration device must have a unique page number(s).

Figure 14–7 shows page pointer 1 being assigned to the **SOF Data** section containing **Device1\_Rev2.sof** (from Figure 14–6).

**Figure 14–7. Software Setting for Selecting Pages**

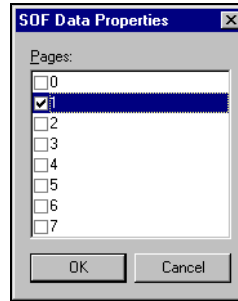
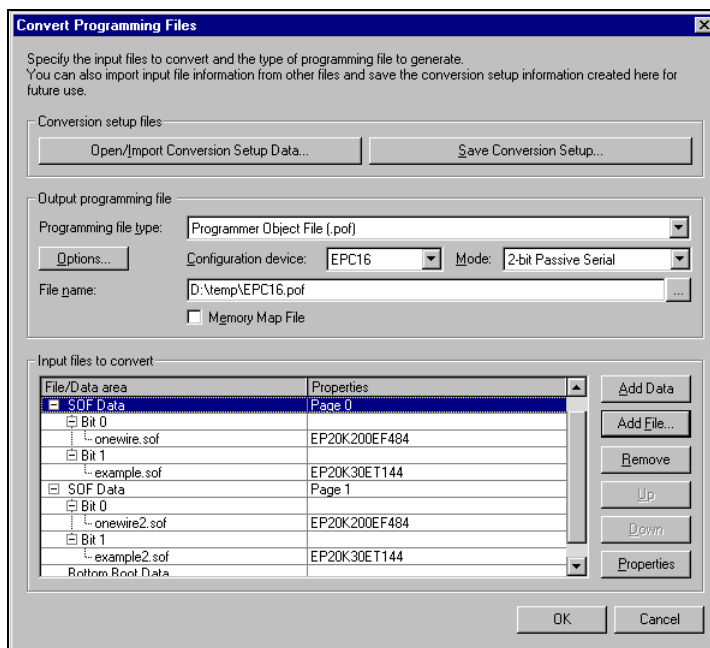


Figure 14–8 shows a more complex setup that uses the 2-bit PS configuration mode to concurrently configure two different APEX devices with multiple pages storing two revisions of each design. Two configurations for the entire system requires four configuration files (i.e., the number of devices multiplied by the number of unique system configurations).

**Figure 14–8. Concurrent Configuration of Two Devices with Two System Configurations**

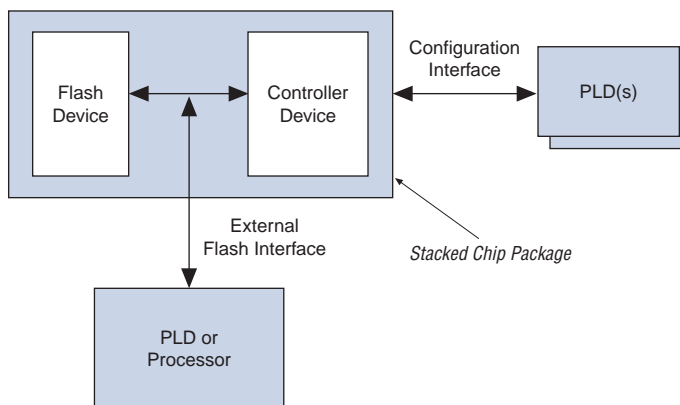


By selecting the *Memory Map File* option, the Quartus II Memory Map output file (**.map**) describing the flash memory address locations is generated. This information is typically useful when using the external flash interface feature.

## External Flash Memory Interface

Enhanced configuration devices support an external flash interface that allows devices external to the controller access to the enhanced configuration device's flash memory. You can use the flash memory to store boot or application code for processors, or as general-purpose memory for processors and PLDs.

Figure 14–9 shows the interfaces available on the enhanced configuration device.

**Figure 14–9. Enhanced Configuration Device Interfaces**

Applications that require remote update capabilities for on-board programmable logic (Stratix and Stratix GX devices), and applications that use soft embedded processor cores (e.g., the Nios<sup>®</sup> embedded processor) typically use the external flash memory interface feature.

For soft core embedded processor applications, the controller configures the programmable logic by using configuration data stored in the flash memory. On successful configuration, the embedded processor uses the external flash interface to boot up and run code from the same flash memory, eliminating the need for a stand-alone flash memory device.

For applications requiring remote system configuration capabilities, a processor or PLD can use the external flash interface to store an updated configuration image into a new page in flash memory (the external flash interface coupled with dynamic configuration). You can obtain new configuration data from a local intelligent host or through the Internet. Reconfiguring the system with the new page updates the system configuration.



For more information on implementing remote and local system updates with enhanced configuration devices, refer to [Chapter 15, Using Remote System Configuration with Stratix & Stratix GX Devices](#).

Currently, EPC4 and EPC16 configuration devices support the external flash interface. For support of this feature in other enhanced configuration devices, contact Altera Applications.

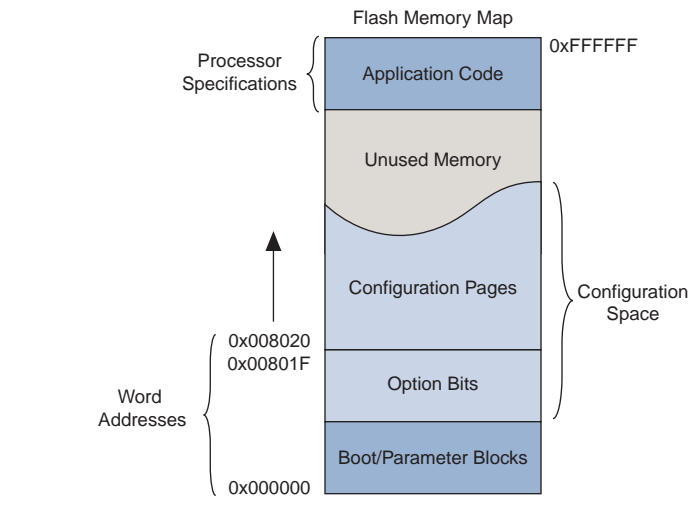
## Flash Memory Map

You can divide an enhanced configuration device's flash memory into two categories: logical (configuration and processor space) and physical (flash data block boundaries). Configuration space consists of portions of memory used to store configuration option bits and configuration data. Processor space consists of portions of memory used to store boot and application code.

### Logical Divisions

In all enhanced configuration devices, configuration option bits are stored ranging from word address  $0x008000$  to  $0x00801F$  (i.e., byte address  $0x010000$  to  $0x01003F$ ). These bits are used to enable various controller features such as configuration mode selection, compression mode selection, and clock divider selection. In all enhanced configuration devices, configuration data is stored starting from word address location  $0x008020$  or byte address  $0x010040$ . The ending address of configuration space is not fixed and depends on the number and density of PLDs configured using the enhanced configuration device as well as the number of pages. All remaining address locations above the configuration space are available for processor application code. The boot space spans addresses  $0x000000$  to  $0x007FFF$ . Both boot and application code spaces are intended for use by an external processor or PLD. Figure 14–10 shows the flash memory map inside an EPC16 device.

**Figure 14–10. EPC16 Flash Memory Map**



### *Physical Divisions*

Conversely, physical divisions are flash data blocks that can be individually written to and erased. For instance, the EPC16 device contains 16-Mbit Sharp flash memory that is divided into 2 boot blocks, 6 parameter blocks, and 31 main data blocks. These physical divisions vary from one flash memory or vendor to another and must be considered if the external flash interface is used to erase or write flash memory. These divisions are not significant if the interface is used as a read-only interface after initial programming.



For detailed information on enhanced configuration device flash memories, refer to the corresponding flash memory data sheet. The SHARP and Micron data sheets include flash command details, timing diagrams, and flash memory map information, and are available at <http://www.altera.com>.

### **Interface Availability & Connections**

Flash memory ports are shared between the internal controller and the external device. A processor or PLD can use the external flash interface to access flash memory only when the controller is not using the interface. Therefore, the internal controller is the primary master of the bus, while the external device is the secondary master.

Flash memory ports (address, data, and control) are internally connected to the controller device. Additionally, these ports are connected to pins on the package providing the external interface. During in-system programming of the enhanced configuration device as well as configuration of the PLDs, the controller uses the internal interface to flash memory, rendering the external interface unavailable. External devices should tri-state all connections (address, data, and control) for the entire duration of in-system programming and configuration to prevent contention.

On completion of in-system programming and configuration, the internal controller tri-states its interface to the flash memory and enables weak internal pull-up resistors on address and control lines as well as bus-hold circuits on the data lines. The internal flash interface is now disabled and the external flash interface is available.



If you do not use the external flash interface feature, most flash-related pins must be left unconnected on the board to avoid contention. There are a few exceptions to this guideline outlined in the data sheet and pin-out tables.



For detailed schematics, refer to the *Enhanced Configuration Device Data Sheet*.

## Quartus II Software Support

You can use the **Convert Programming Files** window to generate flash memory programming files. You can program flash memory in-system using Joint Test Action Group (JTAG) or through the external flash interface. Select the **.pof** when programming the flash memory in-system. You can also convert this **.pof** to a Jam™ standard test and programming language (STAPL) file (**.jam**) or Jam Byte-Code file (**.jbc**) for in-system programming. When programming the flash memory through the external flash interface, you can create a **.hexpof** from this window.



The **.hexpof** used for programming enhanced configuration devices is different from the **.hexout** configuration file generated for SRAM PLDs.

Along with PLD configuration files, you can program processor boot and application code into flash memory through the **Convert Programming Files** window. You can add a **.hex** file containing boot code to the **Bottom Boot Data** section of the window. Similarly, you can add a **.hex** file containing application code to the **Main Block Data** section. You can store these files in the flash memory using relative or absolute addressing. For selecting the type of addressing, highlight the **Bottom Boot Data** or **Main Block Data** section and click **Properties (Convert Programming Files** window).

Relative addressing mode allows the Quartus II software to pick the location of the file in memory. For instance, the Quartus II software always stores boot code starting at address location  $0 \times 000000$ . This data increases to higher addresses.




The maximum boot file size for the EPC16 configuration device is 32 K words or 64 Kbytes. The boot code is limited to the boot and flash memory parameter blocks.

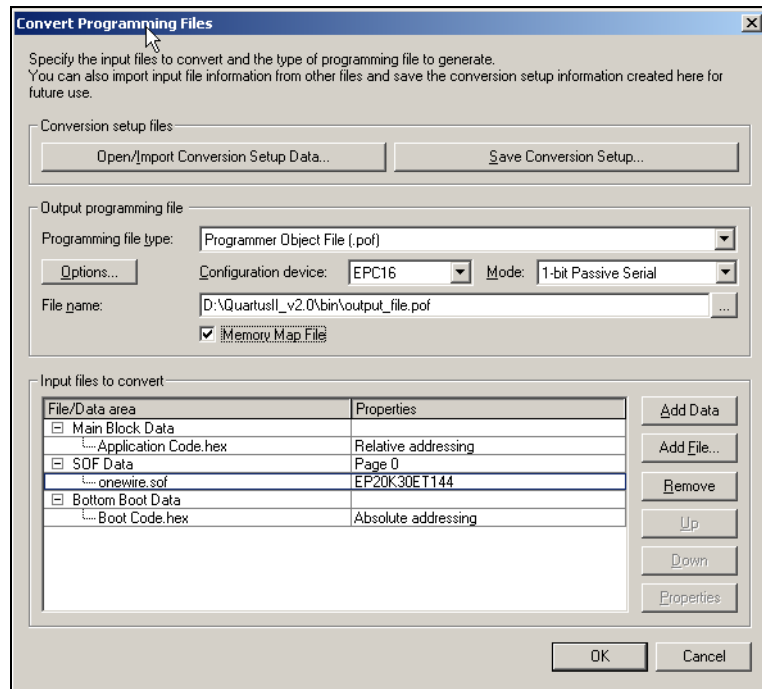
When you select relative addressing mode for **Main Block Data**, the Quartus II software aligns the last byte of information with the highest address (i.e.,  $0 \times 1FFFFFF$ ). Therefore, the starting address is dependent on the size of the **.hex** file. You can easily obtain the starting address of the application code by using the **.map** file discussed below.

Conversely, the absolute addressing mode forces the Quartus II software to store the boot or application **.hex** file data in address locations specified inside the **.hex** file itself. When this mode is selected, create **.hex** files with the correct offsets and ensure there is no overlap with addresses used for storing configuration data.

Figure 14–11 shows a screen shot of the **Convert Programming Files** window setup to create a **.pof** and **.map** file for an enhanced configuration device.

 Only one **.hex** file can be added to the **Bottom Boot Data** and **Main Block Data** sections of this window.

**Figure 14–11. Storing Boot & Application Code in Flash Memory**



You can use the **Quartus II Convert Programming Files** window to create two files specific to the external flash interface feature—the **.hexpof** and the **.map** files. The **.hexpof** contains an image of the flash memory and the **.map** file contains memory map information. The **.hexpof** can be used by an external processor or PLD to program the flash memory via the external flash interface. The **.map** file contains starting and ending addresses for boot code, configuration page data, and application code.

You can use the **.hexpof** to program blank enhanced configuration devices and/or update portions of the flash memory (e.g., a new configuration page). This file uses the Intel hexadecimal file format and contains 16 Mbits or 2 Mbytes of data. The format of the **.map** file is shown in [Table 14–2](#).

Block	Start Address	End Address
BOTTOM BOOT	0x00000000	0x0000001F
OPTION BITS	0x00010000	0x0001003F
PAGE 0	0x00010040	0x0001AD7F
MAIN	0x001FFFE0	0x001FFFFF

*Note to Table 14–2:*

(1) All the addresses in this file are byte addresses.

To perform partial flash memory updates, select the relevant portions of the **.hexpof** using memory map information provided in the **.map** file.



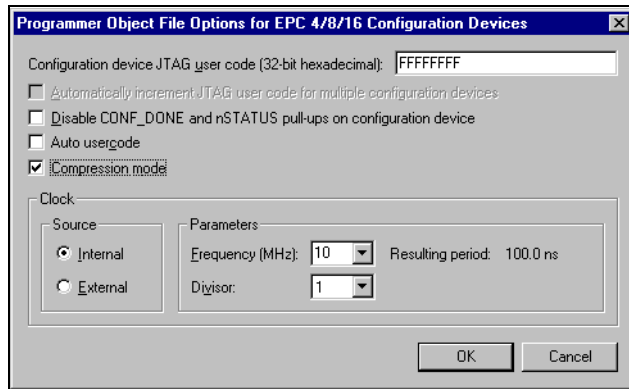
Configuration data and processor space data could exist within the same physical data block. In such cases, erasing the physical data block would affect both configuration and processor data, requiring you to update both. You can avoid this situation by storing application data starting from the next available whole data block.

## Data Compression

Enhanced configuration devices support an efficient compression algorithm that compresses configuration data by 1.9× for typical designs, effectively doubling the size of the device. To select the right density for enhanced configuration devices, you should pre-calculate the total size of uncompressed configuration space.

By clicking **Options** (Convert Programming Files window), you can turn on the *Compression mode* option in the **Programming Object File Options** window with **pof** selected as the programming file type, as shown in [Figure 14–12](#).

Figure 14–12. Selecting Compression Mode



## Calculating the Size of Configuration Space

When using 1-bit PS configuration mode to serially configure multiple devices, all configuration data is transmitted through the same `DATA` line and the devices are daisy-chained together. Therefore, the total size of the uncompressed configuration data is equal to the sum of the SRAM-based device's configuration file size multiplied by the number of pages used.

When using  $n$ -bit PS configuration mode to concurrently configure multiple devices, each SRAM-based device has its own `DATA` line from the enhanced configuration devices. The total size of the uncompressed configuration space is equal to the size of the largest device's configuration file size multiplied by  $n$  (where  $n = 1, 2, 4, \text{ or } 8$ ), which is then multiplied by the number of pages used. For example, if three devices are concurrently configured using 4-bit PS configuration mode, the total size of the uncompressed configuration space is equal to the size of the largest device's configuration file multiplied by four.

When using FPP configuration mode, the total size of the uncompressed configuration space is equal to the sum of the SRAM-based device's configuration file size multiplied by the number of pages used

For configuration file sizes of SRAM-based devices, refer to *Application Note 116: Configuring SRAM-Based LUT Devices*.

## Clock Divider

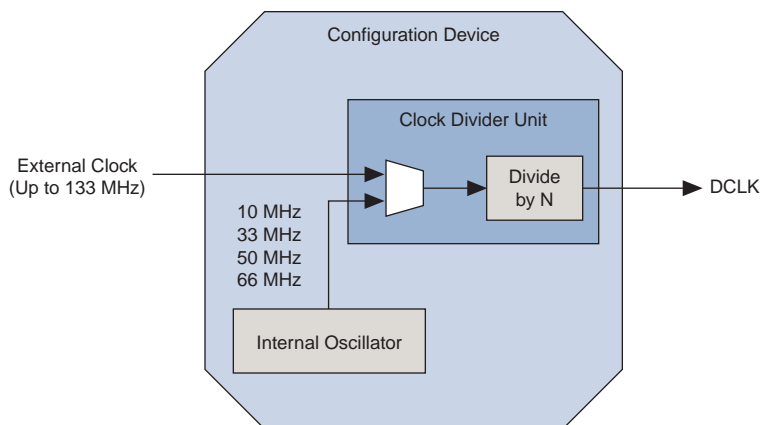
The clock divider value specifies the clock frequency divisor, which is used to determine the `DCLK` frequency, or how fast the data is clocked into the SRAM-based device. You must consider the maximum `DCLK` input frequency of the targeted SRAM device family while selecting the

clock input and divider settings. For DCLK timing specifications of SRAM-based devices, refer to *Application Note 116: Configuring SRAM-Based LUT Devices*.

## Settings & Guidelines

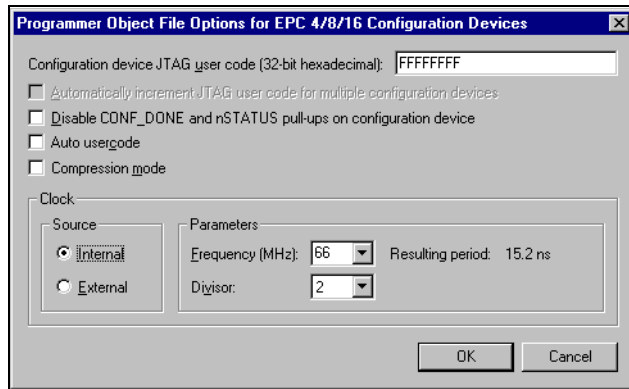
Enhanced configuration devices can use either the internal oscillator or an external clock source to clock data into SRAM-based devices, as shown in Figure 14–13. The enhanced configuration device's internal oscillator runs at nominal speeds of 10, 33, 50, or 66 MHz. The minimum and maximum speeds are shown in the *Enhanced Configuration Device Data Sheet*. Additionally, the enhanced configuration device can accept an external clock source running at speeds of up to 133 MHz.

**Figure 14–13. Clock Divider Unit in Enhanced Configuration Devices**



## Software Implementations

You can select the clock source and the clock speed in the **Programming Object File Options** window with **poF** selected as the programming file type (Convert Programming Files window), as shown in Figure 14–14. You can type the appropriate external clock frequency in the **Frequency (MHz)** drop-down menu, and select any value from the divisor list regardless of the clock source setting.

**Figure 14–14. Software for Setting Clock Source & Clock Divisor**

## Conclusion

The enhanced configuration device is a single-chip configuration solution that provides designers with increased configuration flexibility and faster time-to-market. Features such as data compression, multiple clock sources, clock division, and parallel or concurrent programming significantly reduce configuration times, while the dynamic configuration mode and the external flash interface take intelligent system configuration to a higher level.