


This chapter describes the dynamic reconfiguration features available in Stratix<sup>®</sup> V transceivers.

-  For information about features that will be supported in a future release of the Quartus<sup>®</sup> II software, refer to the *Upcoming Stratix V Device Features* document.

Offset cancellation, as described in “[Offset Cancellation Calibration](#)” on page 6–2, is automatically performed during device power-up. After the reset sequence is completed, the Transceiver Reconfiguration Controller is ready for user-controlled operations.

Stratix V transceivers have a dedicated reconfiguration space. You can enable or disable the following features in the Transceiver Reconfiguration Controller:

- “[PMA Controls Reconfiguration](#)” on page 6–2
- “[On-Chip Signal Quality Monitoring \(EyeQ\)](#)” on page 6–2
- “[Decision Feedback Equalization](#)” on page 6–3
- “[Adaptive Equalization](#)” on page 6–3

The transceiver supports three loopback modes, as described in “[Enabling and Disabling Loopback Modes](#)” on page 6–3:

- Serial loopback
- Reverse serial loopback
- Reverse serial pre-clock data recovery (CDR) loopback

The Transceiver Reconfiguration Controller supports two reconfiguration modes, as described in “[Transceiver PLL Reconfiguration](#)” on page 6–4:

- Channel
- Phase-locked loop (PLL)

-  For more information about the controller, its settings, and how to implement it in your design, refer to the *Transceiver Reconfiguration Controller* chapter of the *Altera Transceiver PHY IP Core User Guide*.

## Offset Cancellation Calibration

Every transceiver channel in Stratix V devices has an offset cancellation circuitry to compensate for non-optimal offsets caused by process variations.


The offset cancellation circuitry is controlled by the offset cancellation control logic IP within the Transceiver Reconfiguration Controller. This IP is active only during device power-up, and it automatically performs offset cancellation. After the reset sequence is completed, the Transceiver Reconfiguration Controller is ready for user-controlled operations.


The clock (`mgmt_clk_clk`) to the Transceiver Reconfiguration Controller is also used for transceiver calibration and should be within the range of 100-125 MHz. If the clock (`mgmt_clk_clk`) is not free-running, the reconfiguration controller reset (`mgmt_rst_reset`) must be held in reset until the clock is stable.

## PMA Controls Reconfiguration

Use the Transceiver Reconfiguration Controller to reconfigure the following analog settings:

- Differential output voltage ( $V_{OD}$ )
- Pre-emphasis taps
- Receiver equalization control
- Receiver equalization DC gain

 For more information about reconfiguring a specific PMA control, refer to “How to Reconfigure a PMA Control” in the *Transceiver Reconfiguration Controller* chapter of the *Altera Transceiver PHY IP Core User Guide*.

 For a specific design example, refer to *AN 645: Dynamic Reconfiguration of PMA Controls in Stratix V Devices*.

## On-Chip Signal Quality Monitoring (EyeQ)

The BER eye contour can be used to measure the quality of the received data. EyeQ is a debug/diagnosis tool that analyzes the received data recovery path, including the receiver’s gain, noise level, and recovery clock jitter. EyeQ can also measure vertical eye height, effectively allowing a BER eye contour to be plotted.


EyeQ uses a phase interpolator (PI) and sampler (SMP) to estimate the horizontal eye opening. Controlled by a logic generator, the PI generates a sampling clock and the SMP samples the data from the receiver output. The SMP outputs parallel data that is monitored for CRC or BER errors. When the PI output clock phase is shifted by small increments, the data error rate goes from high to low to high if the receiver is good. The number of steps of valid data is defined as the width of the eye. If none of the steps yields valid data, the width of the eye is equal to 0, which means the eye is closed.

The dynamic reconfiguration controller in Stratix V devices allows you to enable the EyeQ feature and step through the 32 phase steps of the recovered clock. You can use EyeQ to quantify the change in eye opening for different analog settings.

## Decision Feedback Equalization


Decision feedback equalization (DFE) helps compensate for backplane attenuation because of insufficient bandwidth. DFE works by actively shifting the incoming signal based on the history of the received data. In other words, the purpose of DFE is to cancel out the post-cursor because of intersymbol interference (ISI). The advantage of DFE is that it boosts the power of the highest frequency component of the received data without increasing its noise power. Use DFE in conjunction with the transmitter pre-emphasis and receiver linear equalization.


The dynamic reconfiguration controller in Stratix V devices provides an Avalon<sup>®</sup> Memory-Mapped (Avalon-MM) user interface to step through the DFE tap settings.

 In Stratix V GT devices, the GT channels do not support DFE. This feature is supported in the GX channels.

## Adaptive Equalization

High-speed interface systems require different equalization settings to compensate for changing data rates and backplane losses. Manual tuning of the receiver channel equalization stages involves finding the optimal settings through trial and error, and then locking in those values during compilation. This manual static method is cumbersome and inefficient when system characteristics vary. The adaptive equalization (AEQ) feature solves this problem by automatically tuning an active receiver channel equalization filters based on a frequency content comparison between the incoming signals and the internally generated reference signals.

 In Stratix V GT devices, the GT channels do not support AEQ. This feature is supported in the GX channels.

 The dynamic reconfiguration controller in Stratix V devices allows you to enable the AEQ feature. Refer to the *Transceiver Architecture in Stratix V Devices* chapter for more information about enabling different options and using them to control the AEQ hardware.


## Enabling and Disabling Loopback Modes

You can enable or disable various loopback modes by writing the appropriate registers. You can use the different loopback modes to help debug your design.

The following loopback paths are available:

- **Serial loopback path**—This mode takes the output at the serializer and feeds it back to the CDR. While in this mode, the serializer also feeds the data to the TX output port. Enabling or disabling serial loopback mode is done through the PHY IP management.

- **Reverse serial loopback path**—The receiver (RX) captures the input data and feeds it into the CDR. The recovered data from the CDR output feeds into the TX driver and sends to the TX pins through the TX driver. For this path, you can test the RX and CDR. In the reverse serial loopback mode, you can program the TX driver to use either the main tap only or the main tap and the pre-emphasis first post-tap. Enabling or disabling reverse serial loopback mode is done through the **Analog Controls** section in the Transceiver Reconfiguration Controller.
- **Reverse serial pre-CDR loopback path**—The RX captures the input data and feeds it back to the TX driver through a buffer. This path does not go through the CDR. With this path, you can perform a quick check for the quality of the RX and TX buffers. Enabling or disabling the reverse serial pre-CDR loopback mode is done through the **Analog Controls** section in the Transceiver Reconfiguration Controller.

 For descriptions of the different loopback modes, refer to the *Transceiver Loopback Support in Stratix V Devices* chapter. For implementation details about the different loopback modes, refer to “Loopback Modes” in the *Transceiver Reconfiguration Controller* chapter of the *Altera Transceiver PHY IP Core User Guide*.

## Transceiver PLL Reconfiguration

The Stratix V Transceiver Reconfiguration Controller supports PLL reconfiguration. You can reconfigure the PLLs in the following ways:

- Switch the reference clocks to the CDR and transmitter PLLs
- Reconfigure the PLL connected to the transceiver channel

For example, you can switch the reference clock from 100 MHz to 125 MHz. You can also change the data rate from 2.5G to 5G by reconfiguring the transmitter PLL connected to the transceiver channel.

## Transceiver Channel and Interface Reconfiguration

The Stratix V Transceiver Reconfiguration Controller supports channel and interface reconfiguration.

### Transceiver Channel Reconfiguration

You can reconfigure the channels in the following ways:

- Reconfigure the CDR of the receiver channel.
- Enable and disable the static PCS blocks.
- Select an alternate PLL in the transceiver block to supply a different clock to the transceiver clock generation block.
- Every transmitter channel has a clock divider. When you reconfigure these clock dividers, ensure that the functional mode of the transceiver channel supports the reconfigured data rate.
- You can reconfigure the receiver rate by reconfiguring the CDR.

For example, you can change the data rate from 6.25G to 3.125G by reconfiguring the clock divider.

## Transceiver Interface Reconfiguration

You can reconfigure the transceiver interfaces in the following ways:

- Reconfigure the FPGA fabric-transceiver channel data width
- Reconfigure the existing functional mode of the transceiver channel to a different functional mode (for custom PHY IP only)

For example, you can reconfigure the custom PHY IP from 8B/10B mode to SONET. There is no limit to the number of functional modes you can reconfigure the transceiver channel to if the various clocks involved support the transition. When you switch the custom PHY IP from one function mode to a different function mode, you may need to reconfigure the FPGA fabric-transceiver channel data width, enable or disable PCS blocks, or both, to comply with the protocol requirements.

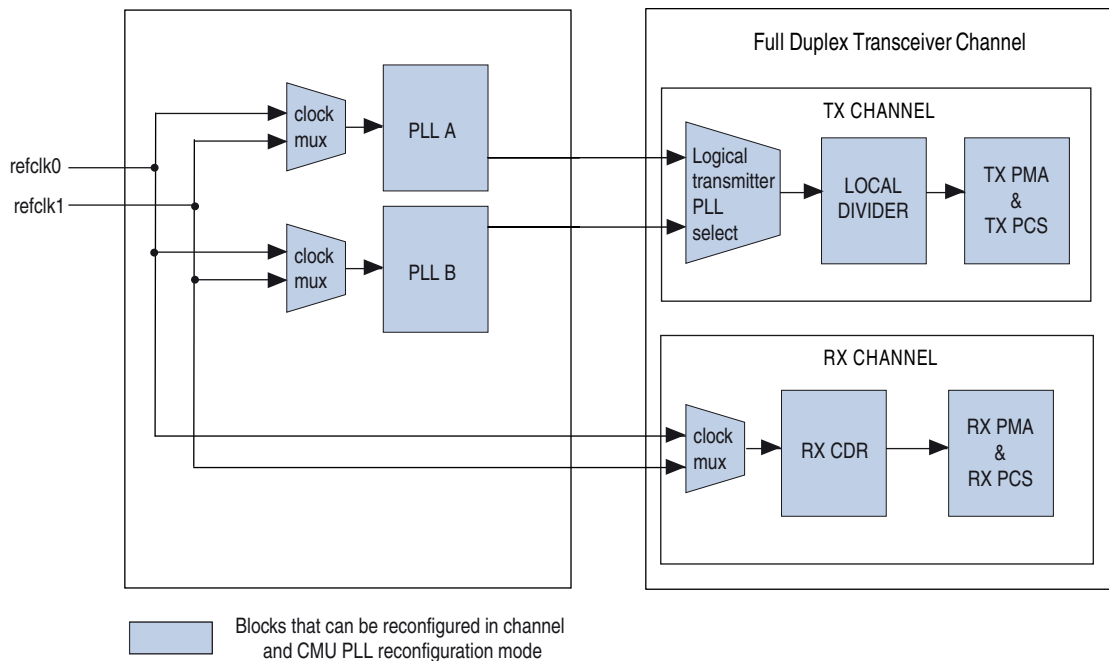
Channel reconfiguration only affects the channel involved in the reconfiguration (the transceiver channel specified by the unique logical channel address), without affecting the remaining transceiver channels controlled by the same dynamic reconfiguration controller. PLL reconfiguration affects all channels that are currently using that PLL for transmission.

Channel reconfiguration from either a transmitter-only configuration to a receiver-only configuration or vice versa is not allowed.

The blocks that are reconfigured by this dynamic reconfiguration mode are the PCS and PMA blocks of a transceiver channel, the clock divider settings of the transmitter and receiver channel, and the CDR and transmitter PLL.

Figure 6–1 shows the functional blocks that you can dynamically reconfigure using transceiver channel and PLL reconfiguration mode.

**Figure 6–1. Transceiver Channel and PLL Reconfiguration in a Transceiver Block**



For more information about the transceiver channel and PLL reconfiguration, refer to the *Transceiver Reconfiguration Controller* chapter of the *Altera Transceiver PHY IP Core User Guide*.

## Document Revision History

Table 6–1 lists the revision history for this chapter.

**Table 6–1. Document Revision History**

Date	Version	Changes
December 2011	2.1	Minor text edits.
November 2011	2.0	<ul style="list-style-type: none"> <li>■ Added “Offset Cancellation Calibration”, “On-Chip Signal Quality Monitoring (EyeQ)”, “Decision Feedback Equalization”, “Adaptive Equalization”, “Enabling and Disabling Loopback Modes”, “Transceiver PLL Reconfiguration”, and “Transceiver Channel and Interface Reconfiguration” sections.</li> <li>■ Minor text edits.</li> </ul>
May 2011	1.2	<ul style="list-style-type: none"> <li>■ Deleted “Indirect Addressing” section and part of introduction.</li> <li>■ Added link to AN 645.</li> <li>■ Chapter moved to Volume 3.</li> </ul>
December 2010	1.1	No changes to the content of this chapter for the Quartus II software 10.1.
July 2010	1.0	Initial release.