

This chapter describes the loopback options on Stratix® V devices, which allow you to verify how different functional blocks work in the transceiver PMA and the standard physical coding sublayer (PCS).

The four available loopback options are:

- “Serial Loopback”—available in all configurations except the PCI Express® (PCIe®) configuration
- “PCIe Reverse Parallel Loopback” on page 5-2—supported in the PCIe configuration only
- “Reverse Serial Loopback” on page 5-3—supported in custom configuration
- “Reverse Serial Pre-CDR Loopback” on page 5-4—supported in custom configuration

Serial Loopback

Figure 5-1 shows the datapath for serial loopback. The data from the FPGA fabric passes through the transmitter channel and is looped back to the receiver channel, bypassing the receiver buffer. The received data is available to the FPGA logic for verification. With this option, you can review how the enabled PCS and physical media attachment (PMA) functional blocks in the transmitter and receiver channel work. Furthermore, you can dynamically enable serial loopback on a channel-by-channel basis.

When you enable serial loopback, the transmitter channel sends the data to both the `tx_serial_data` output port and to the receiver channel. The differential output voltage on the `tx_serial_data` ports is based on the selected differential output voltage (V_{OD}) settings. The looped back data is received by the receiver clock data recovery (CDR) and is retimed through different clock domains. You must provide an alignment pattern for the word aligner to enable the receiver channel to retrieve the byte boundary.

If the device is not in the serial loopback configuration and is receiving data from a remote device, the receiver CDR's recovered clock is locked to the data from that source. If the device is placed in the serial loopback configuration, the data source to the receiver changes from the remote device to the local transmitter channel, which prompts the receiver CDR to start tracking the phase of the new data source. During this time, the receiver CDR's recovered clock may be unstable. As the receiver PCS is running off of this recovered clock, you must place the receiver PCS under reset by asserting the `rx_digitalreset` signal during this time period.


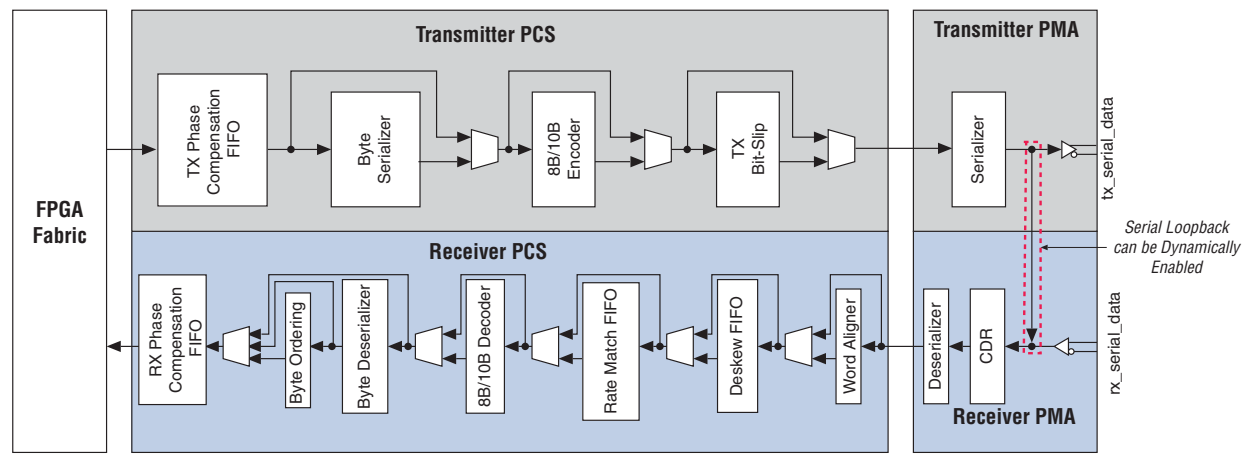

 When moving into or out of serial loopback, you must assert `rx_digitalreset` for a minimum of two parallel clock cycles.


Figure 5-1. Serial Loopback Datapath



 Serial loopback is available for all configurations except the PCIe configuration.

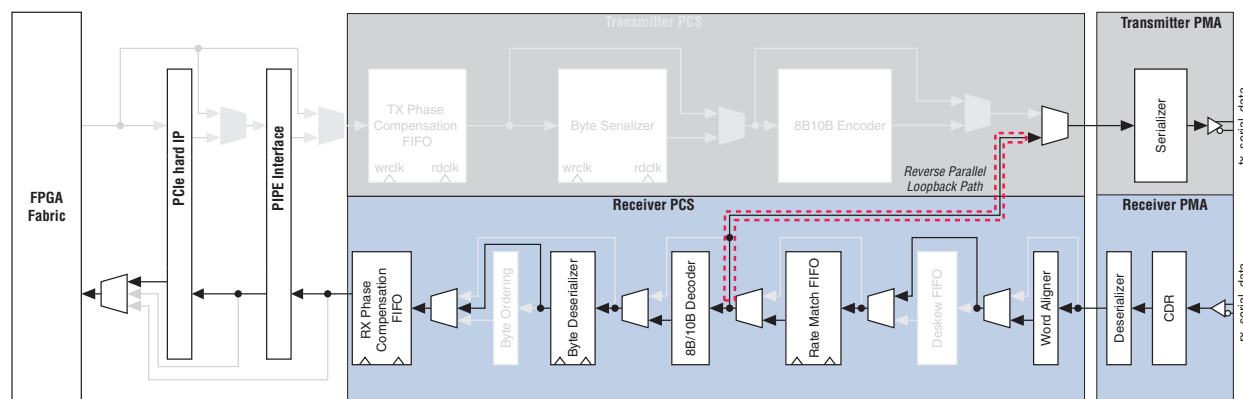
PCIe Reverse Parallel Loopback

PCIe reverse parallel loopback is available only in the PCIe configuration for Gen1 and Gen2 data rates. As shown in [Figure 5-2](#), the received serial data passes through the receiver CDR, deserializer, word aligner, and rate matching FIFO buffer. The data is then looped back to the transmitter serializer and transmitted out through the `tx_serial_data` port. The received data is also available to the FPGA fabric through the `rx_parallel_data` signal. This loopback configuration is designed for the PCIe specification 2.0. To enable this loopback configuration, assert the `tx_detectrxloopback` signal.

 The PCIe reverse parallel loopback is the only loopback option supported in the PCIe configuration. PCIe Reverse Parallel Loopback is not supported in the GT channels of Stratix V GT devices.

For more information, refer to the “PCI Express Reverse Parallel Loopback” section in the *Transceiver Protocol Configuration in Stratix V Devices* chapter.

Figure 5–2. PCIe Reverse Parallel Loopback Configuration Datapath (1)



Note to Figure 5–2:

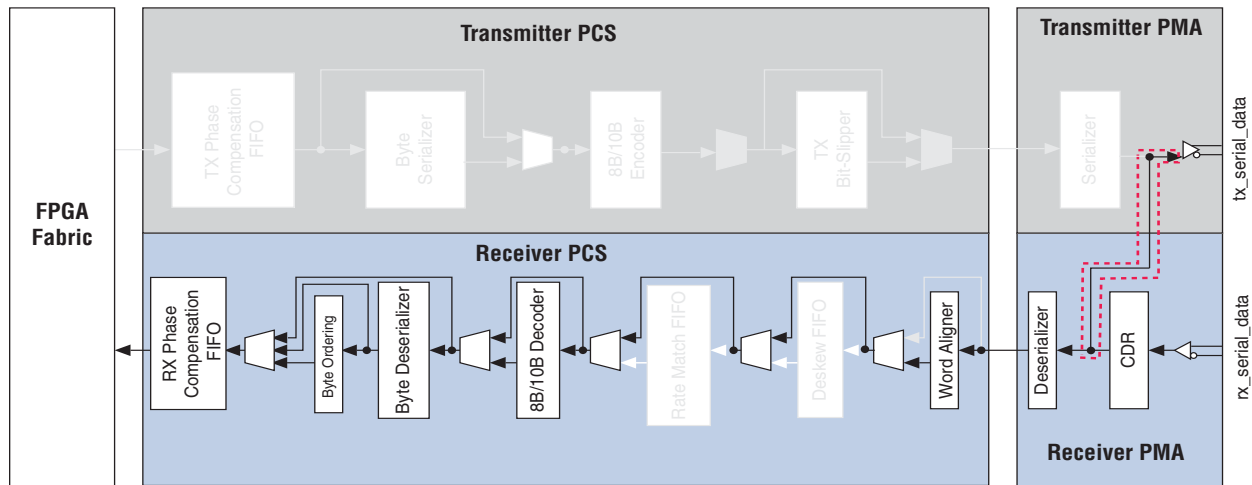
(1) Grayed-out blocks are not active in this configuration.

Reverse Serial Loopback

Reverse serial loopback is available as a subprotocol under custom configuration. In reverse serial loopback, the data is received through the rx_serial_data port, retimed through the receiver CDR, and sent out to the tx_serial_data port. The received data is also available to the FPGA fabric. No dynamic pin control is available to select or deselect reverse serial loopback. Figure 5–3 shows the transceiver channel datapath for reverse serial loopback mode.

The only transmitter channel resource used when implementing reverse serial loopback is the transmitter buffer. You can change the V_{OD} and the pre-emphasis first post tap values on the transmitter buffer through the Custom PHY IP MegaWizard™ Plug-In Manager or through the dynamic reconfiguration controller. Reverse serial loopback is often implemented when using an external bit error rate tester (BERT) on the upstream transmitter.

Figure 5-3. Reverse Serial Loopback Datapath (1)



Note to Figure 5-3:

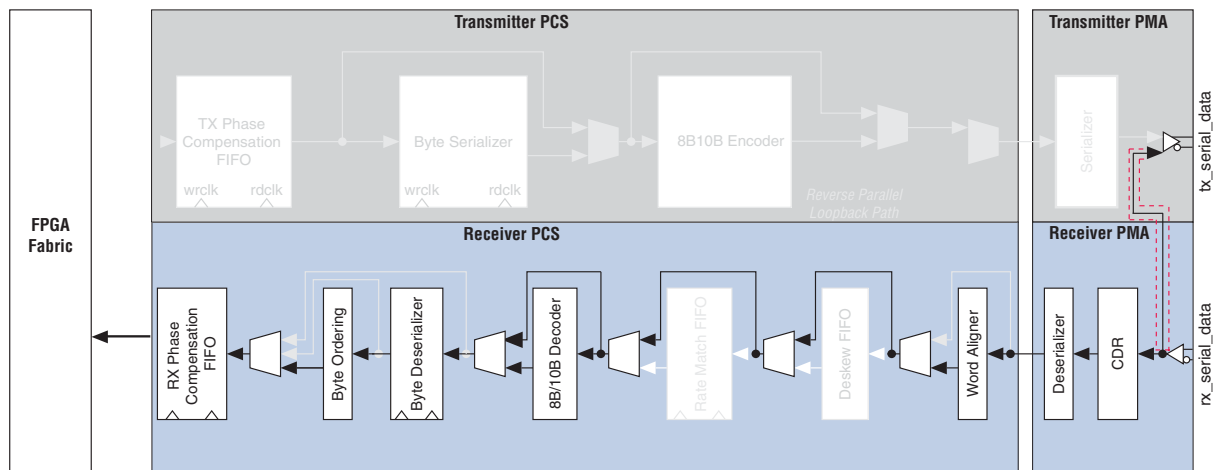
(1) Grayed-out blocks are not active in this configuration.

Reverse Serial Pre-CDR Loopback

Reverse serial pre-CDR loopback is available as a subprotocol under custom configuration. In reverse serial pre-CDR loopback, the data received through the `rx_serial_data` port is looped back to the `tx_serial_data` port *before* the receiver CDR. The received data is also available to the FPGA fabric. Figure 5-4 shows the transceiver channel datapath for reverse serial pre-CDR loopback mode.

The only transmitter channel resource used when implementing reverse serial pre-CDR loopback is the transmitter buffer. You can change the V_{OD} on the transmitter buffer through the Custom PHY IP MegaWizard Plug-In Manager. The receiver data characteristics that are looped back in reverse serial pre-CDR loopback are preserved by the transmitter buffer. The pre-emphasis settings for the transmitter buffer cannot be changed in this configuration.

Figure 5-4. Reverse Serial Pre-CDR Loopback Datapath (1)



Note to Figure 5-4:

(1) Grayed-out blocks are not active in this configuration.

Document Revision History

Table 5-1 lists the revision history for this chapter.

Table 5-1. Document Revision History

Date	Version	Changes
December 2011	2.2	Updated the document to clarify information.
November 2011	2.1	<ul style="list-style-type: none"> ■ This chapter was formerly chapter 6. ■ There are no content changes for this version of the chapter.
May 2011	2.0	<ul style="list-style-type: none"> ■ Added the “Reverse Serial Loopback” and “Reverse Serial Pre-CDR Loopback” sections. ■ Updated Figure 5-2. ■ Updated the chapter title. ■ Chapter moved to Volume 3. ■ Minor text edits.
December 2010	1.1	No changes to the content of this chapter for the Quartus® II software 10.1.
July 2010	1.0	Initial release.

