

This chapter provides information about hot-socketing specifications, power sequencing, power-on reset (POR) requirements, and their implementation in Stratix® V devices.

Stratix V devices offer hot socketing, also known as hot plug-in or hot swap. You can insert or remove a Stratix V device or a board in a system during system operation without causing undesirable effects to the running system bus or board that is inserted into the system, provided that the device's power sequencing requirement is met.

The hot-socketing feature also removes some of the difficulty when using Stratix V devices on PCBs that contain a mixture of 3.0-, 2.5-, 1.8-, 1.5-, 1.35-, 1.25-, 1.20-, and 0.85-V devices.

The Stratix V hot-socketing feature provides the following:

- Board or device insertion and removal without external components or board manipulation
- I/O buffers non-intrusive to system buses during hot insertion

This chapter contains the following sections:

- "Stratix V Hot-Socketing Specifications" on page 8-1
- "Hot-Socketing Feature Implementation in Stratix V Devices" on page 8-3
- "Power Sequencing Requirements" on page 8-4
- "Power-On Reset Circuitry" on page 8-5
- "Power-On Reset Specifications" on page 8-7

Stratix V Hot-Socketing Specifications

Stratix V devices are hot-socketing compliant without the need for external components or special design requirements. The advantages of hot-socketing support in Stratix V devices include the following:

- "Stratix V Devices Can Be Driven Before Power Up"
- "I/O Pins Remain Tri-Stated During Power Up"
- "Insertion or Removal of a Stratix V Device from a Powered-Up System"

Stratix V Devices Can Be Driven Before Power Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix V devices before or during power up or power down without damaging the device. External input signals to I/O pins of the device do not internally power the V_{CCIO} , V_{CCPD} , and V_{CC} power supplies of the device through internal paths within the device.

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing can interrupt the system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Stratix V output buffers are turned off during system power up or power down. Also, the Stratix V device does not drive out until the device is configured and working within the recommended operating conditions.

Insertion or Removal of a Stratix V Device from a Powered-Up System

When powered up through the device signal pins, devices that do not support hot socketing are directly connected to the GND, causing power supplies failure. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

You can insert a Stratix V device into or remove it from a powered-up system board without damaging the system board or interfering with its operation.

The hotsocket circuit monitors the V_{CCIO} , V_{CCPD} , and V_{CC} power supplies. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

You must ensure that all power supplies for Stratix V devices are within the ramp-up and ramp-down rate of 200 μ s to 100 ms.

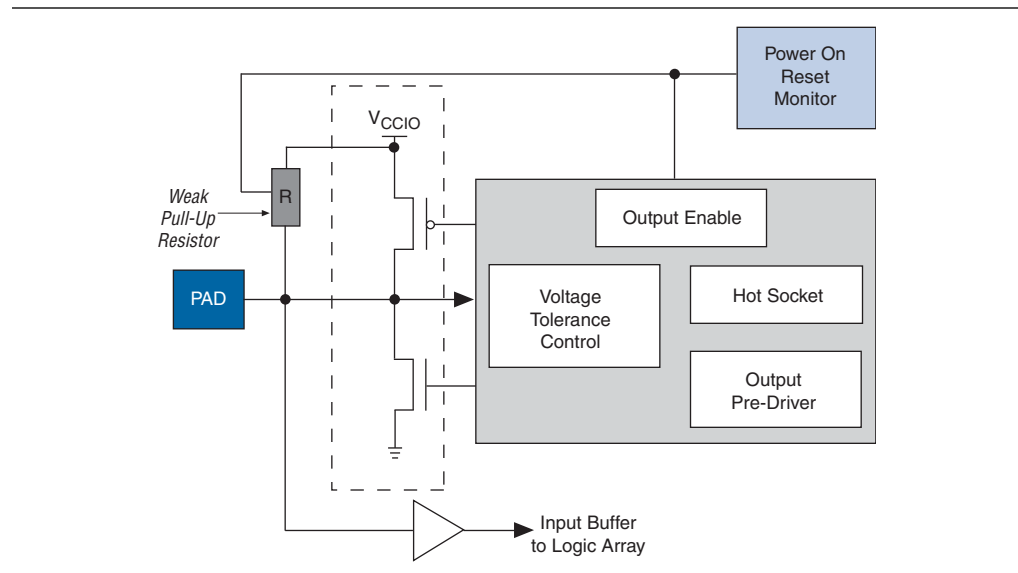
A possible concern regarding hot socketing is the potential for “latch up”. When hot socketing, Stratix V devices are immune to latch up. Latch up occurs when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins can be connected and driven by the active system before the power supply can provide current to the power and GND planes of the device. This condition can lead to latch up and cause a low-impedance path from power to GND within the device. As a result, the device draws a large amount of current, possibly causing electrical damage.

Hot-Socketing Feature Implementation in Stratix V Devices


The hot-socketing feature turns off the output buffer during power up and power down of the V_{CCIO} , V_{CCPD} , and V_{CC} power supplies. When the V_{CCIO} , V_{CCPD} , and V_{CC} power supplies are below the threshold voltage, the hot-socketing circuitry generates an internal `HOTSKT` signal. Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The `CONF_DONE` and `nSTATUS` pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuitry is removed from these configuration pins to ensure that they can operate during configuration. Thus, it is an expected behavior for these pins to drive out during power-up and power-down sequences.


Figure 8-1 shows the I/O pin circuitry for Stratix V devices.

Figure 8-1. Hot-Socketing Circuitry for Stratix V Devices



The POR circuit monitors the voltage level of the power supplies (V_{CC} , V_{CCPGM} , V_{CCPD} , V_{CC_AUX} , V_{CCBAT} , and V_{CCPT}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix V input/output element (IOE) keeps the I/O pins from floating. The 3.0-V tolerance control circuit permits 3.0 V to drive the I/O pins before the V_{CC} , V_{CCPT} , V_{CCPD} , and V_{CCIO} power supplies are powered and prevents the I/O pins from driving out when the device is not in user mode.

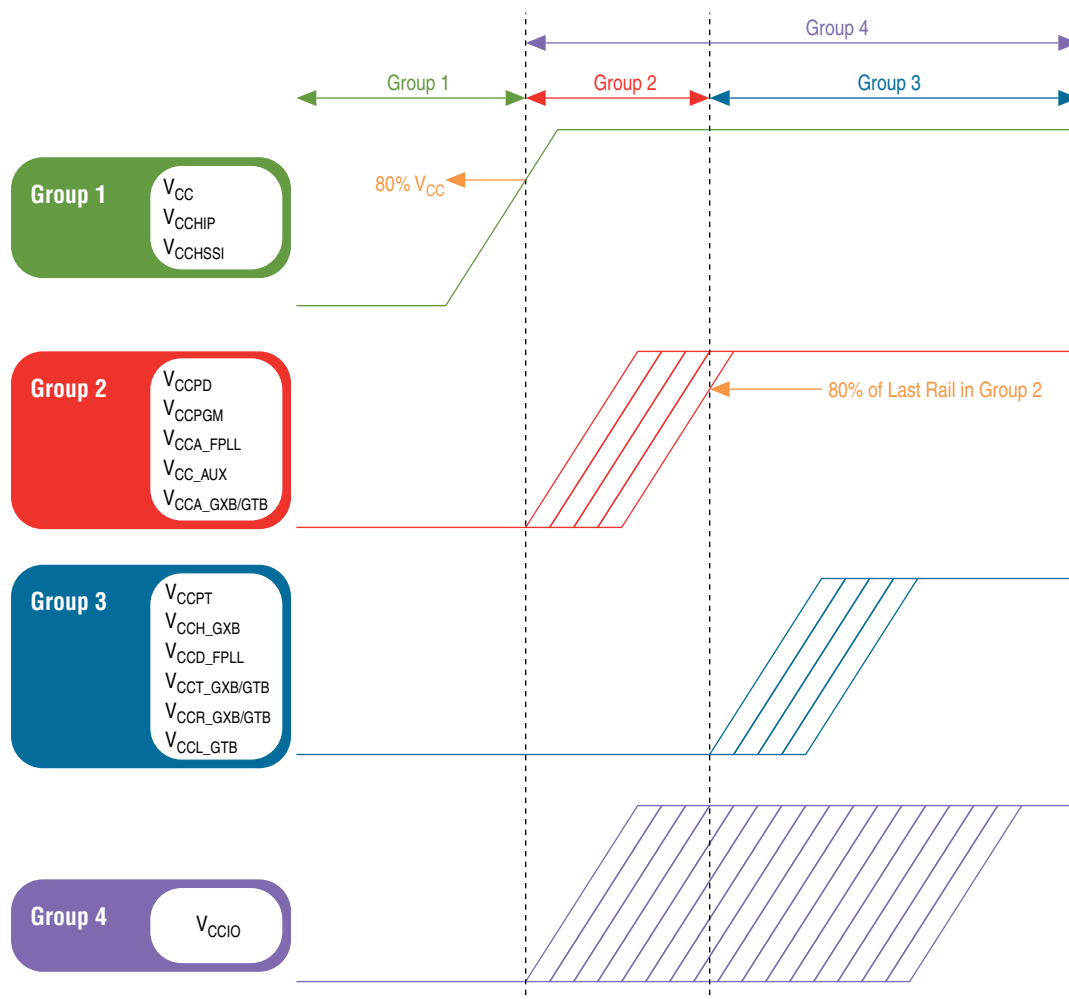
 Altera uses GND as a reference for hot-socketing operations and I/O buffer designs. To ensure proper operation, you must connect the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or over current condition with the Altera® device.

 For the V_{CC_AUX} power supply, POR only monitors one of the V_{CC_AUX} pins. You must connect all the V_{CC_AUX} pins.

Power Sequencing Requirements

Stratix V devices require a power-up sequence as shown in Figure 8-2 to prevent excessive inrush current. This power-up sequence is divided into four power groups. Group 1 contains the first power rails to ramp. The V_{CC} , V_{CCHIP} and V_{CCHSSI} power rails in this group must ramp to a minimum of 80% of their full rail before any other power rails may start. Group 1 power rails can continue to ramp to full rail. The power rails in Group 2 and Group 4 can start to ramp in any order after Group 1 has reached its minimum 80% threshold. When the last power rail in Group 2 reaches 80% of its full rail, the remaining power rails in Group 3 may start their ramp. During this time, Group 2 power rails may continue to ramp to full rail. Power rails in Group 3 may ramp in any order. All power rails must ramp monotonically. The complete power-up sequence must meet either the standard or fast POR delay time, depending on the POR delay setting that is used.

Figure 8-2. Power-Up Sequence Requirement for Stratix V Devices (1), (2), (3)



Notes to Figure 8-2:

- (1) V_{CCBAT} can be powered up at any time.
- (2) If V_{CC} , V_{CCR_GXB} , and V_{CCT_GXB} have the same voltage level, they can be powered by the same regulator in Group 1 and ramp simultaneously.
- (3) All rails can start power-down simultaneously but must reach 0 V within 100 ms.

Stratix V devices may power down all power rails simultaneously. However, all rails must reach 0 V within 100 ms from the start of power-down.

Power-On Reset Circuitry

This section describes POR circuitry in Stratix V devices. POR circuitry keeps the devices in the reset state until the power supply outputs are within operating range.

When power is applied to a Stratix V device, a POR event occurs if the power supply reaches the recommended operating range within the maximum power supply ramp time (t_{RAMP}). If t_{RAMP} is not met, the device I/O pins and programming registers remain tri-stated, during which device configuration could fail. The maximum t_{RAMP} for Stratix V devices is 100 ms; the minimum t_{RAMP} is 200 μ s. All supplies must be strictly monotonic—without plateaus. Set the POR delay by selecting the MSEL pins. The standard or fast POR delay mode that is generated internally from the MSEL decoding block determines the POR delay time, as follows:

- For the standard POR delay mode, the POR delay time is 100 to 300 ms.
- For the fast POR delay mode, the POR delay time is 4 to 12 ms.
- With fast POR, the maximum POR delay width is 12 ms, which leaves enough time after the POR trip for the PCI Express[®] (PCIe[®]) to initialize.

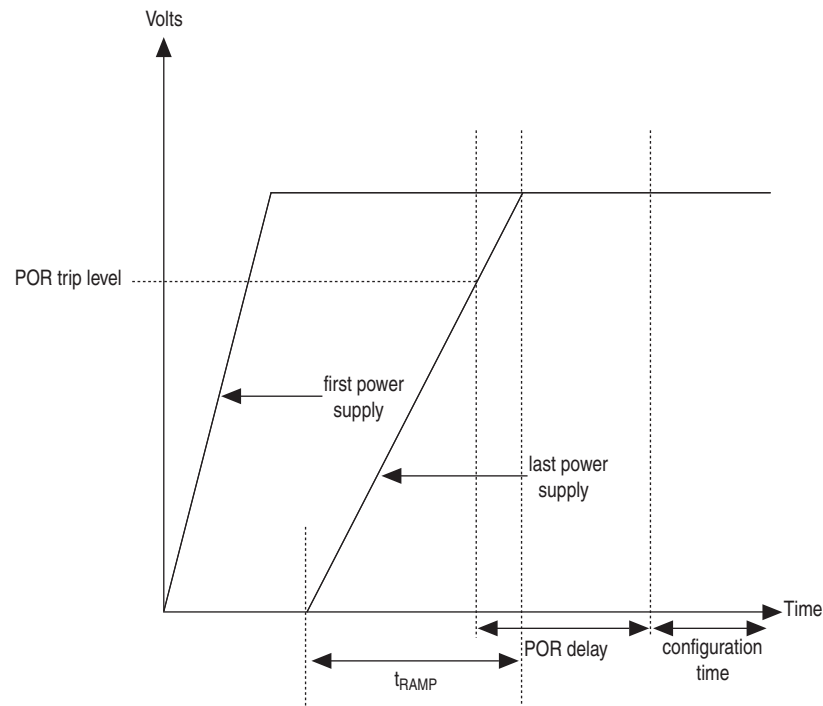
To use Configuration via Protocol (CvP), the total time must be within 10 ms, from the first power supply ramp-up to the last power supply ramp-up.



For more information about the MSEL pin settings, refer to the *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices* chapter.

Figure 8-3 shows the relationship between t_{RAMP} and POR delay.

Figure 8-3. Relationship between t_{RAMP} and POR Delay



The Stratix V POR implements a modularized design structure to monitor the supplies gating the main POR. Each external power supply being monitored has a base POR, which employs a generic design to detect the corresponding voltage level for proper functionality.

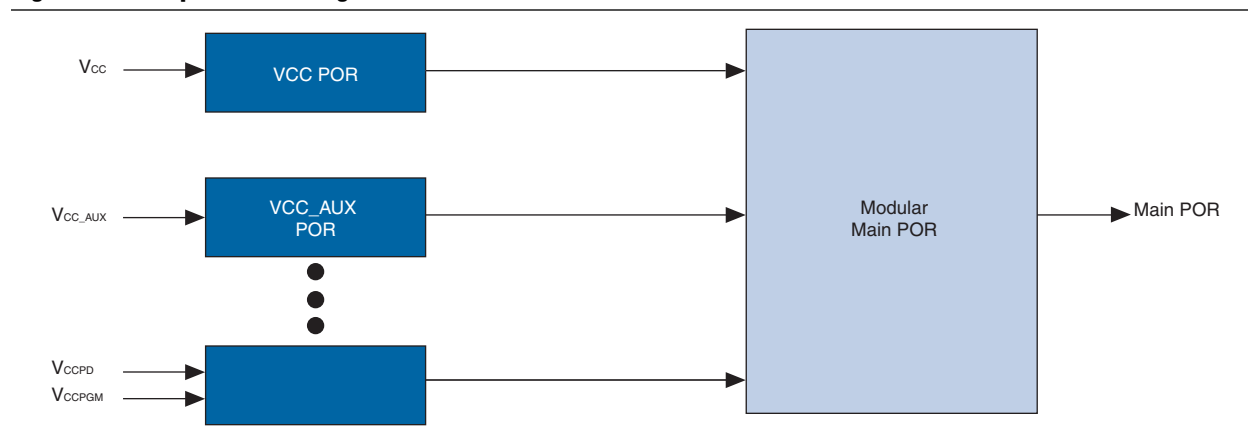
It also checks for functionality of I/O level shifters powered by the V_{CCPD} and V_{CCPGM} power supplies during power-up mode. The main POR waits for all the individual PORs to release the POR signal so that the control block can start programming the device. The Stratix V main POR also employs a modularized structure to enable brown-out detection on a power supply and also to possibly expand the number of power supplies being monitored.



All configuration-related dedicated and dual function I/O pins must be powered by the V_{CCPGM} power supply.

Figure 8-4 shows a simplified POR diagram for Stratix V devices.

Figure 8-4. Simplified POR Diagram for Stratix V Devices



Power-On Reset Specifications

Table 8-1 lists the power supplies that the POR monitors.

Table 8-1. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V _{CC_AUX}	Auxiliary supply for the programmable power technology	2.5
V _{CCBAT}	Battery back-up power supply for design security volatile key register	3.0–1.2
V _{CC}	Core and periphery power supply	0.85
V _{CCPT}	Programmable power technology power supply	1.5
V _{CCPD}	I/O pre-driver power supply	2.5, 3.0
V _{CCPGM}	Configuration pins power supply	1.8, 2.5, 3.0

Table 8-2 lists the power supplies that the POR does not monitor.

Table 8-2. Power Supplies Not Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V _{CCT_GXB}	Transmitter power	0.85, 1.0
V _{CCH_GXB}	Transmitter output buffer power	1.5
V _{CCR_GXB}	Receiver power	0.85, 1.0
V _{CCA_GXB}	Transceiver high voltage power	2.5, 3.0
V _{CCHIP}	Transceiver HIP digital power	0.85
V _{CCIO}	I/O power supply	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0
V _{CCA_FPLL}	PLL analog global power supply	2.5
V _{CCD_FPLL}	PLL digital power supply	1.5

 For more information about the POR specification, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.

Document Revision History

Table 8-3 lists the revision history for this chapter.

Table 8-3. Document Revision History

Date	Version	Changes
November 2011	1.3	<ul style="list-style-type: none"> ■ Added “Power Sequencing Requirements” section. ■ Updated Figure 8-3 and Figure 8-4. ■ Updated Table 8-1. ■ Updated “Hot-Socketing Feature Implementation in Stratix V Devices” and “Power-On Reset Circuitry” sections.
May 2011	1.2	<ul style="list-style-type: none"> ■ Chapter moved to volume 2 for the 11.0 release. ■ Updated “Power-On Reset Circuitry” section. ■ Minor text edits.
December 2010	1.1	No changes to the content of this chapter for the Quartus II software 10.1.
July 2010	1.0	Initial release.