

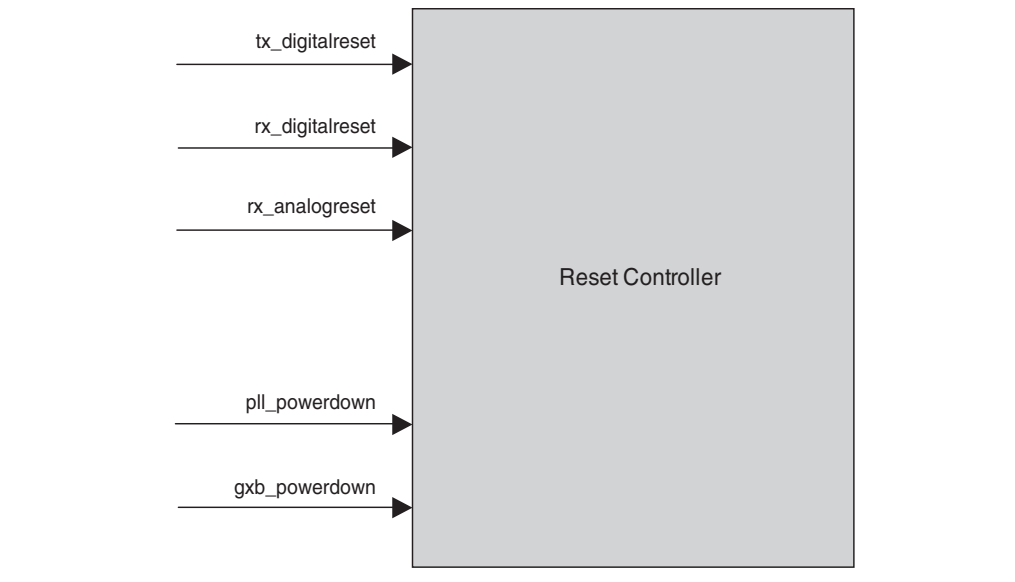
Stratix® IV devices offer multiple reset signals to control the transceiver channels and clock multiplier unit (CMU) phase-locked loops (PLLs) independently. The ALTGX Transceiver MegaWizard™ Plug-In Manager provides individual reset signals for each channel instantiated in your design. It also provides one power-down signal for each transceiver block.

This chapter includes the following sections:

- “User Reset and Power-Down Signals” on page 4-2
- “Transceiver Reset Sequences” on page 4-4
- “PMA Direct Drive Mode Reset Sequences” on page 4-24
- “Dynamic Reconfiguration Reset Sequences” on page 4-36
- “Power Down” on page 4-38
- “Simulation Requirements” on page 4-39
- “Reference Information” on page 4-39

Figure 4-1 shows the reset control and power-down block for a Stratix IV device.

Figure 4-1. Reset Control and Power-Down Block



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User Reset and Power-Down Signals

Each transceiver channel in the Stratix IV device has individual reset signals to reset its physical coding sublayer (PCS) and physical medium attachment (PMA) blocks. Each CMU PLL in the transceiver block has a dedicated reset signal. The transceiver block also has a power-down signal that affects all the channels and CMU PLLs in the transceiver block.



All reset and power-down signals are asynchronous.

Table 4–1 lists the reset signals available for each transceiver channel.

Table 4–1. Transceiver Channel Reset Signals

Signal	ALTGX MegaWizard Plug-In Manager Configurations	Description
tx_digitalreset (1)	<ul style="list-style-type: none"> ■ Transmitter Only ■ Receiver and Transmitter 	<p>Provides asynchronous reset to all digital logic in the transmitter PCS, including the XAUI transmit state machine.</p> <p>The minimum pulse width for this signal is two parallel clock cycles.</p>
rx_digitalreset (1)	<ul style="list-style-type: none"> ■ Receiver Only ■ Receiver and Transmitter 	<p>Resets all digital logic in the receiver PCS, including:</p> <ul style="list-style-type: none"> ■ XAUI receiver state machines ■ GIGE receiver state machines ■ XAUI channel alignment state machine ■ BIST-PRBS verifier ■ BIST-incremental verifier <p>The minimum pulse width for this signal is two parallel clock cycles.</p>
rx_analogreset	<ul style="list-style-type: none"> ■ Receiver Only ■ Receiver and Transmitter 	<p>Resets the receiver CDR present in the receiver channel.</p> <p>The minimum pulse width is two parallel clock cycles.</p>

Note to Table 4–1:

- (1) Assert this signal until the clocks coming out of the transmitter PLL and receiver CDR are stabilized. Stable parallel clocks are essential for proper operation of the transmitter and receiver phase-compensation FIFOs in the PCS.


Table 4-2 lists the power-down signals available for each CMU PLL transceiver block.


Table 4-2. Transceiver Block Power-Down Signals

Signal	Description
pll_powerdown (1)	Each transceiver block has two CMU PLLs. Each CMU PLL has this dedicated power-down signal. This signal powers down the CMU PLLs that provide high-speed serial and low-speed parallel clocks to the transceiver channels.
gxb_powerdown (1)	Powers down the entire transceiver block. When this signal is asserted, it powers down: <ul style="list-style-type: none"> the PCS and PMA in all the transceiver channels the CMU PLLs This signal operates independently from the other reset signals and is common to the transceiver block.
pll_locked	A status signal. Indicates the status of the transmitter PLL. <ul style="list-style-type: none"> A high level—the transmitter PLL is locked to the incoming reference clock frequency. When <code>pll_locked</code> is high, <code>tx_digitalreset</code> must always be asserted. To de-assert <code>tx_digitalreset</code>, follow the initialization reset sequence for your specific mode.
rx_pll_locked	A status signal. <ul style="list-style-type: none"> A high level—the receiver CDR is locked to the incoming reference clock frequency.
rx_freqlocked	A status signal. Indicates the status of the receiver CDR lock mode. <ul style="list-style-type: none"> A high level—the receiver is in lock-to-data (LTD) mode. A low level—the receiver CDR is in lock-to-reference (LTR) mode. In automatic lock mode, when <code>rx_freqlocked</code> is low, <code>rx_digitalreset</code> must always be asserted. To de-assert <code>rx_digitalreset</code>, follow the initialization reset sequence for your specific mode.
busy	A status signal. An output from the ALTGX_RECONFIG block indicates the status of the dynamic reconfiguration controller. This signal remains low for the first <code>reconfig_clk</code> clock cycle after power up. It then is asserted from the second <code>reconfig_clk</code> clock cycle. Assertion on this signal indicates that the offset cancellation process is being executed on the receiver buffer as well as the receiver CDR. When this signal is de-asserted, it indicates that offset cancellation is complete.

Note to Table 4-2:

(1) The `refclk` (`refclk0` or `refclk1`) buffer is not powered down by this signal.

 For more information about offset cancellation, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

 If none of the channels is instantiated in a transceiver block, the Quartus® II software automatically powers down the entire transceiver block.

Blocks Affected by the Reset and Power-Down Signals

Table 4-3 lists the blocks that are affected by specific reset and power-down signals.

Table 4-3. Blocks Affected by Reset and Power-Down Signals (Part 1 of 2)

Transceiver Block	rx_digitalreset	rx_analogreset	tx_digitalreset	pll_powerdown	gxb_powerdown
CMU PLLs	—	—	—	Y	Y
Transmitter Phase Compensation FIFO	—	—	Y	—	Y

Table 4-3. Blocks Affected by Reset and Power-Down Signals (Part 2 of 2)

Transceiver Block	rx_digitalreset	rx_analogreset	tx_digitalreset	pll_powerdown	gxb_powerdown
Byte Serializer	—	—	Y	—	Y
8B/10B Encoder	—	—	Y	—	Y
Serializer	—	—	Y	—	Y
Transmitter Buffer	—	—	—	—	Y
Transmitter XAUI State Machine	—	—	Y	—	Y
Receiver Buffer	—	—	—	—	Y
Receiver CDR	—	Y	—	—	Y
Receiver Deserializer	—	—	—	—	Y
Receiver Word Aligner	Y	—	—	—	Y
Receiver Deskew FIFO	Y	—	—	—	Y
Receiver Clock Rate Compensation FIFO	Y	—	—	—	Y
Receiver 8B/10B Decoder	Y	—	—	—	Y
Receiver Byte Deserializer	Y	—	—	—	Y
Receiver Byte Ordering	Y	—	—	—	Y
Receiver Phase Compensation FIFO	Y	—	—	—	Y
Receiver XAUI State Machine	Y	—	—	—	Y
BIST Verifiers	Y	—	—	—	Y

Transceiver Reset Sequences

You can configure transceiver channels in Stratix IV devices in various configurations. In all functional modes except XAUI functional mode, transceiver channels can be either bonded or non-bonded. In XAUI functional mode, transceiver channels must be bonded. In PCI Express® (PCIe) functional mode, transceiver channels can be either bonded or non-bonded and need to follow a specific reset sequence.

The two categories of reset sequences for Stratix IV devices described in this chapter are:

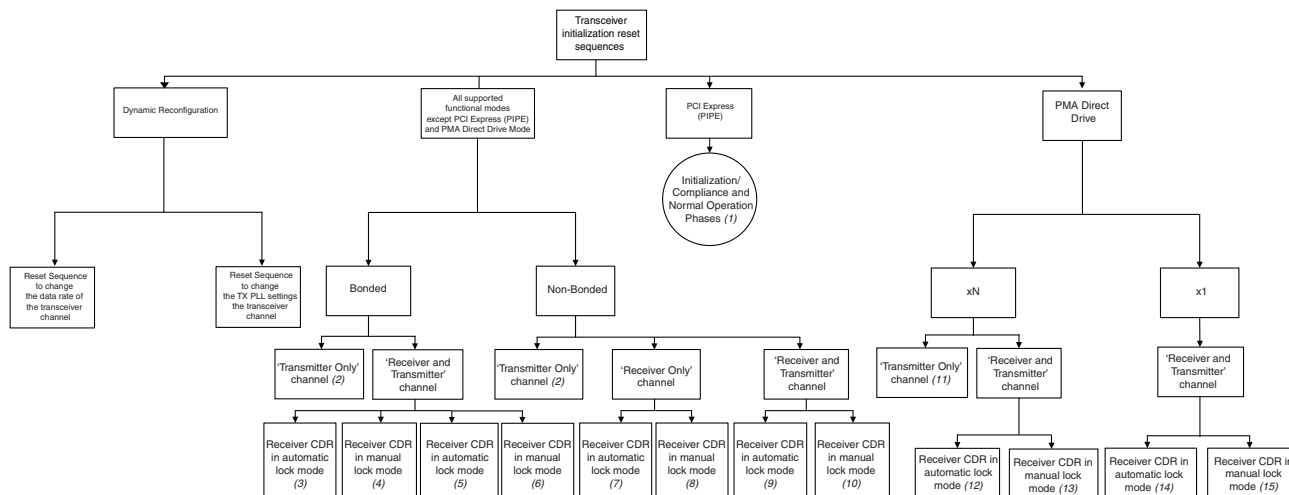
- [“All Supported Functional Modes Except PCIe Functional Mode” on page 4-6](#)—describes the reset sequences in bonded and non-bonded configurations.
- [“PCIe Functional Mode” on page 4-22](#)—describes the reset sequence for the initialization/compliance phase and the normal operation phase in PCIe functional modes.

The busy signal remains low for the first `reconfig_clk` clock cycle. It then is asserted from the second `reconfig_clk` clock cycle. Subsequent de-assertion of the busy signal indicates the completion of the offset cancellation process. This busy signal is required in transceiver reset sequences except for **Transmitter Only** channel configurations. For more information, refer to the reset sequences shown in Figure 4-2 and the associated references listed in the figure notes.

Altera strongly recommends adhering to these reset sequences for proper operation of the Stratix IV transceiver.

Figure 4-2 shows the transceiver reset sequences for Stratix IV devices.

Figure 4-2. Transceiver Reset Sequences Chart



Notes to Figure 4-2:

- (1) Refer to the Timing Diagram in Figure 4-12.
- (2) Refer to the Timing Diagram in Figure 4-3.
- (3) Refer to the Timing Diagram in Figure 4-4.
- (4) Refer to the Timing Diagram in Figure 4-5.
- (5) Refer to the Timing Diagram in Figure 4-6.
- (6) Refer to the Timing Diagram in Figure 4-7.
- (7) Refer to the Timing Diagram in Figure 4-8.
- (8) Refer to the Timing Diagram in Figure 4-9.
- (9) Refer to the Timing Diagram in Figure 4-10.
- (10) Refer to the Timing Diagram in Figure 4-11.
- (11) Refer to the Timing Diagram in Figure 4-13.
- (12) Refer to the Timing Diagram in Figure 4-16.
- (13) Refer to the Timing Diagram in Figure 4-17.
- (14) Refer to the Timing Diagram in Figure 4-18.
- (15) Refer to the Timing Diagram in Figure 4-19.

All Supported Functional Modes Except PCIe Functional Mode

This section describes reset sequences for transceiver channels in bonded and non-bonded configurations. Timing diagrams of some typical configurations are shown to facilitate proper reset sequence implementation. In these functional modes, you can set the receiver CDR either in automatic lock or manual lock mode.



In manual lock mode, the receiver CDR locks to the reference clock (lock-to-reference) or the incoming serial data (lock-to-data), depending on the logic levels on the `rx_locktorefclk` and `rx_locktodata` signals. With the receiver CDR in manual lock mode, you can either configure the transceiver channels in the Stratix IV device in a non-bonded configuration or a bonded configuration. In a bonded configuration, for example in XAUI mode, four channels are bonded together.

Table 4-4 lists the lock-to-reference (LTR) and lock-to-data (LTD) controller lock modes for the `rx_locktorefclk` and `rx_locktodata` signals.

Table 4-4. Lock-To-Reference and Lock-To-Data Modes

<code>rx_locktorefclk</code>	<code>rx_locktodata</code>	LTR/LTD Controller Lock Mode
1	0	Manual, LTR Mode
—	1	Manual, LTD Mode
0	0	Automatic Lock Mode

Bonded Channel Configuration

In a bonded channel configuration, you can reset all the bonded channels simultaneously. Examples of bonded channel configurations are XAUI, PCIe, and Basic $\times 4$ functional modes. In Basic $\times 4$ functional mode, you can bond **Transmitter Only** channels together.

In XAUI mode, the receiver and transmitter channels are bonded. Each of the receiver channels in this mode has its own output status signals, `rx_pll_locked` and `rx_freqlocked`. You must consider the timing of these signals in the reset sequence.

Table 4-5 lists the reset and power-down sequences for bonded configurations under the stated functional modes.

Table 4-5. Reset and Power-Down Sequences for Bonded Channel Configurations

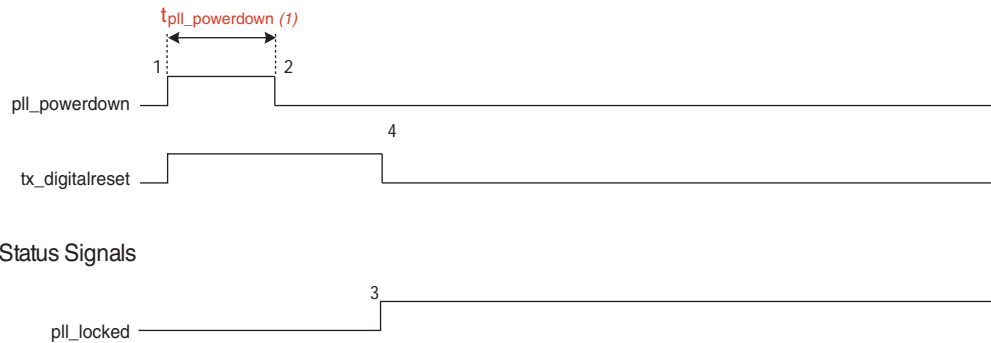
Channel Set Up	Receiver CDR Mode	Refer to
Transmitter Only	Basic $\times 4$	“Transmitter Only Channel” on page 4-7
Receiver and Transmitter	Automatic lock mode for XAUI functional mode	“Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode” on page 4-8
Receiver and Transmitter	Manual lock mode for XAUI functional mode	“Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode” on page 4-10
Receiver and Transmitter	Automatic lock mode for Basic $\times 8$ functional mode	“Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode” on page 4-12
Receiver and Transmitter	Manual lock mode for Basic $\times 8$ functional mode	“Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode” on page 4-14

Transmitter Only Channel

This configuration contains only a transmitter channel. If you create a **Transmitter Only** instance in the ALTGX MegaWizard Plug-In Manager in Basic ×4 functional mode, use the reset sequence shown in [Figure 4-3](#).

Figure 4-3. Sample Reset Sequence for Four Transmitter Only Channels

Reset and Power-Down Signals



Output Status Signals

Note to Figure 4-3:

(1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

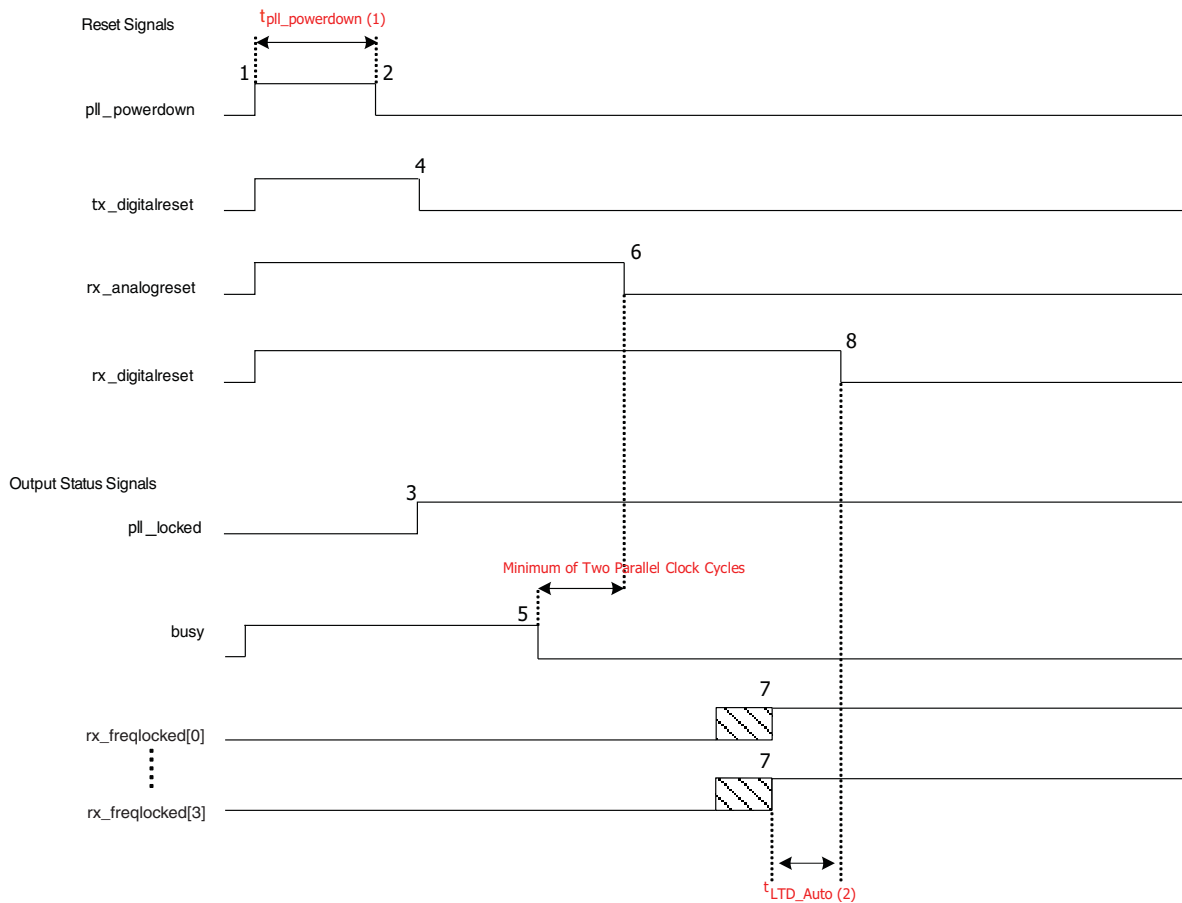
As shown in [Figure 4-3](#), for the **Transmitter Only** channel configuration, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset` signal asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. When the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), de-assert the `tx_digitalreset` signal (marker 4). At this point, the transmitter is ready for transmitting data.

Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode

This configuration contains both a transmitter and receiver channel. For XAUI functional mode, with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 4-4.

Figure 4-4. Sample Reset Sequence for Four Receiver and Transmitter Channels—Receiver CDR in Automatic Lock Mode

**Notes to Figure 4-4:**

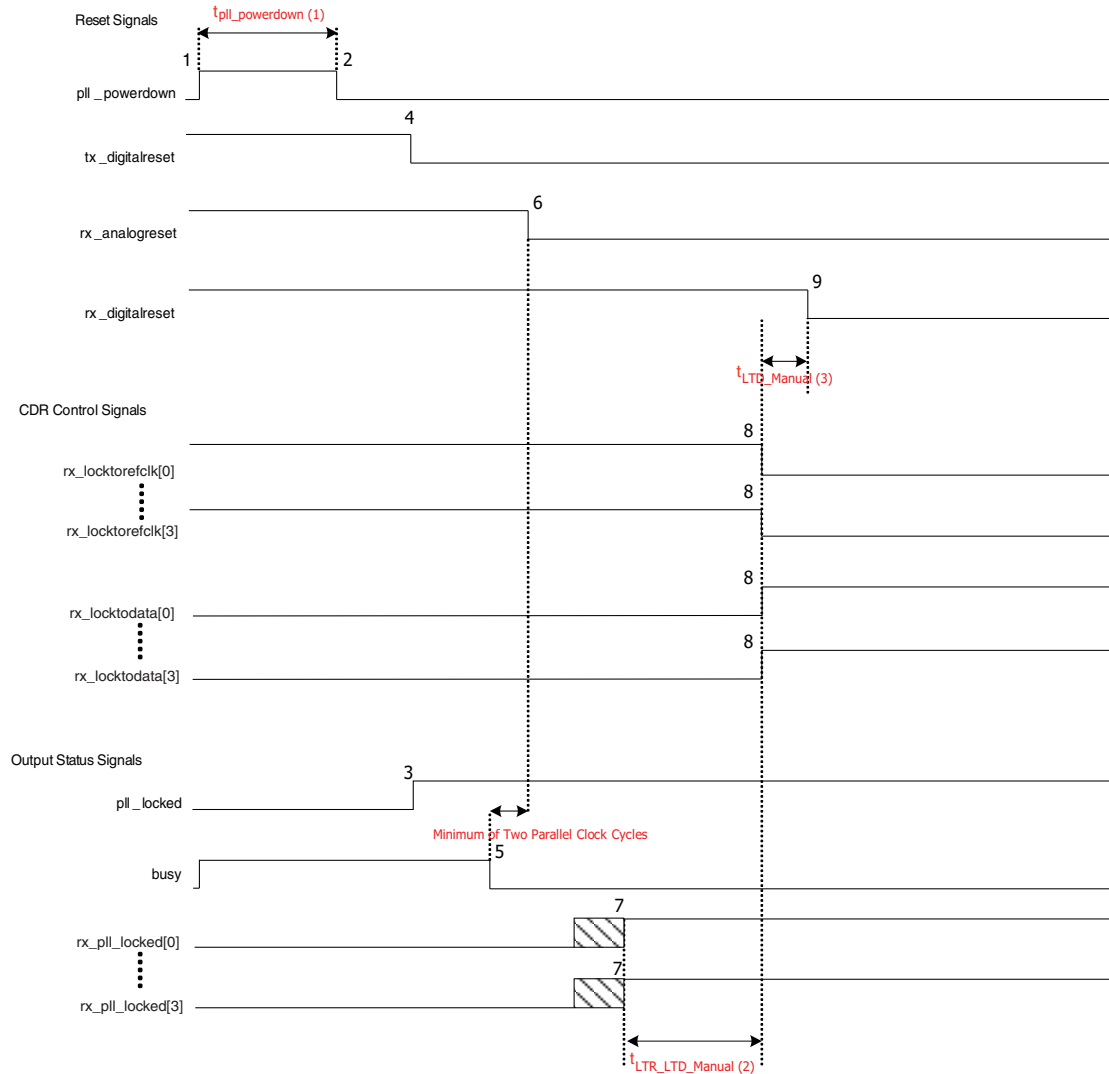
- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-4, for the receiver CDR in automatic lock mode configuration, follow these reset steps:

1. After power up, assert `p11_powerdown` for a minimum period of $t_{p11_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, and `rx_digitalreset` signals asserted during this time period. After you de-assert the `p11_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `p11_locked` signal going high, de-assert the `tx_digitalreset` signal. At this point, the transmitter is ready for data traffic.
4. For the receiver operation, after de-assertion of busy signal, wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signal. After `rx_analogreset` is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock.
5. Wait for the `rx_freqlocked` signal from each channel to go high. The `rx_freqlocked` signal of each channel may go high at different times (indicated by the slashed pattern at marker 7).
6. In a bonded channel group, when the `rx_freqlocked` signals of all the channels has gone high, from that point onwards, wait for at least t_{LTD_Auto} for the receiver parallel clock to be stable, then de-assert the `rx_digitalreset` signal (marker 8). At this point, all the receivers are ready for data traffic. Note that `rx_digitalreset` must not be released if there is no data present at the receiver pins to avoid overflow/underflow of the phase compensation FIFOs.

Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. For XAUI functional mode, with the receiver CDR in manual lock mode, use the reset sequence shown in Figure 4-5.

Figure 4-5. Sample Reset Sequence for Four Receiver and Transmitter Channels—Receiver CDR in Manual Lock Mode**Notes to Figure 4-5:**

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For $t_{LTR_LTD_Manual}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (3) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

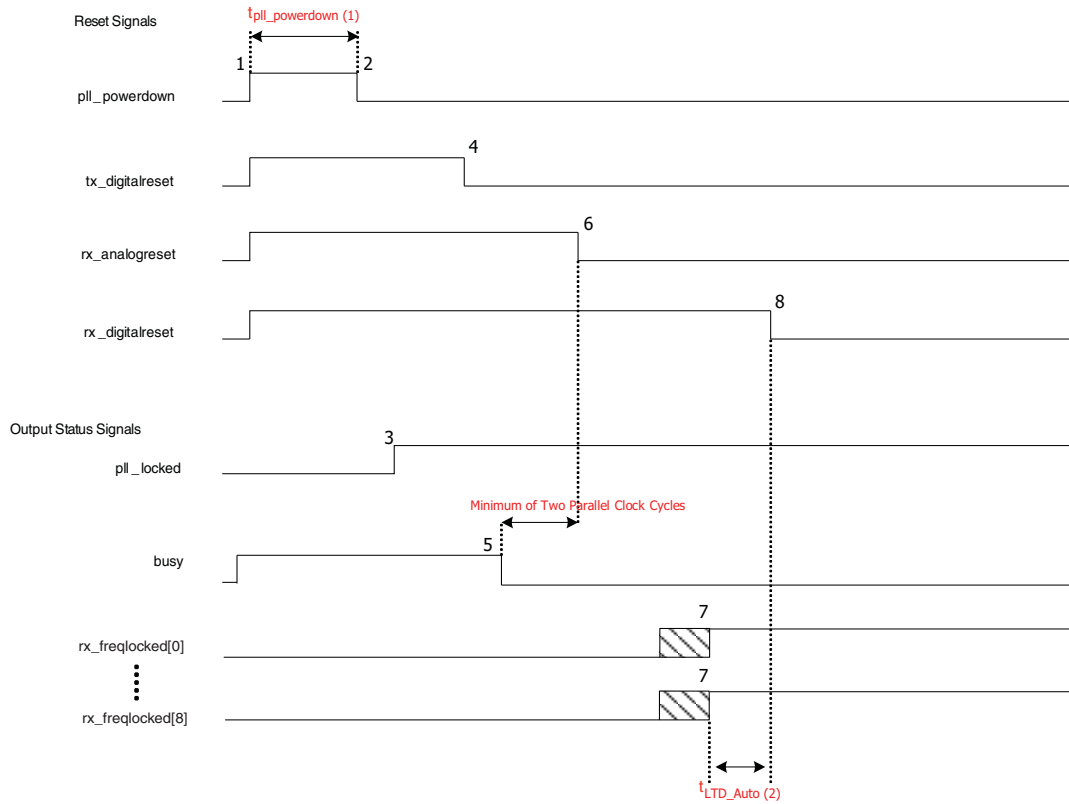
As shown in Figure 4-5, for the receiver CDR in manual lock mode configuration, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, and `rx_locktoefclk` signals asserted and the `rx_locktodata` signal de-asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), de-assert the `tx_digitalreset` signal (marker 4). For the receiver operation, after de-assertion of the busy signal, wait for a minimum of **two parallel clock cycles** to de-assert the `rx_analogreset` signal. After the `rx_analogreset` signal is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock because `rx_locktoefclk` is asserted.
4. Wait for the `rx_pll_locked` signal from each channel to go high. The `rx_pll_locked` signal of each channel may go high at different times with respect to each other (indicated by the slashed pattern at marker 7).
5. In a bonded channel group, when the `rx_pll_locked` signal of all the channels have gone high, from that point onwards, wait for at least $t_{LTR_LTD_Manual}$, then de-assert `rx_locktoefclk` and assert `rx_locktodata` (marker 8). At this point, the receiver CDR of all the channels enters into lock-to-data mode and starts locking to the received data.
6. After asserting the `rx_locktodata` signal, wait for at least t_{LTD_Manual} before de-asserting `rx_digitalreset` (the time between markers 8 and 9).

Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode

This configuration contains both a transmitter and a receiver channel. For Basic $\times 8$ functional mode, with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 4-6.

Figure 4-6. Sample Reset Sequence for Eight Receiver and Transmitter Channels—Receiver CDR in Automatic Lock Mode

**Notes to Figure 4-6:**

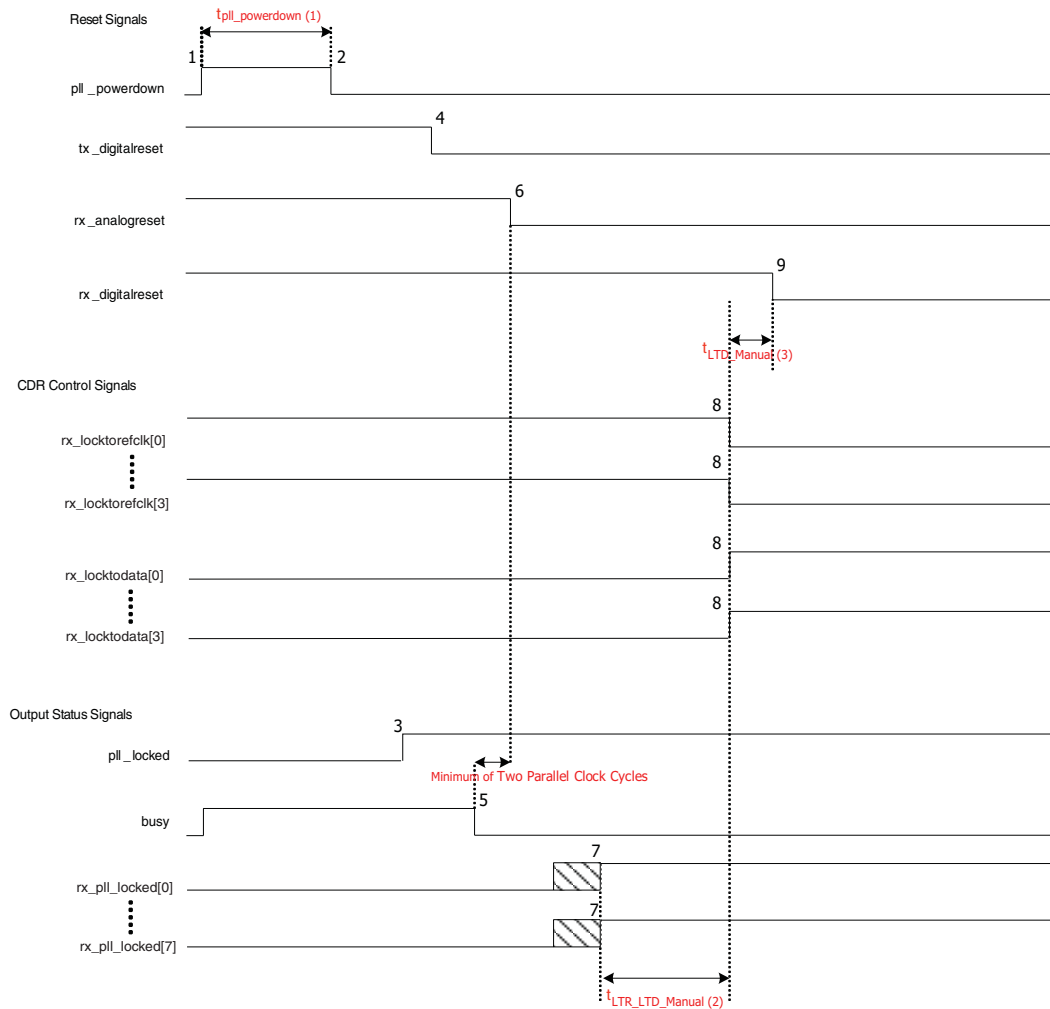
- (1) For $t_{\text{pll_powerdown}}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For $t_{\text{LTD_Auto}}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-6, for the receiver CDR in automatic lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, and `rx_digitalreset` signals asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `pll_locked` signal going high, de-assert the `tx_digitalreset` signal. At this point, the transmitter is ready for data traffic.
4. For the receiver operation, after de-assertion of the busy signal, wait for a minimum of **two parallel clock cycles** to de-assert the `rx_analogreset` signal. After `rx_analogreset` is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock.
5. Wait for the `rx_freqlocked` signal from each channel to go high. The `rx_freqlocked` signal of each channel may go high at different times (indicated by the slashed pattern at marker 7).
6. In a bonded channel group, when the `rx_freqlocked` signals of all the channels have gone high, from that point onwards, wait for at least t_{LTD_Auto} for the receiver parallel clock to stabilize, then de-assert the `rx_digitalreset` signal (marker 8). At this point, all the receivers are ready for data traffic. Note that `rx_digitalreset` must not be released if there is no data present at the receiver pins to avoid overflow/underflow of the phase compensation FIFOs.

Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. For Basic $\times 8$ functional mode, with the receiver CDR in manual lock mode, use the reset sequence shown in Figure 4-7.

Figure 4-7. Sample Reset Sequence for Eight Receiver and Transmitter Channels—Receiver CDR in Manual Lock Mode**Notes to Figure 4-7:**

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For $t_{LTR_LTD_Manual}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (3) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-7, for the receiver CDR in manual lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, and `rx_locktorefclk` signals asserted and the `rx_locktodata` signal de-asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), de-assert the `tx_digitalreset` signal (marker 4). For the receiver operation, after de-assertion of the busy signal, wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signal. After the `rx_analogreset` signal is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock because `rx_locktorefclk` is asserted.
4. Wait for the `rx_pll_locked` signal from each channel to go high. The `rx_pll_locked` signal of each channel may go high at different times with respect to each other (indicated by the slashed pattern at marker 7).
5. In a bonded channel group, when the `rx_pll_locked` signal of all the channels has gone high, from that point onwards, wait for at least $t_{LTR_LTD_Manual}$, then de-assert `rx_locktorefclk` and assert `rx_locktodata` (marker 8). At this point, the receiver CDR of all the channels enters into lock-to-data mode and starts locking to the received data.
6. De-assert `rx_digitalreset` at least t_{LTD_Manual} (the time between markers 8 and 9) after asserting the `rx_locktodata` signal.

Non-Bonded Channel Configuration

In non-bonded channels, each channel in the ALTGX MegaWizard Plug-In Manager instance contains its own `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, `rx_pll_locked`, and `rx_freqlocked` signals.

You can reset each channel independently. For example, if there are four non-bonded channels, the ALTGX MegaWizard Plug-In Manager provides four each of the following signals: `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, `rx_pll_locked`, and `rx_freqlocked`.

Table 4-6 lists the reset and power-down sequences for one channel in a non-bonded configuration under the stated functional modes.

Table 4-6. Reset and Power-Down Sequences for Bonded Channel Configurations (Part 1 of 2)

Channel Set Up	Receiver CDR Mode	Refer to
Transmitter Only	Basic x4	"Transmitter Only Channel" on page 4-16
Receiver Only	Automatic lock mode	"Receiver Only Channel—Receiver CDR in Automatic Lock Mode" on page 4-16
Receiver Only	Manual lock mode	"Receiver Only Channel—Receiver CDR in Manual Lock Mode" on page 4-17

Table 4-6. Reset and Power-Down Sequences for Bonded Channel Configurations (Part 2 of 2)

Channel Set Up	Receiver CDR Mode	Refer to
Receiver and Transmitter	Automatic lock mode	“Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode” on page 4-18
Receiver and Transmitter	Manual lock mode	“Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode” on page 4-20



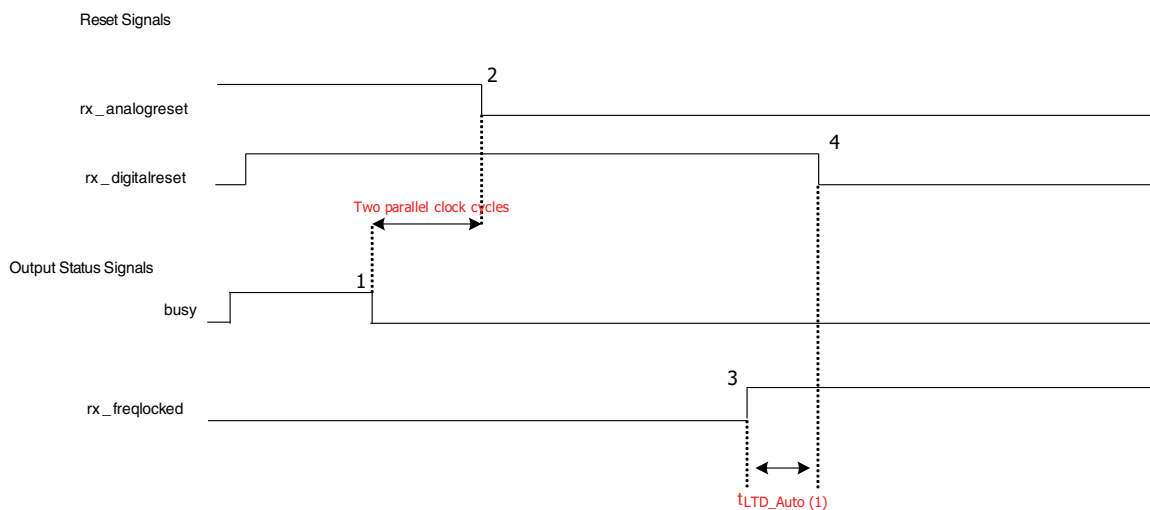
Follow the same reset sequence for all the other channels in the non-bonded configuration.

Transmitter Only Channel

This configuration contains only a transmitter channel. If you create a **Transmitter Only** instance in the ALTGX MegaWizard Plug-In Manager, use the same reset sequence shown in [Figure 4-3 on page 4-7](#).

Receiver Only Channel—Receiver CDR in Automatic Lock Mode

This configuration contains only a receiver channel. If you create a **Receiver Only** instance in the ALTGX MegaWizard Plug-In Manager with the receiver CDR in automatic lock mode, use the reset sequence shown in [Figure 4-8](#).

Figure 4-8. Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Automatic Lock Mode

Note to Figure 4-8:

(1) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

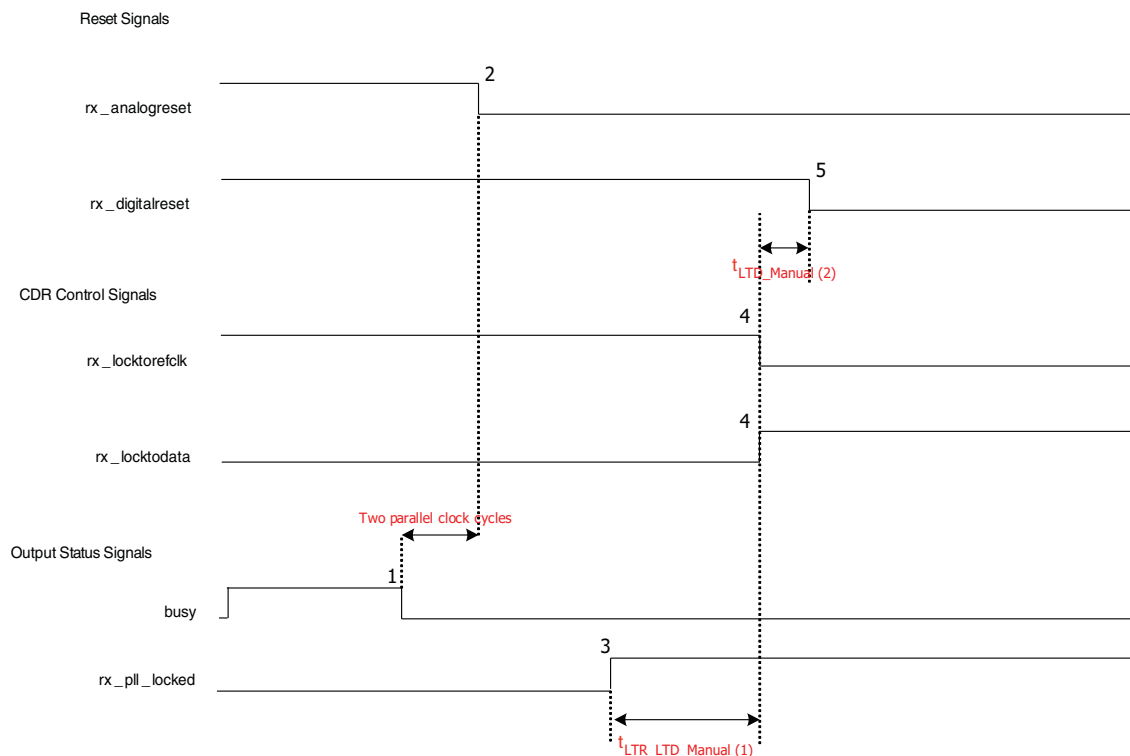
As shown in Figure 4-8, for the receiver in CDR automatic lock mode, follow these reset steps:

1. After power up, wait for the busy signal to be de-asserted.
2. De-assert the rx_analogreset signal.
3. Keep the rx_digitalreset signal asserted during this time period. After you de-assert the rx_analogreset signal, the receiver CDR starts locking to the receiver input reference clock.
4. Wait for the rx_freqlocked signal to go high.
5. When rx_freqlocked goes high (marker 3), from that point onwards, wait for at least t_{LTD_Auto} , then de-assert the rx_digitalreset signal (marker 4). At this point, the receiver is ready to receive data.

Receiver Only Channel—Receiver CDR in Manual Lock Mode

This configuration contains only a receiver channel. If you create a **Receiver Only** instance in the ALTGX MegaWizard Plug-In Manager with receiver CDR in manual lock mode, use the reset sequence shown in Figure 4-9.

Figure 4-9. Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Manual Lock Mode



Notes to Figure 4-9:

- (1) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

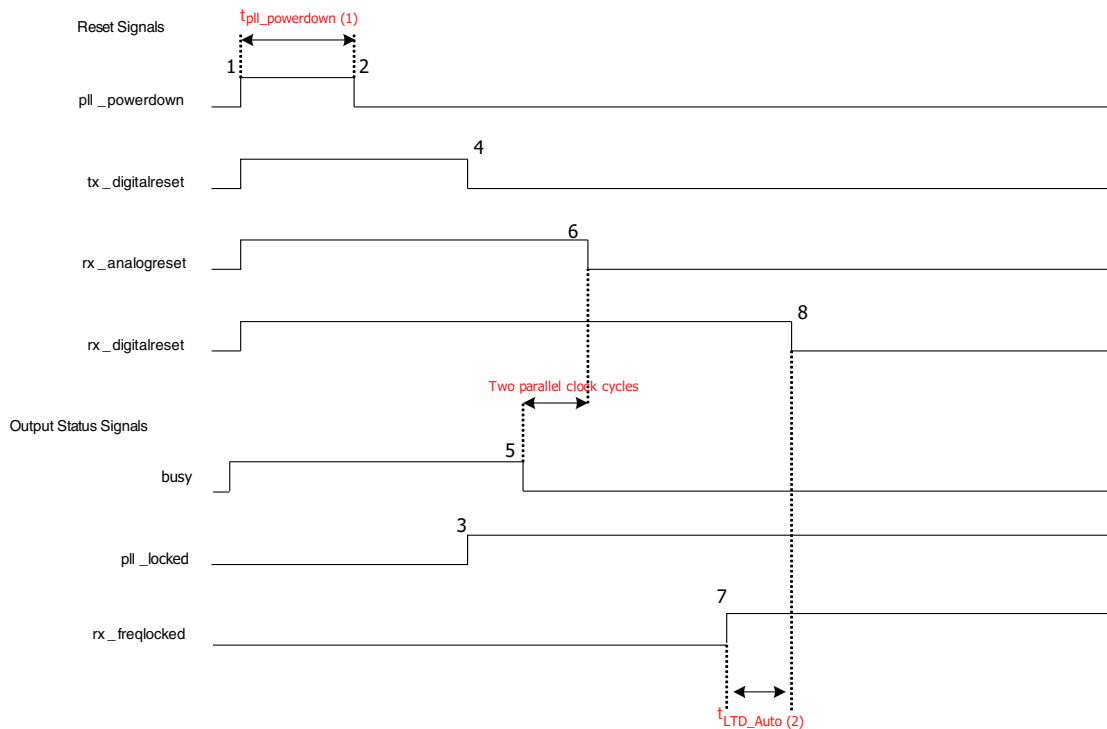
As shown in Figure 4-9, for the receiver CDR in manual lock mode, follow these reset steps:

1. After power up, wait for the busy signal to be asserted.
2. Keep the rx_digitalreset and rx_locktoefclk signals asserted and the rx_locktoedata signal de-asserted during this time period.
3. After de-assertion of the busy signal, de-assert the rx_analogreset signal. The receiver CDR then starts locking to the receiver input reference clock because the rx_locktoefclk signal is asserted.
4. Wait for at least $t_{LTR_LTD_Manual}$ time (the time between markers 3 and 4) after the rx_pll_locked signal goes high and then de-assert the rx_locktoefclk signal. At the same time, assert the rx_locktoedata signal (marker 4). At this point, the receiver CDR enters lock-to-data mode and the receiver PLL starts locking to the received data.
5. De-assert rx_digitalreset at least t_{LTD_Manual} (the time between markers 4 and 5) after asserting the rx_locktoedata signal.

Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode

This configuration contains both a transmitter and a receiver channel. If you create a **Receiver and Transmitter** instance in the ALTGX MegaWizard Plug-In Manager with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 4-10.

Figure 4-10. Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode



Notes to Figure 4-10:

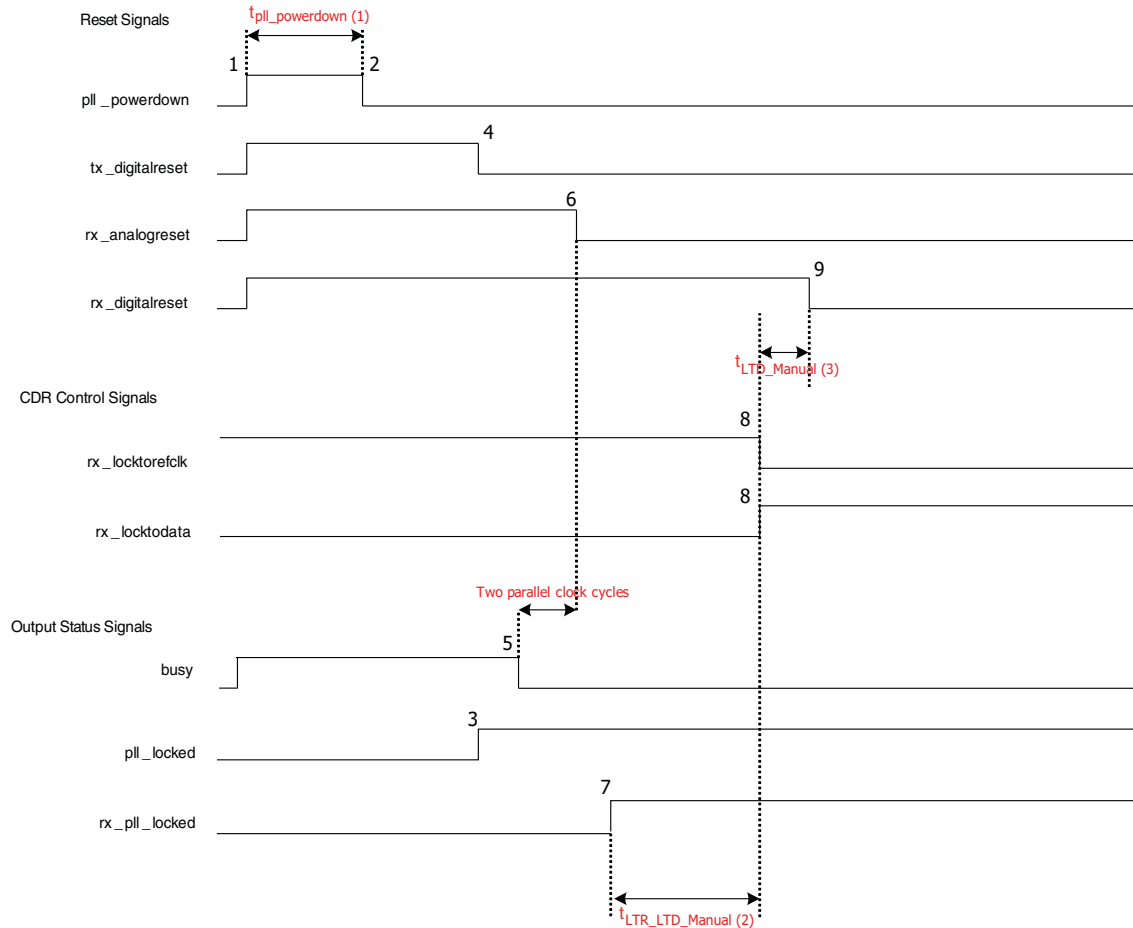
- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in [Figure 4-10](#), for the receiver in CDR automatic lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, and `rx_digitalreset` signals asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), de-assert `tx_digitalreset`. For receiver operation, wait for the `busy` signal to be de-asserted, after which `rx_analogreset` is de-asserted. After you de-assert `rx_analogreset`, the receiver CDR starts locking to the receiver input reference clock.
4. Wait for the `rx_freqlocked` signal to go high (marker 7).
5. After the `rx_freqlocked` signal goes high, wait for at least t_{LTD_Auto} , then de-assert the `rx_digitalreset` signal (marker 8). Note that `rx_digitalreset` must not be released if there is no data present at the receiver pins to avoid overflow/underflow of the phase compensation FIFOs. At this point, the transmitter and receiver are ready for data traffic.

Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. If you create a **Receiver and Transmitter** instance in the ALTGX MegaWizard Plug-In Manager with the receiver CDR in manual lock mode, use the reset sequence shown in [Figure 4-11](#).

Figure 4-11. Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode**Notes to Figure 4-11:**

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For $t_{LTR_LTD_Manual}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (3) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in [Figure 4-11](#), perform the following reset procedure for the receiver in manual lock mode:

1. After power up, assert `p11_powerdown` for a minimum period of $t_{p11_powerdown}$ (the time between markers 1 and 2).
2. Keep the `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, and `rx_locktorefclk` signals asserted and the `rx_locktodata` signal de-asserted during this time period. After you de-assert the `p11_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. After the transmitter PLL locks, as indicated by the `p11_locked` signal going high (marker 3), de-assert `tx_digitalreset`. For receiver operation, wait for the `busy` signal to be de-asserted. At this point `rx_analogreset` is de-asserted. When `rx_analogreset` is de-asserted, the receiver CDR starts locking to the receiver input reference clock because `rx_locktorefclk` is asserted.
4. Wait for at least $t_{LTR_LTD_Manual}$ (the time between markers 7 and 8) after the `rx_p11_locked` signal goes high, then de-assert the `rx_locktorefclk` signal. At the same time, assert the `rx_locktodata` signal (marker 8). At this point, the receiver CDR enters lock-to-data mode and the receiver CDR starts locking to the received data.
5. De-assert `rx_digitalreset` at least t_{LTD_Manual} (the time between markers 8 and 9) after asserting the `rx_locktodata` signal.

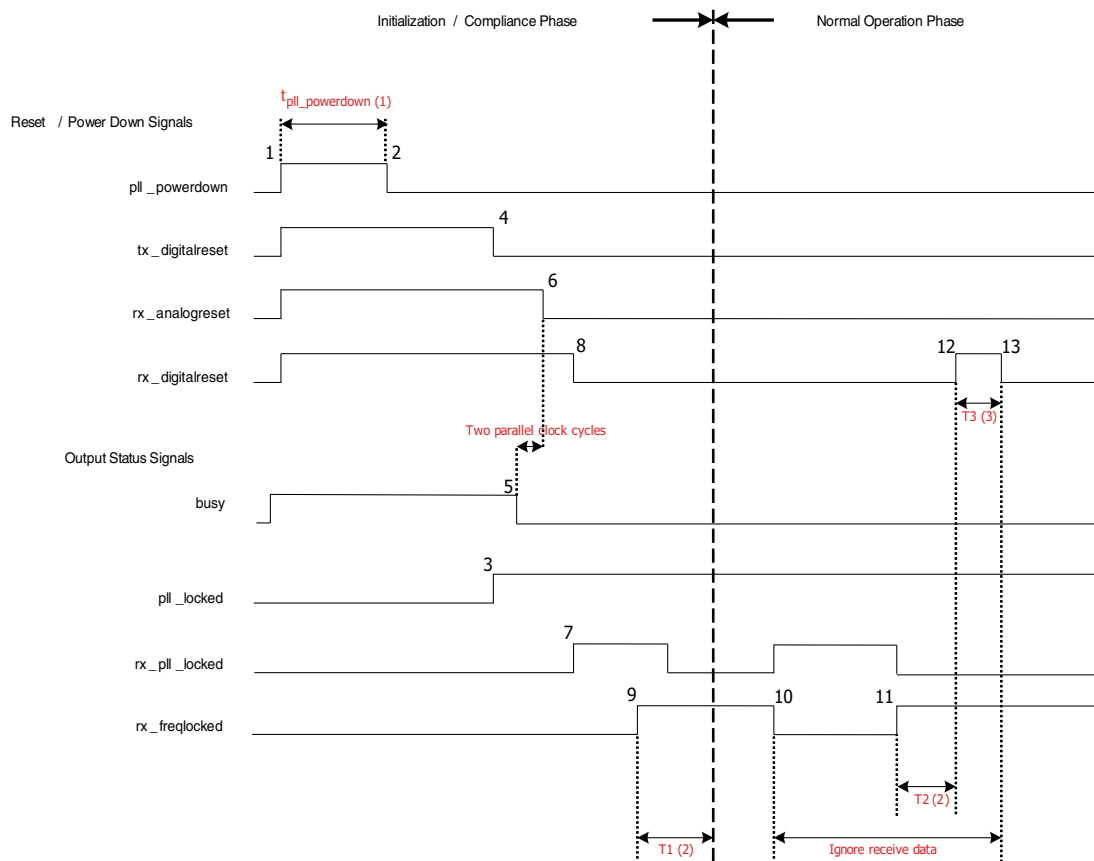
PCIe Functional Mode

You can configure PCIe functional mode with or without the receiver clock rate compensation FIFO in the Stratix IV device. The reset sequence remains the same whether or not you use the receiver clock rate compensation FIFO.

PCIe Reset Sequence

The PCIe protocol consists of an initialization/compliance phase and a normal operation phase. The reset sequences for these two phases are described based on the timing diagram in Figure 4-12.

Figure 4-12. Reset Sequence of PCIe Functional Mode



Notes to Figure 4-12:

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) The minimum T1 and T2 period is 4 μ s.
- (3) The minimum T3 period is two parallel clock cycles.

PCIe Initialization/Compliance Phase

After the device is powered up, a PCIe-compliant device goes through the compliance phase during initialization. In this phase, the PCIe protocol requires the system to be operating at the Gen 1 data rate. The `rx_digitalreset` signal must be de-asserted during this compliance phase to achieve transitions on the `pipephydonestatus` signal, as expected by the link layer. The `rx_digitalreset` signal is de-asserted based on the assertion of the `rx_freqlocked` signal.

During the initialization/compliance phase, do not use the `rx_freqlocked` signal to trigger a de-assertion of the `rx_digitalreset` signal. Instead, follow these reset steps:


1. After power up, assert `p11_powerdown` for a minimum period of $t_{p11_powerdown}$ (the time between markers 1 and 2). Keep the `tx_digitalreset`, `rx_analogreset`, and `rx_digitalreset` signals asserted during this time period. After you de-assert the `p11_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
2. When the transmitter PLL locks, as indicated by the `p11_locked` signal going high (marker 3), de-assert `tx_digitalreset`. For a receiver operation, wait for the busy signal to be de-asserted. `rx_analogreset` is then de-asserted. After `rx_analogreset` is de-asserted, the receiver CDR starts locking to the receiver input reference clock.
3. When the receiver CDR locks to the input reference clock, as indicated by the `rx_p11_locked` signal going high at marker 7 in [Figure 4-12](#), de-assert the `rx_digitalreset` signal (marker 8). After de-asserting `rx_digitalreset`, the `pipephydonestatus` signal transitions from the transceiver channel to indicate the status to the link layer. Depending on its status, `pipephydonestatus` helps with the continuation of the compliance phase. After successful completion of this phase, the device enters into the normal operation phase.

PCIe Normal Phase

For the normal PCIe phase, follow these steps:

1. After completion of the Initialization/Compliance phase, during the normal operation phase at the Gen 1 data rate, when the `rx_freqlocked` signal is de-asserted (marker 10 in [Figure 4-12](#)), wait for the `rx_p11_locked` signal assertion signifying the lock-to-reference clock.
2. Wait for the `rx_freqlocked` signal to go high again. In this phase, the received data is valid (not electrical idle) and the receiver CDR locks to the incoming data. Proceed with the reset sequence after assertion of the `rx_freqlocked` signal.
3. After the `rx_freqlocked` signal goes high, wait for at least 4 μ s before asserting `rx_digitalreset` (marker 12 in [Figure 4-12](#)) for two parallel receive clock cycles so that the receiver phase compensation FIFO is initialized.
4. During normal operation, after you speed-negotiate to the Gen 2 data rate, asserting the `rx_digitalreset` signal causes the PCIe rate switch circuitry to switch the transceiver to the Gen 1 data rate.

Data from the transceiver block is not valid from the time the `rx_freqlocked` signal goes low (marker 10 in [Figure 4-12](#)) to the time `rx_digitalreset` is de-asserted (marker 13 in [Figure 4-12](#)). The PLD logic ignores the data during this period (between markers 10 and 13 in [Figure 4-12](#)).

 You can configure the Stratix IV device in $\times 1$, $\times 4$, and $\times 8$ PCIe configurations. The reset sequence described in “PCIe Reset Sequence” on page 4-22 applies to all these multi-lane configurations.

PMA Direct Drive Mode Reset Sequences

Stratix IV devices provide a PMA Direct mode in which all PCS blocks, including the phase compensation FIFOs, are bypassed in both the transmitter and receiver channel data paths. In this mode, the PMA block in the transmitter and receiver channels directly interface with the FPGA fabric.

In PMA Direct drive mode, you can configure the transceiver channels as a single channel or in bonded configurations. Basic single- and double-width functional modes support bonding of PMA functional blocks across all transceiver channels on the same side of the device.


 The `tx_digitalreset` and `rx_digitalreset` signals are not available because there are no PCS blocks available in this mode.

Table 4-7 lists the reset and power-down sequences for PMA Direct drive $\times N$ functional mode.

Table 4-7. Reset and Power-Down Sequences for PMA Direct Drive $\times N$ Configurations

Channel Set Up	Functional Mode	Refer to
Transmitter Only with no PLL_L/R	Basic (PMA Direct) drive $\times 4$	“Transmitter Only Channel with No PLL_L/R” on page 4-25
Transmitter Only with a PLL_L/R	Manual lock mode	“Transmitter Only Channel with a PLL_L/R” on page 4-26
Receiver and Transmitter	Automatic lock mode for Basic (PMA Direct) drive $\times N$ mode	“Receiver and Transmitter Channel Set-up—Receiver CDR in Automatic Lock Mode” on page 4-28
Receiver and Transmitter	Manual lock mode for Basic (PMA Direct) drive $\times N$ mode	“Receiver and Transmitter Channel Set-up—Receiver CDR in Manual Lock Mode” on page 4-30

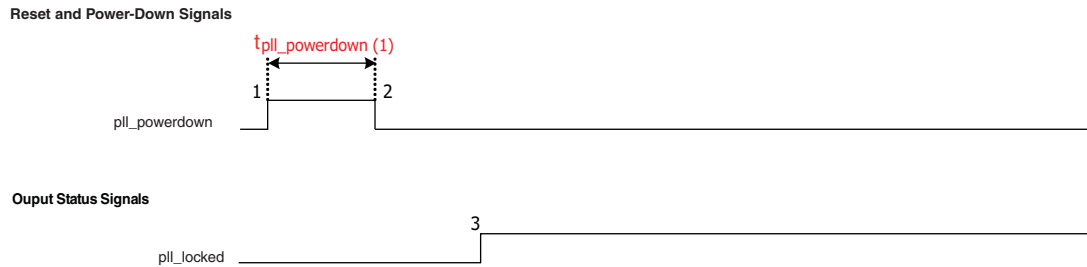
Basic (PMA Direct) Drive $\times N$ Mode

When bonding $\times N$ channels in a Basic (PMA Direct) drive mode configuration, you can reset all bonded channels simultaneously.

Transmitter Only Channel with No PLL_L/R

Figure 4-13 shows an example reset sequence timing diagram of four **Transmitter Only** channels in Basic (PMA Direct) drive $\times 4$ functional mode with no PLL_L/R.

Figure 4-13. Reset Sequence Timing in Basic (PMA Direct) Drive $\times 4$ Mode



Note to Figure 4-13:

(1) For $t_{p11_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

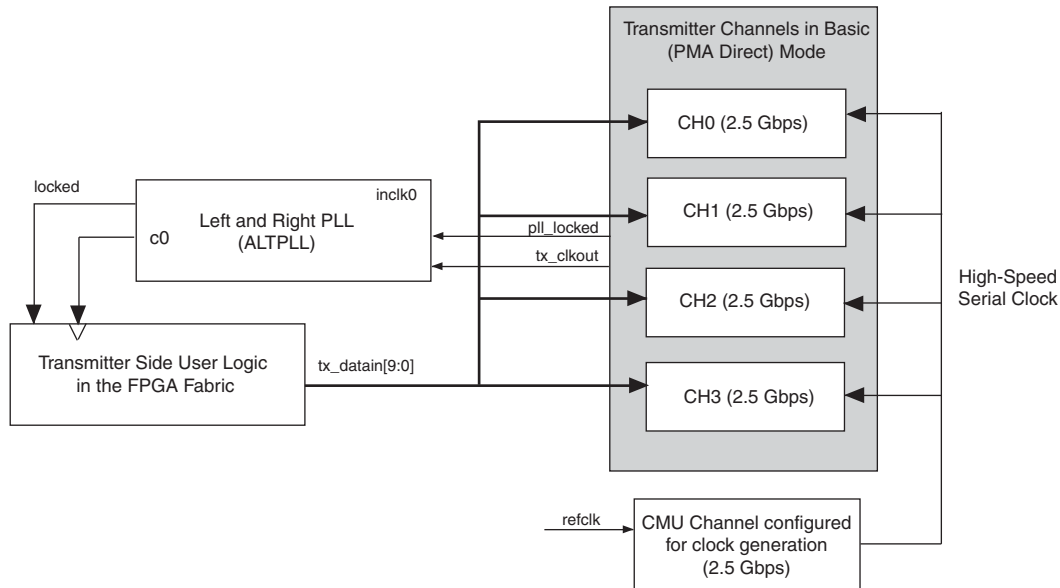
As shown in Figure 4-13, for the **Transmitter Only** channel in Basic (PMA Direct) drive functional $\times 4$ mode with no PLL_L/R, follow these reset steps:

1. After power up, assert `p11_powerdown` for a minimum of $t_{p11_powerdown}$ (the time between markers 1 and 2).
2. When the transmitter PLL locks, as indicated by the `p11_locked` signal going high (marker 3), the transmitter is ready to accept parallel data from the FPGA fabric and subsequently transmitting serial data reliably.

Transmitter Only Channel with a PLL_L/R

The Basic (PMA Direct) mode configuration that requires a PLL_L/R is one where each channel in PMA-Direct mode is identical. Figure 4-14 shows a simple set up of identical channels.

Figure 4-14. Identical Channels



Identical channels have the following same configuration:

- Same effective data rate
- Same transmitter local clock divider settings in each channel
- Same FPGA fabric-to-transceiver interface data path width
- The transmitter channels must receive the high-speed clock from the same PLL (either CMU PLL or ATX PLL).

Figure 4-15 shows an example reset sequence timing diagram of four **Transmitter Only** channels in Basic (PMA Direct) Drive x4 functional mode with a PLL_L/R.

As shown in Figure 4-15, for the **Transmitter Only** channel in Basic (PMA Direct) Drive functional mode with a PLL_L/R configuration, follow these reset steps:

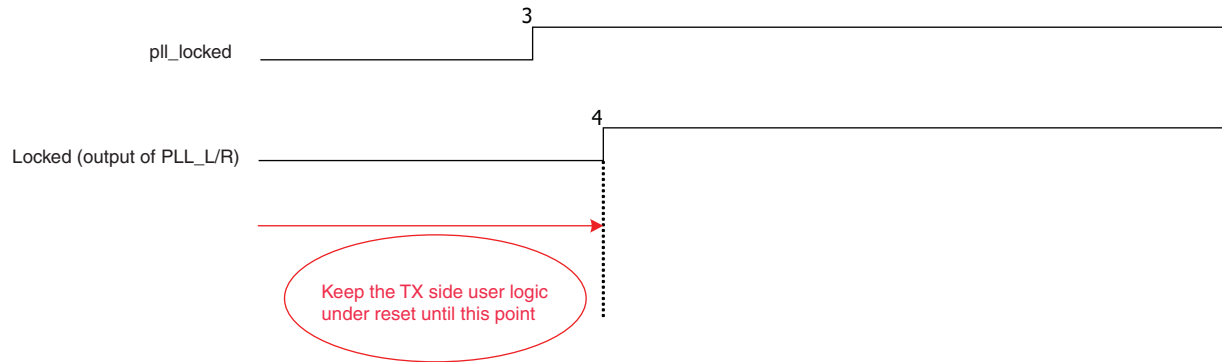
1. After power up, assert `p11_powerdown` for a minimum of $t_{p11_powerdown}$ (the time between markers 1 and 2).
2. After the transmitter PLL locks, as indicated by the `p11_locked` signal going high (marker 3), wait for the locked signal to be asserted. The locked signal is an output of the PLL_L/R.
3. After the PLL_L/R locks, as indicated by the `locked` signal going high (marker 4), the transmitter is ready to accept parallel data from the FPGA fabric and subsequently transmitting serial data reliably.

Figure 4-15. Reset Sequence Timing Diagram of Four Transmitter-Only Channels in Basic (PMA Direct) Drive x4 Functional Mode

Reset and Power-Down Signals



Output Status Signals

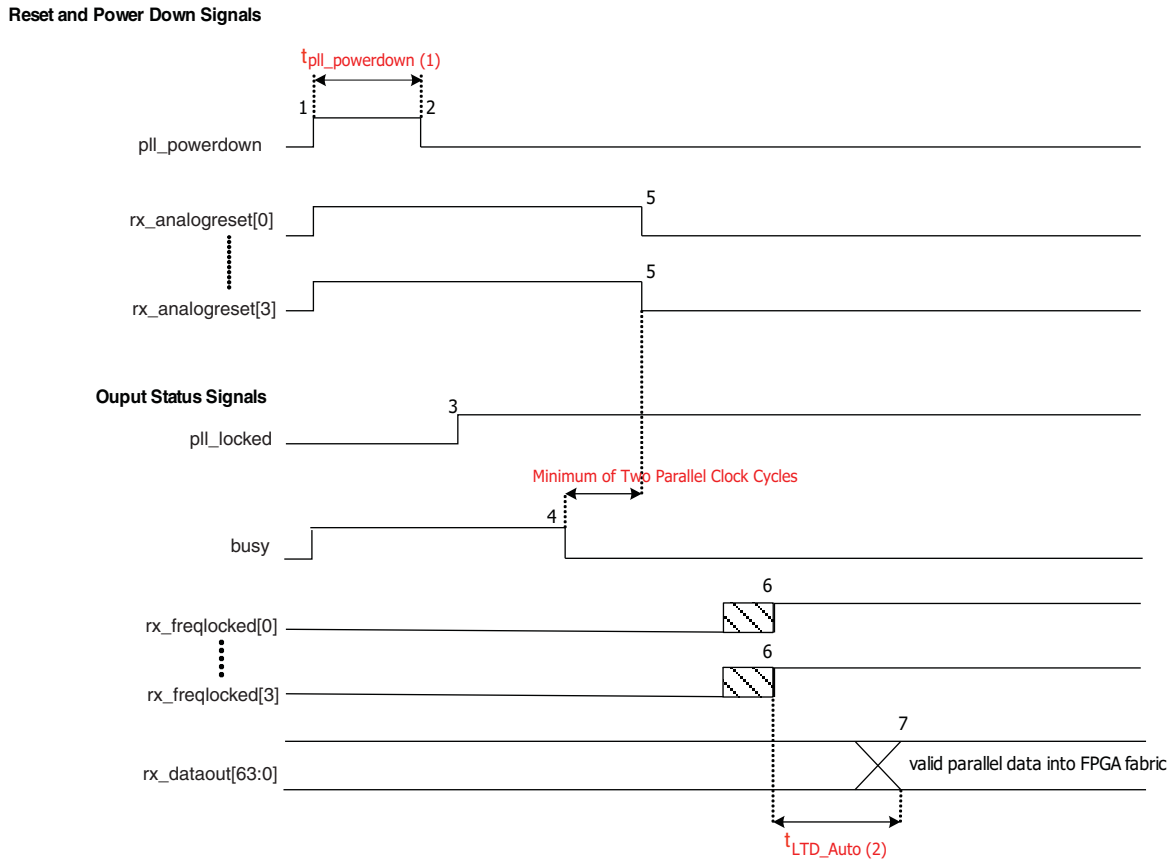


Note to Figure 4-15:

(1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Receiver and Transmitter Channel Set-up—Receiver CDR in Automatic Lock Mode

This configuration contains both a transmitter and receiver channel. For PMA Direct drive $\times N$ mode, with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 4-16. In this example, $N = 4$.

Figure 4-16. Reset Sequence with CDR in Automatic Lock Mode**Notes to Figure 4-16:**

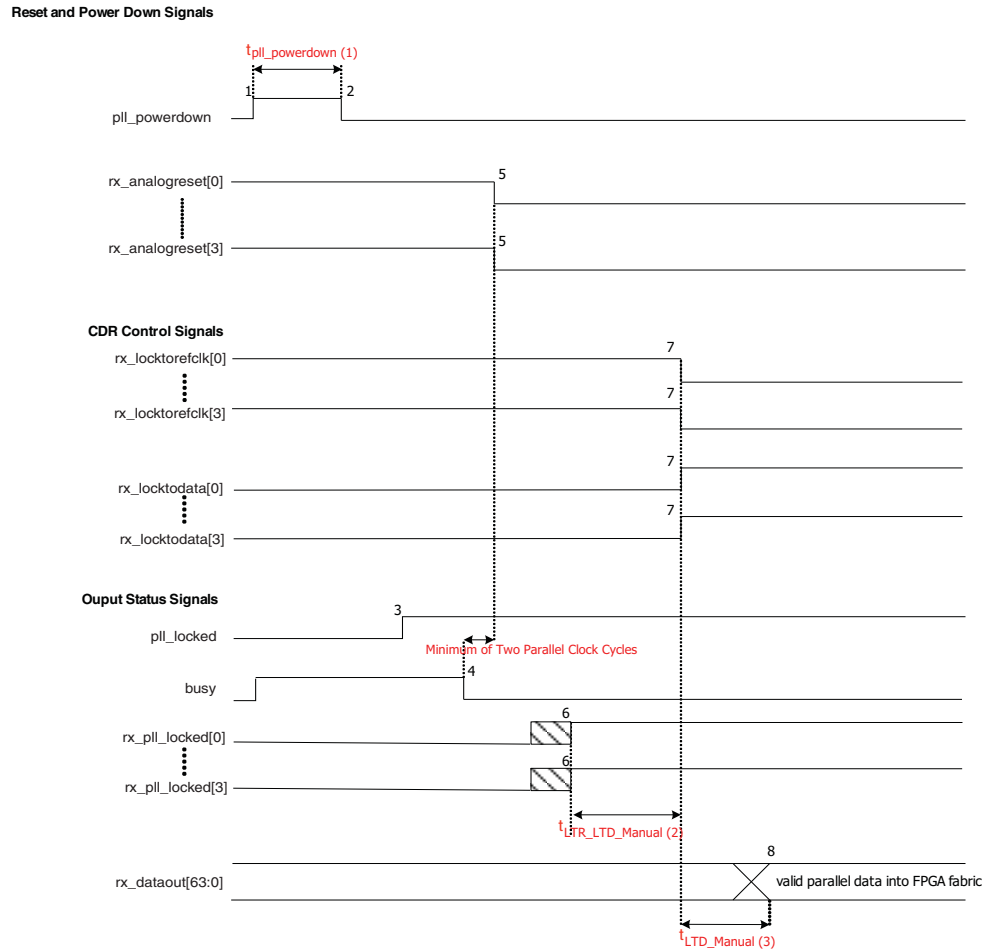
- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-16, for the receiver and transmitter channel in PMA Direct drive $\times 4$ double-width configuration with CDR in automatic lock mode, follow these reset steps:

1. After power up, assert `p11_powerdown` for a minimum period of $t_{p11_powerdown}$ (the time between markers 1 and 2).
2. Keep the `rx_analogreset` signal asserted during this time period. After you de-assert the `p11_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. When the transmitter PLL locks, as indicated by the `p11_locked` signal going high (marker 3), the transmitter is ready to accept parallel data from the FPGA fabric and transmitting serial data reliably.
4. For the receiver operation, after de-assertion of the busy signal, wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signals of each channel. After `rx_analogreset` is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock.
5. Wait for the `rx_freqlocked` signal from each channel to go high. The `rx_freqlocked` signal of each channel may go high at different times (as indicated by the slashed pattern at marker 6).
6. In a PMA Direct drive $\times 4$ double-width configuration, when the `rx_freqlocked` signals of all the channels has gone high (marker 6), from that point onwards, wait for at least t_{LTD_Auto} (marker 7) for the receiver parallel clock to become stable. At this point, all the receivers are ready for transferring valid parallel data into the FPGA fabric (until this time, Altera recommends that the user logic that processes this data be under reset).

Receiver and Transmitter Channel Set-up—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. For PMA Direct drive $\times N$ mode, with receiver CDR in manual lock mode, use the reset sequence shown in Figure 4-17. In this example, $N = 4$.

Figure 4-17. Reset Sequence with CDR in Manual Lock Mode**Notes to Figure 4-17:**

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (3) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-17, for the receiver and transmitter channel in PMA Direct drive ×4 double-width configuration with CDR in manual lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `rx_analogreset` and `rx_locktorefclk` signals asserted and the `rx_locktodata` signal de-asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. When the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), the transmitter is ready to accept parallel data from the FPGA fabric and transmitting serial data reliably.
4. For the receiver operation, after de-assertion of the busy signal (marker 4), wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signal. After the `rx_analogreset` signal is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock because `rx_locktorefclk` is asserted.
5. Wait for the `rx_pll_locked` signal from each channel to go high. The `rx_pll_locked` signal of each channel may go high at different times with respect to each other (indicated by the slashed pattern at marker 6).
6. In a PMA Direct drive ×4 double-width configuration, when the `rx_pll_locked` signal of all the channels has gone high, from that point onwards, wait for at least t_{LTD_Manual} , then de-assert `rx_locktorefclk` and assert `rx_locktodata` (marker 7). At this point, the receiver CDR of all the channels enters into lock-to-data mode and starts locking to the received data.
7. After assertion of the `rx_locktodata` signal, from that point onwards, wait for at least t_{LTD_Manual} (marker 8) for the receiver parallel clock to become stable. At this point, all the receivers are ready for transferring valid parallel data into the FPGA fabric (until this time, Altera recommends that the user logic that processes this data be under reset).

Basic (PMA Direct) Drive x1 Mode

The following timing diagram examples are used to describe the reset and power down sequences for Basic (PMA Direct) drive mode without bonding between the transceiver channels.

Table 4-8 lists the reset and power-down sequences for Basic (PMA Direct) drive ×1 functional mode.

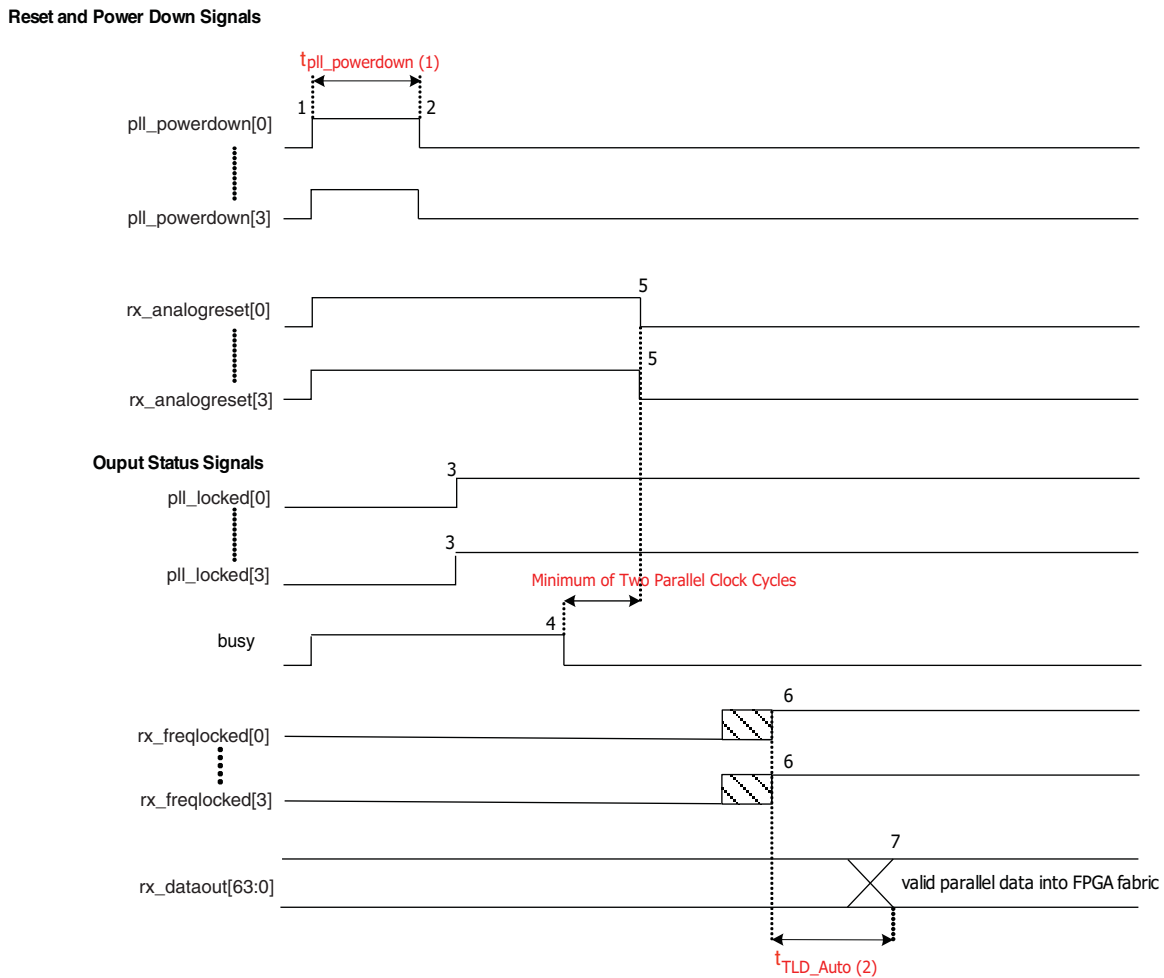
Table 4-8. Reset and Power-Down Sequences for Basic (PMA Direct) Drive ×1 Configurations

Channel Set Up	Functional Mode	Refer to
Receiver and Transmitter	Automatic lock mode for Basic (PMA Direct) drive ×1 mode	“Receiver and Transmitter Channel Set-Up—Receiver CDR in Automatic Lock Mode” on page 4-32
Receiver and Transmitter	Manual lock mode for Basic (PMA Direct) drive ×1 mode	“Receiver and Transmitter Channel Set-up—Receiver CDR in Manual Lock Mode” on page 4-34

Receiver and Transmitter Channel Set-Up—Receiver CDR in Automatic Lock Mode

This configuration contains both a transmitter and receiver channel. For Basic (PMA Direct) drive $\times 1$ mode, with receiver CDR in automatic lock mode, use the reset sequence shown in Figure 4-18. In this example, four channels are configured in this mode.

Figure 4-18. Reset Sequence with CDR in Automatic Lock Mode



Notes to Figure 4-18:

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{TLD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

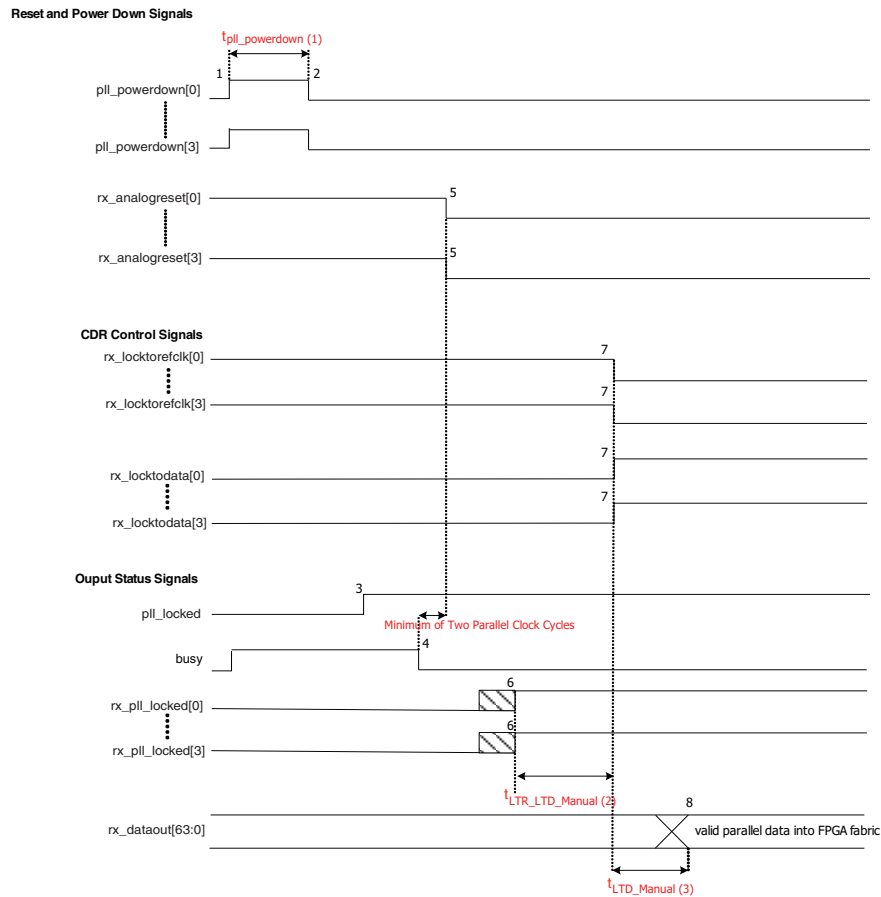
As shown in Figure 4-18, for the receiver and transmitter channel in Basic (PMA Direct) drive double-width configuration, non-bonded with CDR in automatic lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` of each channel for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `rx_analogreset` signal of each channel asserted during this time period. After you de-assert the `pll_powerdown` signal on all channels, the transmitter PLL of each channel starts locking to the transmitter input reference clock.
3. When the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), the transmitters are ready for accepting parallel data from the FPGA fabric and subsequently transmitting serial data reliably.
4. For the receiver operation, after de-assertion of the busy signal, wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signals of each channel. After `rx_analogreset` is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock.
5. Wait for the `rx_freqlocked` signal from each channel to go high. The `rx_freqlocked` signal of each channel may go high at different times (indicated by the slashed pattern at marker 6).
6. In a Basic (PMA Direct) drive double-width configuration without bonding between channels, when the `rx_freqlocked` signals of all the channels have gone high (marker 6), from that point onwards, wait for at least t_{LTD_Auto} (marker 7) for the receiver parallel clock to become stable. At this point, all the receivers are ready for transferring valid parallel data into the FPGA fabric (until this time, Altera recommends that the user logic that processes this data be under reset).

Receiver and Transmitter Channel Set-up—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. For Basic (PMA Direct) drive $\times 1$ mode, with receiver CDR in manual lock mode, use the reset sequence shown in Figure 4-19. In this example, four channels are configured in this mode.

Figure 4-19. Reset Sequence with CDR in Manual Lock Mode



Notes to Figure 4-19

- (1) For $t_{pll_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For $t_{LTR_LTD_Manual}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (3) For t_{LTD_Manual} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4-19, for the receiver and transmitter channel in Basic (PMA Direct) drive double-width configuration, non-bonded with CDR in manual lock mode, follow these reset steps:

1. After power up, assert `pll_powerdown` of each channel for a minimum period of $t_{pll_powerdown}$ (the time between markers 1 and 2).
2. Keep the `rx_analogreset` and `rx_locktorefclk` signals of each channel asserted and the `rx_locktodata` signals de-asserted during this time period. After you de-assert the `pll_powerdown` signal, the transmitter PLL starts locking to the transmitter input reference clock.
3. When the transmitter PLL locks, as indicated by the `pll_locked` signal going high (marker 3), the transmitters are ready to accept parallel data from the FPGA fabric and subsequently transmitting serial data reliably.
4. For the receiver operation, after de-assertion of the busy signal (marker 4), wait for a minimum of two parallel clock cycles to de-assert the `rx_analogreset` signal of each channel. After the `rx_analogreset` signal is de-asserted, the receiver CDR of each channel starts locking to the receiver input reference clock because `rx_locktorefclk` is asserted.
5. Wait for the `rx_pll_locked` signal from each channel to go high. The `rx_pll_locked` signal of each channel may go high at different times with respect to each other (indicated by the slashed pattern at marker 6).
6. In a Basic (PMA Direct) drive double-width configuration without bonding between channels, when the `rx_pll_locked` signal of all the channels has gone high, from that point onwards, wait for at least $t_{LTR_LTD_Manual}$, then de-assert `rx_locktorefclk` and assert `rx_locktodata` (marker 7). At this point, the receiver CDR of all the channels enters into lock-to-data mode and starts locking to the received data.
7. After assertion of the `rx_locktodata` signal, from that point onwards, wait for at least t_{LTD_Manual} (marker 8) for the receiver parallel clock to be stable. At this point, all the receivers are ready for transferring valid parallel data into the FPGA fabric (until this time, Altera recommends that the user logic that processes this data be reset).

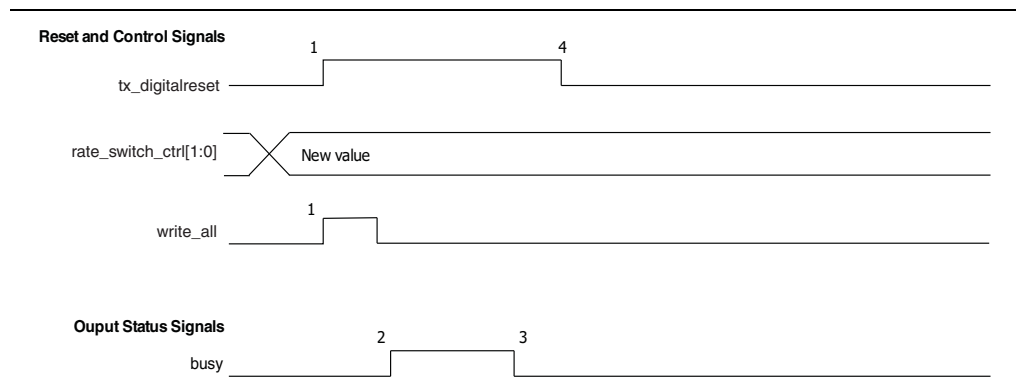
Dynamic Reconfiguration Reset Sequences

When using dynamic reconfiguration in data rate divisions in TX or channel and TX CMU PLL select/reconfig modes, use the following reset sequences.

Reset Sequence when Using Dynamic Reconfiguration with the ‘data rate division in TX’ Option


Use the example reset sequence shown in [Figure 4–20](#) when you use the dynamic reconfiguration controller to change the data rate of the transceiver channel. In this example, dynamic reconfiguration is used to dynamically reconfigure the data rate of the transceiver channel configured in Basic $\times 1$ mode with the receiver CDR in automatic lock mode.

Figure 4–20. Reset Sequence When Using the Dynamic Reconfiguration Controller to Change the Data Rate of the Transceiver Channel



As shown in [Figure 4–20](#), when using the dynamic reconfiguration controller to change the configuration of the transmitter channel, follow these reset steps:

1. After power up and properly establishing that the transmitter is operating as desired, write the desired new value for the data rate in the appropriate register (in this example, `rate_switch_ctrl[1:0]`) and subsequently assert the `write_all` signal (marker 1) to initiate the dynamic reconfiguration.

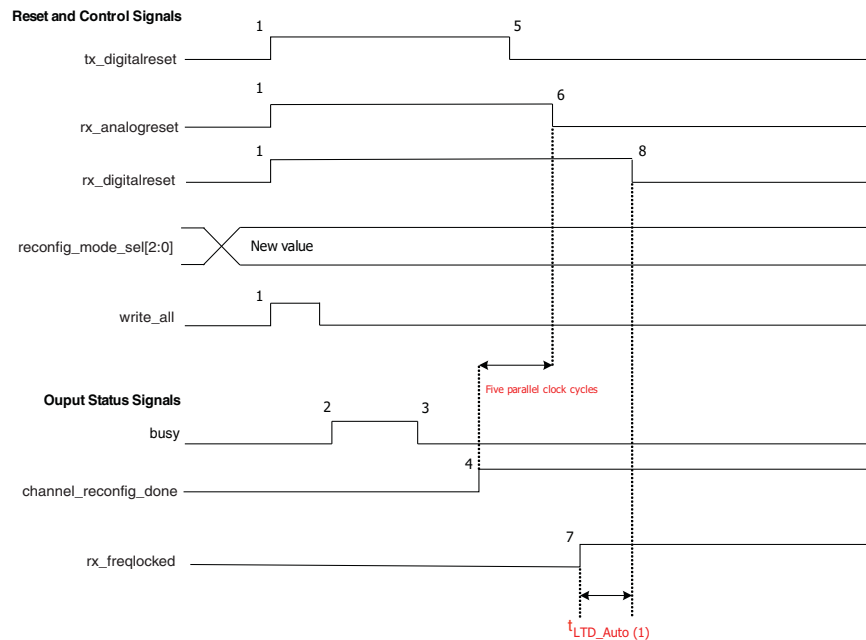
 For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

2. Assert the `tx_digitalreset` signal.
3. As soon as `write_all` is asserted, the dynamic reconfiguration controller starts to execute its operation. This is indicated by the assertion of the `busy` signal (marker 2).
4. After the completion of dynamic reconfiguration, the `busy` signal is de-asserted (marker 3).
5. Lastly, `tx_digitalreset` can be de-asserted to continue with the transmitter operation (marker 4).

Reset Sequence when Using Dynamic Reconfiguration with the ‘Channel and TX PLL select/reconfig’ Option

Use the example reset sequence shown in Figure 4–21 when you are using the dynamic reconfiguration controller to change the TX PLL settings of the transceiver channel. In this example, the dynamic reconfiguration is used to dynamically reconfigure the data rate of the transceiver channel configured in Basic ×1 mode with receiver CDR in automatic lock mode.

Figure 4–21. Reset Sequence When Using the Dynamic Reconfiguration Controller to Change the TX PLL Settings of the Transceiver Channel




Note to Figure 4–21:

(1) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

As shown in Figure 4–21, when using the dynamic reconfiguration controller to change the configuration of the transceiver channel, follow these reset steps:

1. After power up and establishing that the transceiver is operating as desired, write the desired new value in the appropriate registers (including `reconfig_mode_sel[2:0]`) and subsequently assert the `write_all` signal (marker 1) to initiate the dynamic reconfiguration.

 For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

2. Assert the `tx_digitalreset`, `rx_analogreset`, and `rx_digitalreset` signals.
3. As soon as `write_all` is asserted, the dynamic reconfiguration controller starts to execute its operation. This is indicated by the assertion of the `busy` signal (marker 2).
4. Wait for the assertion of the `channel_reconfig_done` signal (marker 4) that indicates the completion of dynamic reconfiguration in this mode.

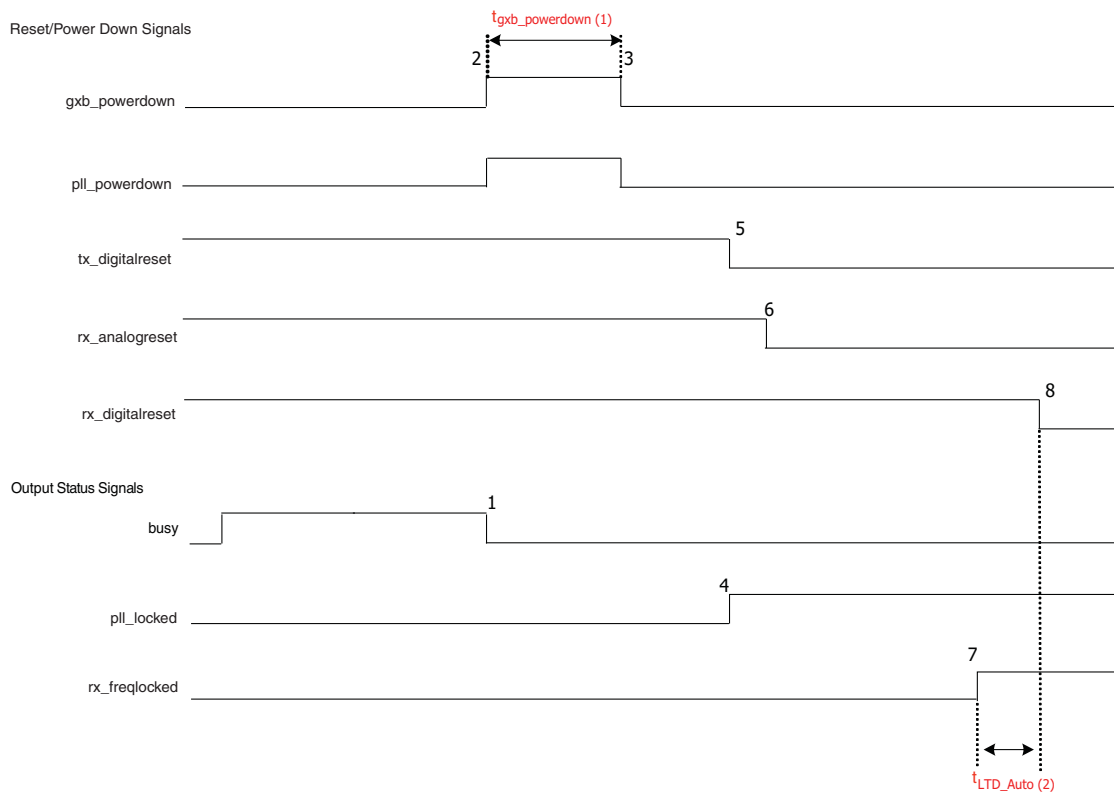
5. After assertion of the channel_reconfig_done signal, de-assert tx_digitalreset (marker 5) and wait for at least five parallel clock cycles to de-assert the rx_analogreset signal (marker 6).
6. Lastly, wait for the rx_freqlocked signal to go high. After rx_freqlocked goes high (marker 7), wait for t_{LTD_Auto} to de-assert the rx_digitalreset signal (marker 8). At this point, the receiver is ready for data traffic.

Power Down

The Quartus II software automatically selects the power-down channel feature, which takes effect when you configure the Stratix IV device. All unused transceiver channels and blocks are powered down to reduce overall power consumption. The gxb_powerdown signal is an optional transceiver block signal. It powers down all transceiver channels and all functional blocks in the transceiver block. The minimum pulse width for this signal is 1 μ s. After power up, if you use the gxb_powerdown signal, wait for de-assertion of the busy signal, then assert the gxb_powerdown signal for a minimum of 1 μ s. Lastly, follow the sequence shown in Figure 4-22.

The de-assertion of the busy signal indicates proper completion of the offset cancellation process on the receiver channel.

Figure 4-22. Sample Reset Sequence of Four Receiver and Transmitter Channels-Receiver CDR in Automatic Lock Mode with the Optional gxb_powerdown Signal



Notes to Figure 4-22:

- (1) For $t_{gxb_powerdown}$ duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- (2) For t_{LTD_Auto} duration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Simulation Requirements

The following are simulation requirements:

- The `gxb_powerdown` port is optional. In simulation, if the `gxb_powerdown` port is not instantiated, you must assert the `tx_digitalreset`, `rx_digitalreset`, and `rx_analogreset` signals appropriately for correct simulation behavior.
- If the `gxb_powerdown` port is instantiated, and the other reset signals are not used, you must assert the `gxb_powerdown` signal for at least one parallel clock cycle for correct simulation behavior.
- You can de-assert the `rx_digitalreset` signal immediately after the `rx_freqlocked` signal goes high to reduce the simulation run time. It is not necessary to wait for `tLTD_Auto` (as suggested in the actual reset sequence).
- The `busy` signal is de-asserted after about 20 parallel `reconfig_clk` clock cycles in order to reduce simulation run time. For silicon behavior in hardware, you can follow the reset sequences described in the previous pages.
- In PCIe mode simulation, you must assert the `tx_forceecleidle` signal for at least one parallel clock cycle before transmitting normal data for correct simulation behavior.

Reference Information

For more information about some useful reference terms used in this chapter, refer to the links listed in [Table 4-9](#).

Table 4-9. Reference Information (Part 1 of 2)

Terms Used in this Chapter	Useful Reference Points
Automatic Lock Mode	page 4-8
Basic (PMA Direct) Drive x1 Mode	page 4-31
Basic (PMA Direct) Drive xN Mode	page 4-25
Bonded channel configuration	page 4-6
<code>busy</code>	page 4-3
Dynamic Reconfiguration Reset Sequences	page 4-36
<code>gxb_powerdown</code>	page 4-3
LTD	page 4-6
LTR	page 4-6
Manual Lock Mode	page 4-10
Non-Bonded channel configuration	page 4-15
PCIe	page 4-22
<code>pll_locked</code>	page 4-3
<code>pll_powerdown</code>	page 4-3
<code>rx_analogreset</code>	page 4-2
<code>rx_digitalreset</code>	page 4-2
<code>rx_freqlocked</code>	page 4-3

Table 4-9. Reference Information (Part 2 of 2)

Terms Used in this Chapter	Useful Reference Points
rx_pll_locked	page 4-3
tx_digitalreset	page 4-2

Document Revision History

Table 4-10 lists the revision history for this chapter.

Table 4-10. Document Revision History

Date	Version	Changes
December 2011	4.2	Updated Table 4-2.
February 2010	4.1	<ul style="list-style-type: none"> ■ Updated the “Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Automatic Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”, “Receiver and Transmitter Channel Set-up—Receiver CDR in Automatic Lock Mode”, “Receiver and Transmitter Channel Set-up—Receiver CDR in Manual Lock Mode” ■ Updated Figure 4-4, Figure 4-5, Figure 4-6, Figure 4-7, Figure 4-16, Figure 4-17, Figure 4-18, and Figure 4-19. ■ Updated Table 4-2. ■ Updated chapter title. ■ Applied new template. ■ Minor text edits.
November 2009	4.0	<ul style="list-style-type: none"> ■ Updated all figures (except Figure 1, Figure 2, and Figure 14) and all sections so they use the same terms that are found in the <i>DC and Switching Characteristics</i> chapter in the <i>Stratix IV Device Datasheet</i> section. ■ Added Table 4-1, Table 4-2, Table 4-5, Table 4-6, Table 4-7, and Table 4-8. ■ Added the “Reference Information” section. ■ Updated all figures (except Figure 1). ■ Changed “PLL_powerdown” to “pll_powerdown” throughout. ■ Minor text edits.
June 2009	3.1	<ul style="list-style-type: none"> ■ Added new “Transmitter Only Channel with a PLL_L/R” section. ■ Updated the “Transmitter Only Channel with no PLL_L/R” and “Transmitter Only Channel” sections. ■ Minor text edits.
March 2009	3.0	<p>Added:</p> <ul style="list-style-type: none"> ■ “PMA Direct Drive Mode Reset Sequences” ■ “Dynamic Reconfiguration Reset Sequences”
November 2008	2.0	Added chapter to the <i>Stratix IV Device Handbook</i> .