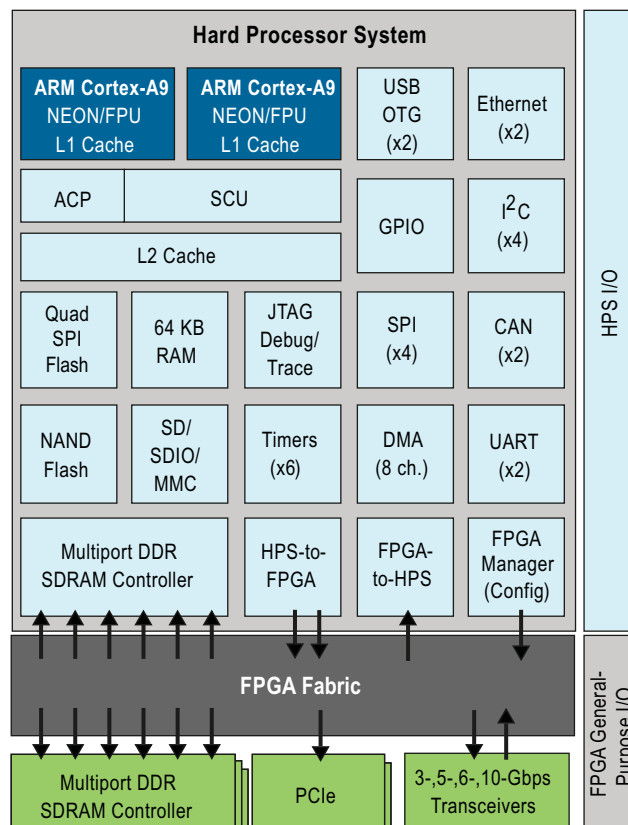


Altera's 28-nm Cyclone® V and Arria® V system on a chip (SoC) FPGAs feature a hard processor system (HPS)—containing a microprocessor unit (MPU) with a dual-core ARM® Cortex™-A9 MPCore™ processor, a rich set of peripherals, a multi-port memory controller, and FPGA fabric, as shown in [Figure 1](#).

The tight integration between the HPS and FPGA fabric supports over 100-Gbps peak bandwidth with integrated data coherency between the processors, peripherals, and the FPGA. The included set of hardened embedded peripherals eliminates the need to implement these functions in programmable logic, leaving more FPGA resources for application-specific custom logic. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP.

**Figure 1. Hard Processor System**



The combination of embedded processor and programmable logic provides the following advantages:

- Reduces board space, system power, and material cost by eliminating the need for a discrete embedded processor
- Differentiates the end product in both hardware and software
- Adds support for virtually any interface standard in programmable logic
- Extends product life and revenue through in-field hardware and software updates

The dual-core ARM Cortex-A9 MPCore processor features a high-efficiency superscalar pipeline that delivers 2.5 DMIPS/MHz peak performance per each CPU. Each processor core includes a single instruction, multiple data (SIMD) NEON™ media processing engine, and a single- or double-precision floating-point unit to accelerate image processing, graphics, and scientific computational performance. Performance and power optimized level 1 (L1) caches combine minimal access latency techniques to maximize performance and minimize power consumption. The snoop control unit (SCU) provides cache coherence for enhanced inter-processor communication or support of rich Symmetric multiprocessing (SMP)-capable operating systems for simplified multicore software development.

You can power the HPS and FPGA independently, and configure the FPGA and boot the HPS in any order. In addition to traditional configuration methods, such as JTAG, the FPGA can be configured using any of the following memories or methods:

- Serial flash
- Parallel flash
- PCI Express® (PCIe®)
- HPS, under software control

You can also use the HPS to configure other FPGA devices in the system. The processor system can boot from dedicated HPS interfaces, such as quad Serial Peripheral Interface (SPI) flash memory, or from user-defined interfaces in the FPGA logic.

The following list summarizes the features of the HPS of the SoC FPGA.

# Feature Summary

## Processor Architecture

- Dual-core ARM Cortex-A9 MPCore processor
  - Up to 800 MHz maximum frequency
  - Support for symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP)
- Each processor core includes:
  - 32 kilobytes (KB) of L1 instruction cache
  - 32 KB of L1 data cache
  - NEON media processing engine
  - Single- or double-precision floating-point unit
  - Memory management unit (MMU)
  - Private interval timer
  - Private watchdog timer
  - 512 KB of shared level 2 (L2) cache
- SCU for cache coherency
- Accelerator coherency port (ACP)
- Global timer
- Generic interrupt controller
- CoreSight™ instruction trace

## Memory Interface Support

- Multiport SDRAM controller subsystem
  - DDR2 and DDR3
  - LPDDR1 and LPDDR2
  - Error correction code (ECC)
- Flash memory controller
  - NAND with direct memory access (DMA) and optional ECC
  - Quad SPI (NOR)
  - Secure Digital (SD)/ secure digital I/O (SDIO)/ MultiMediaCard (MMC) with DMA

## Interface Peripherals

- Two 10/100/1000 megabits per second (Mbps) Ethernet media access controllers (EMACs) with DMA
- Two USB 2.0 On-The-Go (USB OTG) controllers with DMA
- Four I<sup>2</sup>C controllers
- Two controller area networks (CAN), two master SPIs, two slave SPIs, UART
- Up to 71 general-purpose I/Os (GPIOs) and 14 input-only

## System Peripherals

- Four general purpose timers
- Two watchdog timers
- 8-channel DMA controller
- FPGA manager for FPGA configuration
- Clock and reset managers

## On-Chip Memory

- 64 KB on-chip RAM
- 64 KB on-chip boot ROM

## HPS/FPGA Interfaces

- HPS-to-FPGA bridges
  - Processor and DMA access to FPGA peripherals
  - Configurable 32-, 64-, or 128-bit Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™)
- FPGA-to-HPS bridges
  - FPGA masters access processor subsystem peripherals
  - Configurable 32-, 64-, or 128-bit AMBA AXI interface
  - Coherent access to processor cache through ACP
  - FPGA-to-HPS SDRAM controller subsystem interface
  - FPGA access to DRAM for shared memory
  - Up to 6 masters, 4 x64-bit read, 4 x64-bit write data
- Miscellaneous
  - FPGA-to-HPS interrupts
  - DMA handshake (allows FPGA peripherals to perform block-level transfers with system DMA controller)
  - More than 100 Gbps HPS-to-FPGA and FPGA-to-HPS bandwidth

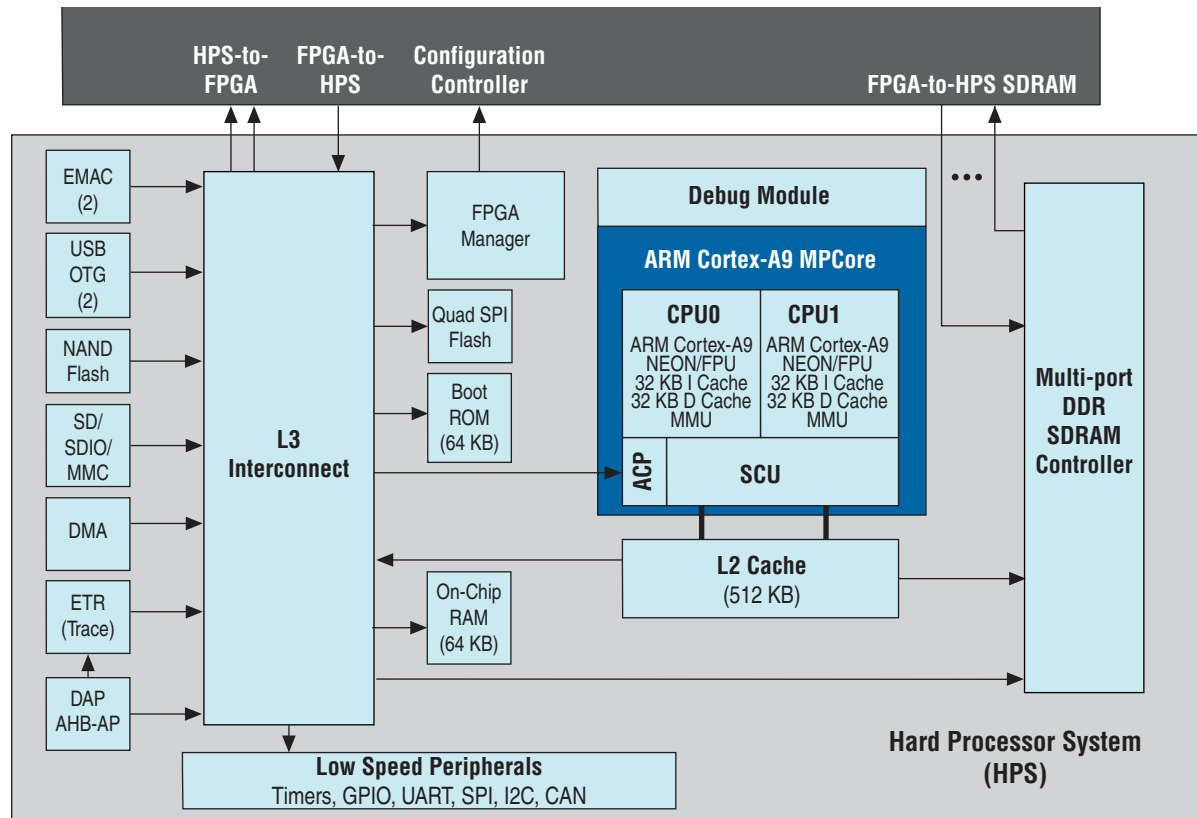
## Debug

- IEEE standard 1149.1-2001 (JTAG)
  - CPU Debug Access Port (DAP)
  - Direct memory debug via Advanced High-performance Bus Access Port (AHB-AP)
- Embedded trace router (ETR) port with DMA
  - Processor trace
  - System bus trace
  - Operating system (OS) trace
- On-chip trace storage

## ARM Cortex-A9 MPCore Processor

The HPS contains a dual-core ARM Cortex-A9 MPCore processor, an SCU that ensures processor cache coherency, and an ACP that accepts coherent memory access requests. Each Cortex-A9 central processing unit (CPU) contains a 32 KB L1 instruction cache and a 32 KB L1 data cache. The 512 KB L2 cache is shared between the two processors. The L2 cache has one AMBA AXI master port connected to the level 3 (L3) interconnect, and another AMBA AXI master port connected directly to the SDRAM controller, as shown in [Figure 2](#).

**Figure 2. ARM Cortex-A9 MPCore Processor**



### System Peripherals

The HPS includes the following peripherals:

- Two 10/100/1000 Mbps EMACs compliant with the IEEE standard 802.3-2005. Each EMAC is also compliant with the IEEE standard 1588-2002 and the IEEE standard 1588-2008 for precision networked clock synchronization. The controllers also support multiple TCP/IP offload functions. The EMACs have integrated DMA controllers.
- Two USB OTG controllers to support USB 2.0 host and device operation. The USB OTG controller has an integrated DMA controller.
- NAND controller to support Single-Level Cell (SLC) and Multi-Level Cell (MLC) devices, with optional ECC support. The controller has an integrated DMA controller.

- SD/SDIO/MMC peripheral with an integrated DMA controller.
- Quad SPI flash controller to support x1, x2, and x4 NOR flash devices.
- DMA controller to provide up to eight channels of high-bandwidth data transfer for modules without integrated DMA controllers.
- ARM CoreSight™ debug and trace modules to facilitate software development and debug, providing interfaces to industry standard debug probes. The Embedded Trace Router (ETR) and DAP each have an integrated DMA controller.
- A set of low-speed general purpose peripherals connected to the HPS via a 32-bit AMBA Advanced Peripheral Bus (APB™) interconnect. The following peripherals are included:
  - Interval timer
  - GPIO
  - UART
  - SPI
  - CAN
  - I<sup>2</sup>C
- System control peripherals connected to the ARM APB interconnect:
  - System manager—controls system configuration, status, and HPS I/O pin multiplexing.
  - Scan manager—drives serial scan-chains to FPGA JTAG and HPS I/O bank configuration.
  - Clock manager—manages clocks for the HPS. The clock managers contains three phase-locked loops (PLLs).
  - Reset manager—accepts reset requests from various sources in the HPS and FPGA and internally generates module reset signals.
- FPGA manager module to configure and monitor the FPGA fabric. This module interfaces with control block related signals in the FPGA fabric.
- 64 KB on-chip ROM containing the code required to support HPS boot from cold or warm reset.
- 64 KB on-chip RAM supporting a wide range of uses, including fast access to frequently used data, trace data storage, custom boot code.

## Interconnects with FPGA Fabric

SoC FPGAs provide performance that cannot be achieved by multiple-chip solutions based on an FPGA and a discrete processor. The high-throughput datapaths between the HPS and the FPGA fabric achieve superior performance and lower latency when compared to solutions containing a separate FPGA and discrete processor. The HPS provides the following interconnect features:

- FPGA-to-HPS bridges
  - Allows logic in the FPGA fabric to master peripherals and memories in the HPS
  - Maximum of 128-bit AMBA AXI interface in both read and write directions
  - 245 MHz typical in Arria V fabric, 200 MHz typical in Cyclone V fabric
  - Provides asynchronous clock crossing with the clock provided from FPGA logic
- HPS-to-FPGA bridges
  - Allows components in the HPS to master components in the FPGA fabric
  - Provides a maximum of 128-bit AMBA AXI interface in read and write directions
  - 245 MHz typical in Arria V fabric, 200 MHz typical in Cyclone V fabric
  - Provides asynchronous clock crossing with the clock provided by FPGA logic
  - Additional 32-bit HPS-to-FPGA bridge dedicated to peripheral control and status register (CSR) accesses
- FPGA-to-SDRAM interface
  - Allows components in the FPGA fabric to master the SDRAM controller in the HPS
  - Provides up to four bidirectional data ports (configurable: 1 x 256-bits, 2 x 128-bits, 4 x 64-bits)
  - Provides up to six command (read/write transaction) ports
  - Supports either AMBA AXI or Avalon Memory-Mapped (Avalon-MM configuration)
  - Separate 256-bit read and write data paths
  - 245 MHz typical in Arria V fabric, 200 MHz typical in Cyclone V fabric
  - Provides asynchronous clock crossing with the clock provided from FPGA logic
- MPU subsystem standby mode
  - Provides notification signals to the FPGA fabric that the MPU is in standby mode
  - Provides event signals to wake up the MPU subsystem from a wait for event (WFE) state
- FPGA clocks and resets—supply flexible clocking to and from the HPS

- HPS JTAG interface—optionally extends HPS JTAG into the FPGA fabric
- Trace Port Interface Unit (TPIU)—ARM CoreSight-compatible interface for on-chip trace
- FPGA System Trace Macrocell (STM) Events—interface that allows FPGA fabric to send hardware events using the ARM System Trace Macrocell
- FPGA Cross-Trigger Interface (CTI)—interface that allows triggers to and from the ARM CoreSight trigger system
- Peripheral interfaces—allows some of the HPS peripherals to use FPGA fabric and pins for customization and external communication
- Interrupts—supports interrupts directly to the MPU interrupt controller by soft IP
- FPGA manager interface—communication signals with FPGA fabric for boot and configuration and supplies information on FPGA configuration status

## SDRAM Controller Subsystem

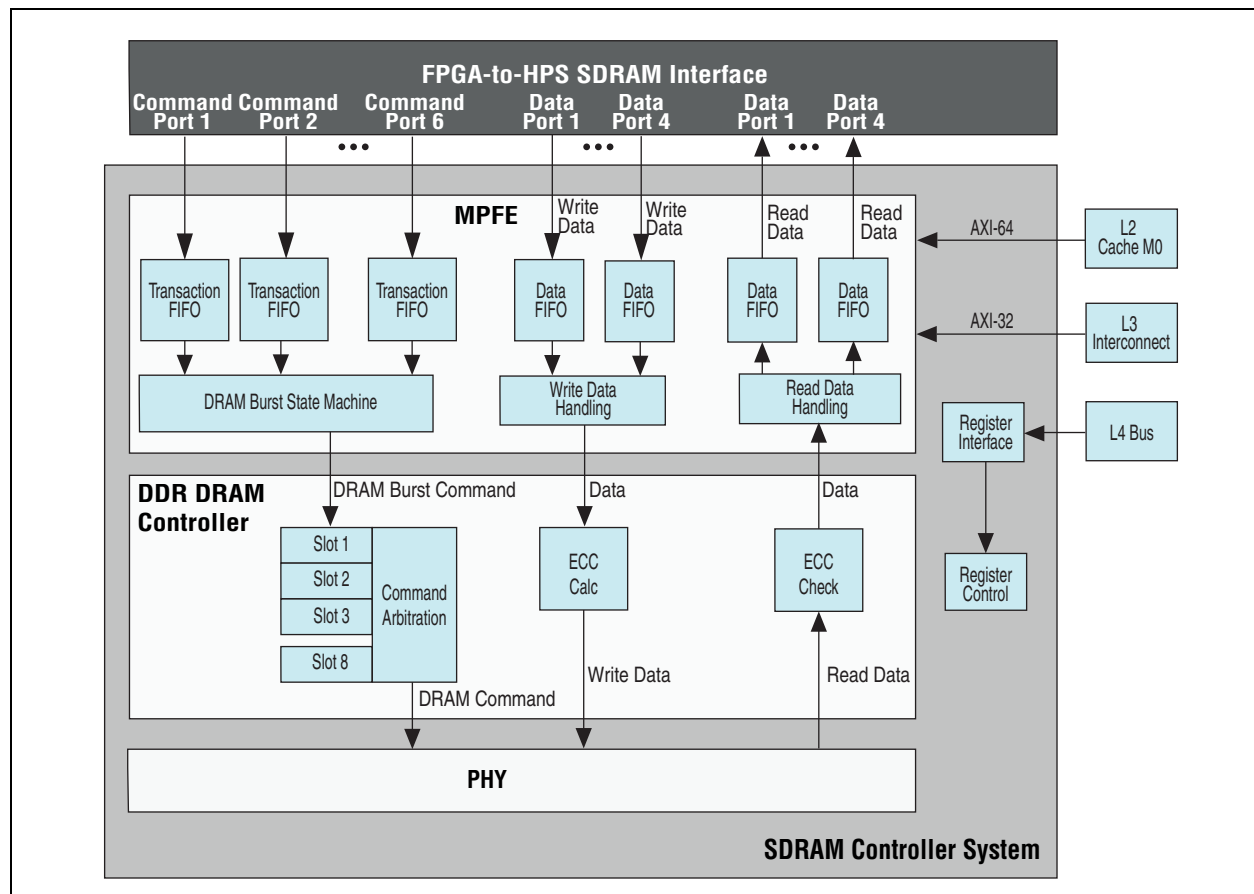
The HPS includes a multiple port front end (MPFE) SDRAM memory controller subsystem that is shared between logic in the FPGA fabric (FPGA-to-HPS SDRAM interface), the processor L2 cache, and the L3 interconnect.

The SDRAM controller provides the following features to maximize memory performance:

- Command reordering (look-ahead bank management)
- Data reordering (out-of-order transactions)
- Deficit round-robin arbitration with aging for bandwidth management
- High-priority bypass for latency-sensitive traffic

Figure 3 shows the SDRAM controller subsystem block diagram.

Figure 3. SDRAM Controller Subsystem



The SDRAM controller subsystem supports the following memory capabilities:

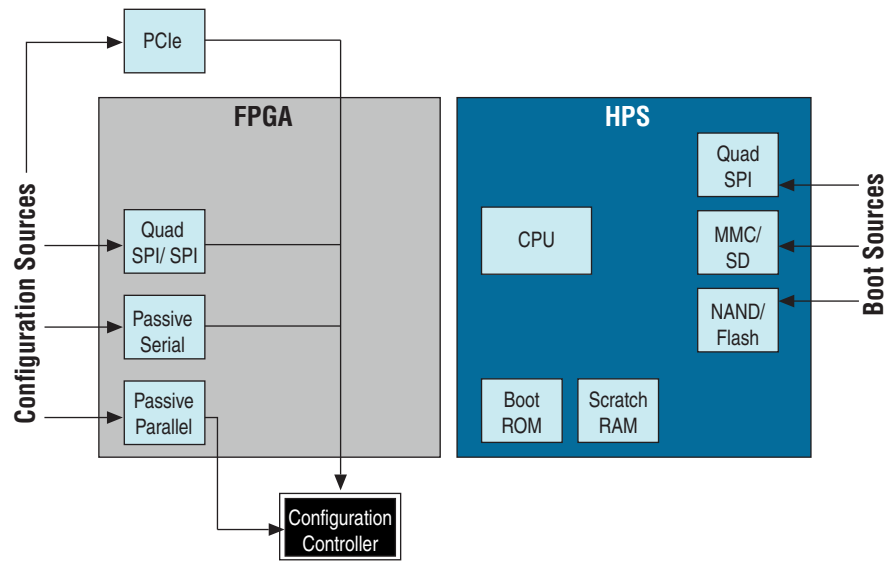
- DDR2, DDR3, LPDDR, or LPDDR2 devices
- Up to 4 Gigabytes (GB) RAM
- Up to 533 MHz (1066 Mbps data rate) in Arria V devices
- Up to 400 MHz (800 Mbps data rate) in Cyclone V devices
- Data width of 8, 16, or 32 bits
- Optional ECC support
- Low voltage 1.35 V DDR3L and 1.2 V DDR3U support
- Full memory device power management support
- 8-bit and 16-bit modes with two chip selects

# FPGA Configuration and Processor Booting

The FPGA fabric and HPS portions of the SoC FPGA are powered independently. Combining this feature with the clock and reset control features provides a wide range of control for power-constrained systems. You can reduce clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric or HPS to reduce total system power.

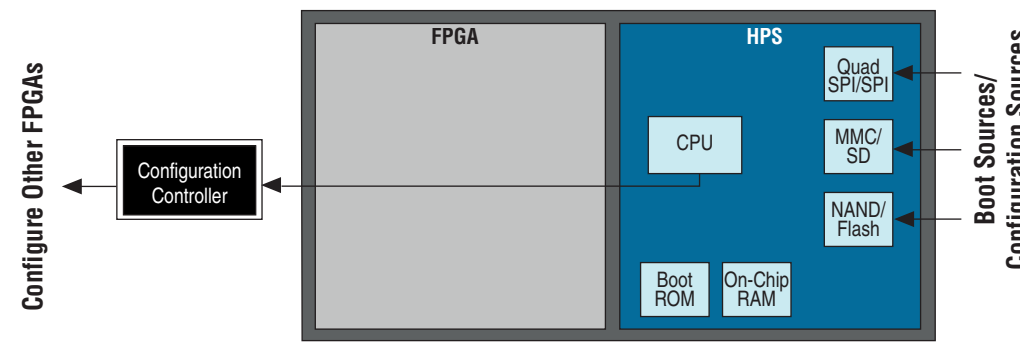
You can configure the FPGA fabric and boot the HPS independently, in any order, providing the ultimate design flexibility, as shown in [Figure 4](#).

**Figure 4. Independent FPGA Configuration and HPS Booting**



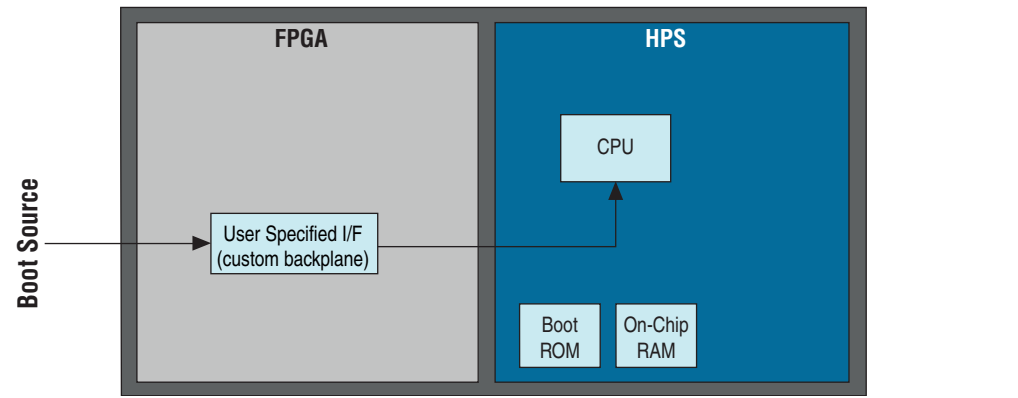
The HPS can boot independently and then configure the FPGA fabric. Once running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller, as shown in [Figure 5](#).

**Figure 5. Configuration of other FPGAs from HPS**



Alternatively, you can configure the FPGA fabric first, and then provide a custom interface over which the HPS boot code is made available, as shown in [Figure 6](#).

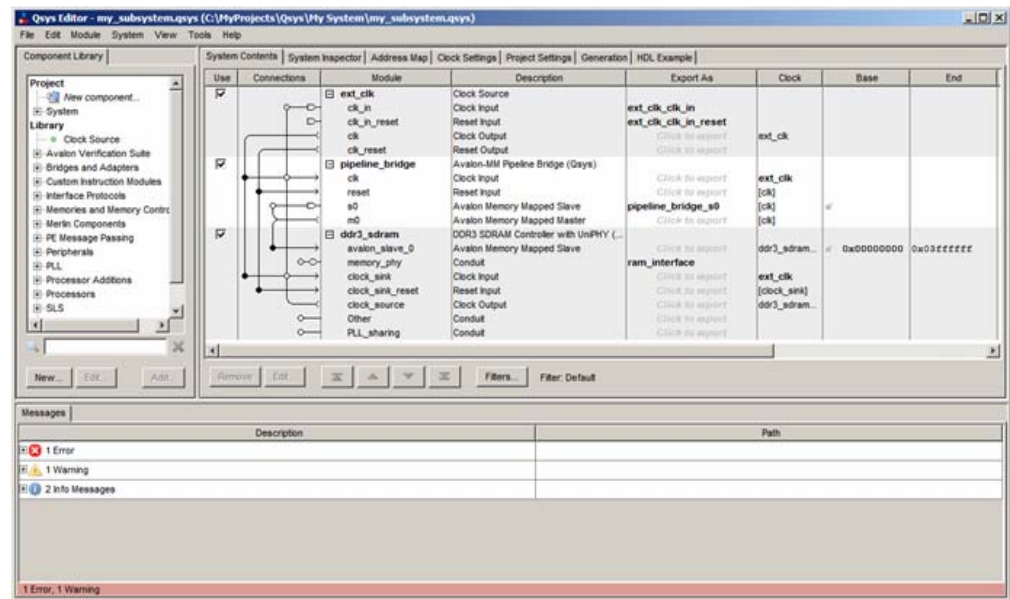
**Figure 6. Boot Code Uploaded Via FPGA**



## Hardware Development

Altera's Qsys system integration tool is the development front end for designing hardware systems using the HPS. Qsys includes a user interface for configuring the HPS and connecting soft logic to the various HPS interfaces, as shown in [Figure 7](#).

**Figure 7. Qsys System Integration Tool**



Qsys automatically generates a system testbench, simulation model, and software handoff file to expedite development across the hardware and software teams. Developers can also connect their FPGA logic to the HPS manually or by using an alternative system integration tool.

The Qsys system integration tool saves time and effort in the FPGA design process. As part of the Quartus II software, the Qsys system integration tool provides the following capabilities:

- Creates a high-performance interconnect based on network-on-chip technology to boost system throughput.
- Supports ARM AMBA AXI, Avalon-MM, and Avalon-ST interfaces.
- Provides a broad portfolio of soft IP cores for embedded, video, image processing, digital signal processing (DSP), interface protocols, and memory controllers for use in the FPGA fabric.
- Supports hierarchical design that allows easy reuse of IP collections as subsystems. Hierarchical design provides a higher level of abstraction, and simplifies the development of a complex system.
- Supports faster board bring-up through real-time system debug using verification IP and the Altera System Console.

## Software Development

Altera's ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 processor, including software development tools and operating systems. This ecosystem compatibility ensures that software developers can remain productive using familiar tools and reuse legacy software to shorten the development cycle.

The software development process for Altera SoC FPGAs follows the same steps as other SoC devices. Altera and its ecosystem partners will provide tool choices for each step of the process, from board bring-up, to building Linux kernels, to debugging application software.

Altera is developing comprehensive operating system support including Linux, VxWorks, and others. Using Altera reference Linux kernel or board support packages for other operating systems, software engineers can start OS-based application development immediately.

Device-specific firmware and software development can begin on the Altera SoC FPGA Virtual Target. The Virtual Target is a fast, host-based functional simulation of a target development system. It functions like a complete development board that runs on a workstation.

Binary- and register-compatible with the real hardware that it simulates, the Virtual Target enables the development of device-specific production software which can run unmodified on real hardware.

Virtual targets provide an unparalleled level of full-system visibility and control for software development. With the use of a virtual target, software development can begin well in advance of hardware availability, and continue to make software teams more productive even after FPGA devices are available.

## Device Family Plan

Cyclone V and Arria V devices are the first Altera FPGA families to integrate an HPS. In addition to the FPGA fabric, the SoC FPGAs include the same hard functional blocks found in Altera's other 28-nm low-power Arria V and Cyclone V FPGAs. The following functional blocks are examples of those found in the family:

- 8-input ALMS

- Variable-precision DSP blocks
- 640-bit memory logic array blocks (MLABs)
- Fractional PLLs
- PCIe IP
- Memory controllers

Cyclone V SoC FPGAs provide the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications from your competition. The Cyclone V SoC family provides the following advantages:

- Low total power consumption
- Low static power consumption
- Efficient logic integration capabilities
- Integrated transceiver variants


The Cyclone V family's total power consumption is up to 40 percent lower than that of the Cyclone IV family. Its static power consumption is up to 30 percent lower. The Cyclone V SoC FPGA family plan includes the following variations:


- Cyclone V SE SoC FPGA with ARM-based HPS
- Cyclone V SX SoC FPGA with ARM-based HPS and integrated 3-Gbps transceivers
- Cyclone V ST SoC FPGA with ARM-based HPS and integrated 5-Gbps transceivers

Arria V SoC FPGAs balance cost and power with performance for mid-range applications such as remote radio units, 10-Gbps/40-Gbps line cards, and in-studio mixers. Arria V FPGAs achieve high system performance because of the fast FPGA fabric, fast I/Os, and fast transceiver data rates. You can also meet your cost and power requirements for applications in this space. The Arria V SoC FPGA family plan includes the following variations:

- Arria V SX SoC FPGA with ARM-based HPS and integrated 6-Gbps transceivers
- Arria V ST SoC FPGA with ARM-based HPS and integrated 10-Gbps transceivers

In addition to GPIOs and transceivers, Cyclone V SoC and Arria V SoC devices include HPS-dedicated I/Os. The HPS-dedicated I/Os support the memory interfaces and system peripherals in the HPS.

 For Cyclone V device family and package information, refer to *Volume 1: Device Overview and Datasheet* of the *Cyclone V Device Handbook*.

 For Arria V device family and package information, refer to *Volume 1: Device Overview and Datasheet* of the *Arria V Device Handbook*.

## Further Information

- SoC FPGA Overview:  
[www.altera.com/devices/processor/soc-fpga/proc-soc-fpga.html](http://www.altera.com/devices/processor/soc-fpga/proc-soc-fpga.html)

- *SoC FPGA ARM Cortex-A9 MPCore Processor Advance information Brief (AIB):*  
[www.altera.com/literature/hb/soc-fpga/aib-01020-soc-fpga-cortex-a9-processor.pdf](http://www.altera.com/literature/hb/soc-fpga/aib-01020-soc-fpga-cortex-a9-processor.pdf)
- *Arria V FPGAs: Balance of Cost, Performance, and Power:*  
[www.altera.com/devices/fpga/arrria-fpgas/arrria-v/arrv-index.jsp](http://www.altera.com/devices/fpga/arrria-fpgas/arrria-v/arrv-index.jsp)
- *Cyclone V FPGAs: Lowest System Cost and Power:*  
[www.altera.com/devices/fpga/cyclone-v-fpgas/cyv-index.jsp](http://www.altera.com/devices/fpga/cyclone-v-fpgas/cyv-index.jsp)
- *Dual-Core ARM Cortex-A9 MPCore Processor*  
[www.altera.com/devices/processor/arm/cortex-a9/m-arm-cortex-a9.html](http://www.altera.com/devices/processor/arm/cortex-a9/m-arm-cortex-a9.html)
- *Using Virtual Target with the ARM Cortex-A9 MPCore Processor:*  
[www.altera.com/devices/processor/arm/cortex-a9/virtual-target/proc-a9-virtual-target.html](http://www.altera.com/devices/processor/arm/cortex-a9/virtual-target/proc-a9-virtual-target.html)
- *Qsys—Altera’s System Integration Tool:*  
[www.altera.com/products/software/quartus-ii/subscription-edition/qsys/qtsqsys.html](http://www.altera.com/products/software/quartus-ii/subscription-edition/qsys/qtsqsys.html)
- *Processors from Altera and Embedded Alliance Partners:*  
[www.altera.com/devices/processor/emb-index.html](http://www.altera.com/devices/processor/emb-index.html)
- *Presentation: “ARM NEON Technology Introduction”:*  
[http://www.arm.com/files/pdf/AT\\_-\\_NEON\\_for\\_Multimedia\\_Applications.pdf](http://www.arm.com/files/pdf/AT_-_NEON_for_Multimedia_Applications.pdf)
- *Webcast: “Getting to Know the ARM-Based SoC FPGA”:*  
[www.altera.com/education/webcasts/all/wc-2011-arm-based-soc-fpga.html](http://www.altera.com/education/webcasts/all/wc-2011-arm-based-soc-fpga.html)
- *Video: “Jump-Start Software Development with the SoC FPGA Virtual Target”:*  
[www.accelcomm.com/acc/socfpga-wp/1/51451958/](http://www.accelcomm.com/acc/socfpga-wp/1/51451958/)
- *White Paper: Strategic Considerations for Emerging SoC FPGAs*  
<http://www.altera.com/literature/wp/wp-01157-embedded-soc.pdf>
- *White Paper: ARM Cortex-A9 Processors*  
<http://www.arm.com/files/pdf/ARMCortexA-9Processors.pdf>

## Document Revision History

Table 1 shows the revision history for this document.

**Table 1. Document Revision History**

Date	Version	Changes
February 2012	1.3	Edited technical figures.
October 2011	1.2	Updated for standard Altera document template.
September 2011	1.1	Updated device family and package plan tables with latest data.
August 2011	1.0	Initial release.

