18. Prototyping Strategy for HardCopy II Devices

H51023-2.0

Introduction

Altera® HardCopy® II devices, manufactured using 1.2-V, 90-nm process technology, are the newest additions to the HardCopy series of structured ASICs and provide a powerful alternative to standard-cell ASICs. HardCopy II devices are the industry's lowest-risk structured ASICs and offer high logic density at a low unit cost, while requiring minimal up-front investment and development time. HardCopy II devices also serve as a low-cost migration device for users of Altera's Stratix® II FPGAs.

Beginning with Quartus® II software version 4.2, you can choose a HardCopy II structured ASIC to use for volume production and prototype a design with a Stratix II FPGA. Prototyping with Stratix II FPGA devices today lets you do early system evaluation while simultaneously planning for eventual migration to HardCopy II devices to reduce unit cost for volume production.

HardCopy II Device Prototyping Benefits

The HardCopy II family builds upon the success of the 0.13-µm HardCopy Stratix and 0.18-µm HardCopy APEX™ devices. The HardCopy II family of devices offers the lowest risk and fastest time-to-market development for structured ASICs by combining the FPGA prototyping and production development into a seamless migration process. Altera's proven seamless migration methodology guarantees first-silicon success by preserving the proven netlist while developing the HardCopy II structured ASIC, thereby minimizing design risk.

Prototyping your HardCopy II design using a Stratix II FPGA reduces the total design risk by addressing key decision areas:

- Verification—Functional verification, system development, and lab testing of the prototype guarantee first-silicon success with the HardCopy II device.
- Time to market—Prototyping in a Stratix II FPGA allows you to do early field trials and gain early market entry with your product. You can evaluate demand uncertainties in the market that might make a standard-cell ASIC too risky and expensive to develop.
- Total cost of ownership—Using HardCopy II devices reduces the total design cost when factoring in recurring engineering expenses for long ASIC design cycles, as well as the increasing infrastructure costs for EDA software, computing hardware, and ASIC vendor fees.

Prototyping and subsequent production with HardCopy II greatly reduces the risk of needing a re-spin of your design for functional bugs.

The Quartus II software integrates with popular EDA industry tools used today by ASIC designers, such as Synopsys DC FPGA, PrimeTime, and VCS; Synplicity Synplify; Mentor Graphics® ModelSim® and Precision; and Cadence NC-Verilog. Additional investment in software is minimal.

For more information on HardCopy Stratix and HardCopy APEX families, refer to their respective sections in the *HardCopy Series Handbook*.

For more information on designing for HardCopy II devices, see the *Quartus II Support for HardCopy II Devices* and *Migrating Stratix II Device Resources to HardCopy II Devices* chapters in the HardCopy Series Device Handbook.

HardCopy II Prototyping Options

The FPGA prototyping strategy allows you to verify your hardware description language (HDL) code, software for embedded processors, and system integration by having a working silicon prototype of your planned HardCopy II device. The variety of Stratix II devices that are available offers flexibility in choosing which FPGA to use as the prototype for your HardCopy II design.

There are multiple prototyping options possible using Stratix II and HardCopy II devices. The final logic resource, memory, and pin usage of the HardCopy II design are key determinants for selecting the appropriate Stratix II FPGA for prototyping. Table 18–1shows the suitable migration paths between Stratix II and HardCopy II devices.

Table 18–1. HardCopy II Device Family Features (Part 1 of 2)

Feature	HC210W *(1)*	HC210	HC220	HC230	HC240
ASIC gates *(2)*	1,000,000	1,000,000	1,600,000	2,200,000	2,200,000
Additional gates for digital signal processing (DSP) block *(3)*	0	0	300,000	700,000	1,400,000
M4K RAM blocks (4 Kbits plus parity)	190	190	408	614	816
M-RAM blocks (512 Kbits plus parity)	0	0	2	6	9
Total RAM bits (including parity bits)	875,520	875,520	3,059,712	6,368,256	9,068,544

Table 18–1. HardCopy II Device Family Features (Part 2 of 2)

Feature	HC210W *(1)*	HC210	HC220	HC230	HC240
Enhanced PLLs	2	2	2	4	4
Fast PLLs	2	2	2	4	8
Maximum user I/O pins *(4)*, *(5)*	*(6)*	334	494	698	951
FPGA prototype options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180

Notes to Table 18–1:

(1) HC210W devices are in a wire-bond package. All other HardCopy II devices and Stratix II FPGAs use a flip-chip package. Devices in a wire-bond package offer different performance and signal integrity characteristics compared to devices in a flip-chip package.
(2) This is the number of ASIC gates available in the HardCopy II base array for both logic and DSP functions that can be implemented in a Stratix II FPGA prototype.
(3) This number includes additional ASIC gates available for Stratix II DSP functions.
(4) The I/O pin counts include the dedicated `CLK` input pins, which can be used for clock signals or data inputs.
(5) The Quartus II I/O pin counts include an additional pin (`PLLENA`), which is not available as a general-purpose I/O pin. The `PLLENA` pin can only be used to enable the PLLs.
(6) Contact Altera® Applications for more information.

For example, referring to Table 18–1, you can see that a design estimated to contain 2 million ASIC gates, 6 Mbits of memory, and 500 user I/O pins would best fit into the HC230F1020 device. The design can be prototyped in the EP2S90F1020, EP2S130F1020, or EP2S180F1020 devices.

For more detailed information on the HardCopy II device family resources and architecture, see the *HardCopy II Device Family Data Sheet* in the *HardCopy Series Handbook*.

Unified Design Methodology

One benefit of using Stratix II devices to prototype HardCopy II devices is that they share the same development flow. The steps to develop a regular Stratix II FPGA are the same as to prototype a HardCopy II device. This unified design methodology saves you the complexity of managing different sets of EDA tools for FPGA and ASIC development.

Beginning with Quartus II software version 4.2, you can design your HardCopy II prototype using a Stratix II device and verify the design in-system to meet functionality specifications.

Once you are satisfied with your Stratix II FPGA, you can use the HardCopy II Utilities to create your HardCopy II Companion Revision and compile your design for the desired HardCopy II device. The HardCopy II Utilities also verify your design is functionally equivalent to your Stratix II FPGA prototype.

HardCopy II Utilities

Beginning in version 5.0 of the Quartus II software, the HardCopy II Utilities (Projects menu) is available to help you design for Stratix II FPGA prototype devices and HardCopy II companion devices. These utilities are described in detail in the *Quartus II Support for HardCopy II Devices* chapter of the *HardCopy Series Devices Handbook*.

The HardCopy II Utilities features the HardCopy II Advisor, which provides a step by step checklist for your design process as you progress from Stratix II FPGA prototyping to HardCopy II companion device development. You can run the HardCopy II Advisor frequently throughout the design process, and can be used while developing for the Stratix II FPGA revision design as well as the HardCopy II companion revision design. The HardCopy II Advisor identifies different tasks depending on which device (the Stratix II or HardCopy II device) is the active device in the current project revision open in the Quartus II software.

Figure 18–1 shows the HardCopy II Advisor with the Stratix II device selected.

Figure 18–1. HardCopy II Advisor

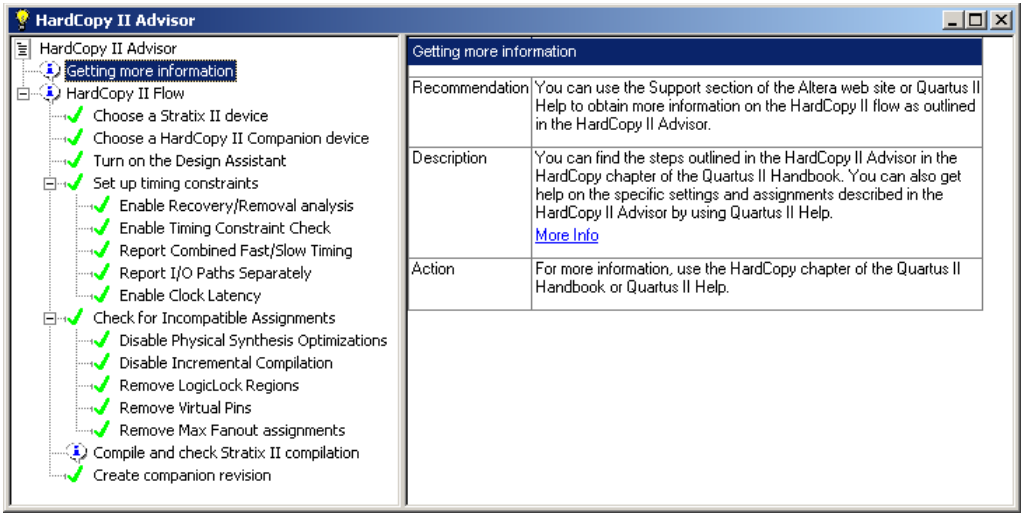
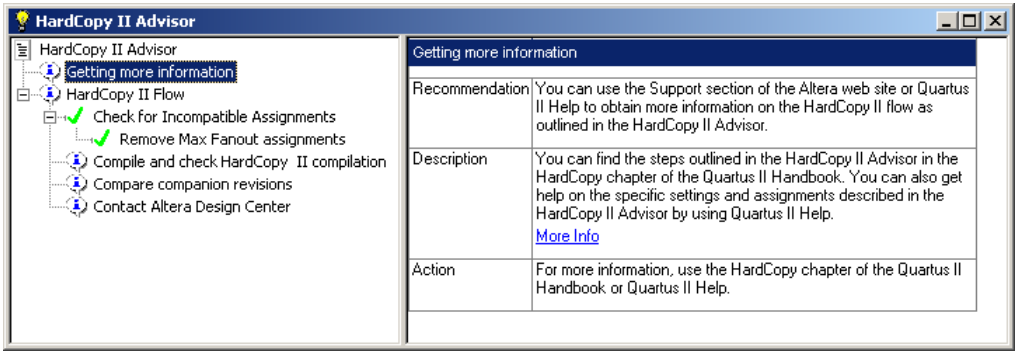


Figure 18–2 shows the HardCopy II Advisor with the HardCopy II device selected.

Figure 18–2. HardCopy II Device Selected in the Advisor



HardCopy II Overall Design Flow

In order to use HardCopy II structured ASICs, first build your prototype design in a migration-compatible Stratix II device. The selection of which Stratix II and HardCopy II devices to use is design dependent. However not all Stratix II FPGA devices are suitable prototypes for HardCopy II structured ASICs. The Stratix II FPGA devices that are suitable for prototyping your HardCopy II design are shown in Table 18–1 on page 18–2. After a design is compiled for a Stratix II device, the Quartus II Fitter reports the resource utilization of the Stratix II device for comparison to the HardCopy II devices.

The following resources used in your design are some of the key determinants as to which HardCopy II device to target:

- Packaging
- I/O pins
- I/O buffer types (differential, PCI/PCI-X, DDR, etc.)
- Memory bit count and block count (M4K and M-RAM blocks)
- PLLs
- Delay-locked loops (DLLs)
- DSP blocks
- Logic gates (Stratix II adaptive logic modules)

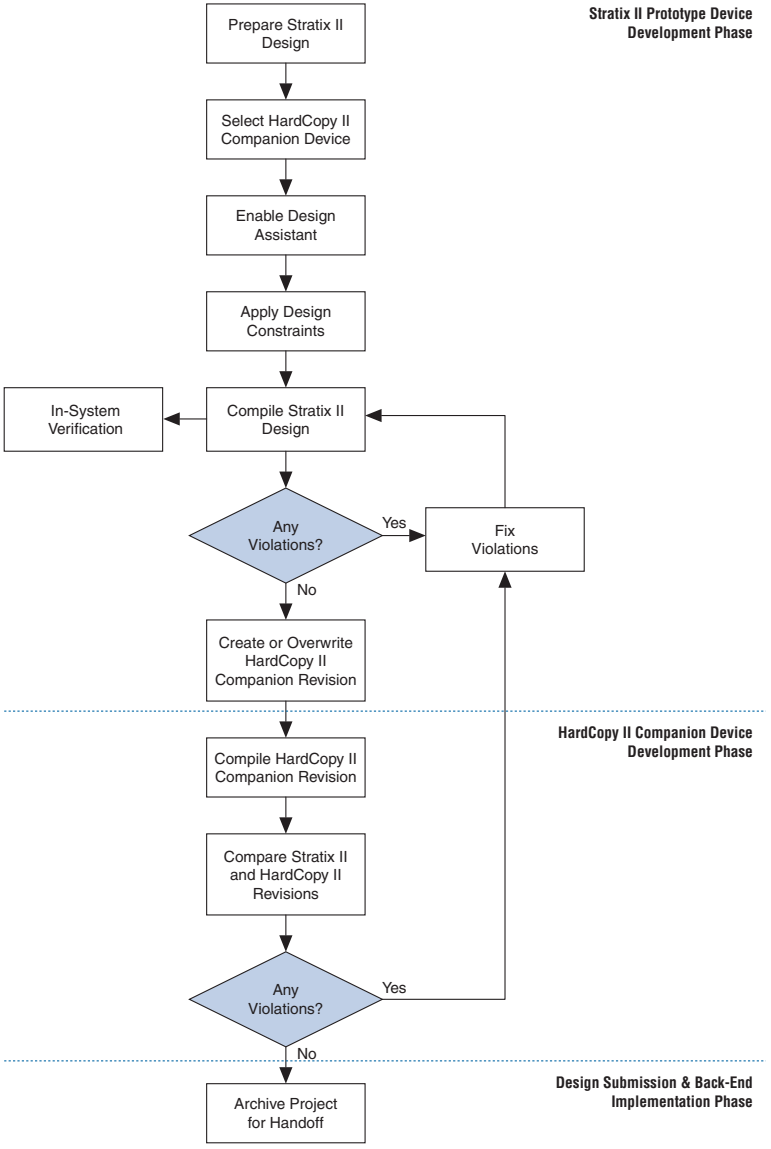
Once you have a general idea how many logic gates, memory bits, and I/O signals are required for your design, you can select a Stratix II FPGA and perform an initial compilation of the design using the Quartus II software. The total usable gates of HardCopy II devices is estimated in terms of ASIC gates, which you should use in your gate count estimates.

The HardCopy II design flow has three main phases:

- Stratix II FPGA prototype development
- HardCopy II companion device development
- Design submission and back-end implementation.

Figure 18–3 shows the entire HardCopy II design flow at a high level.

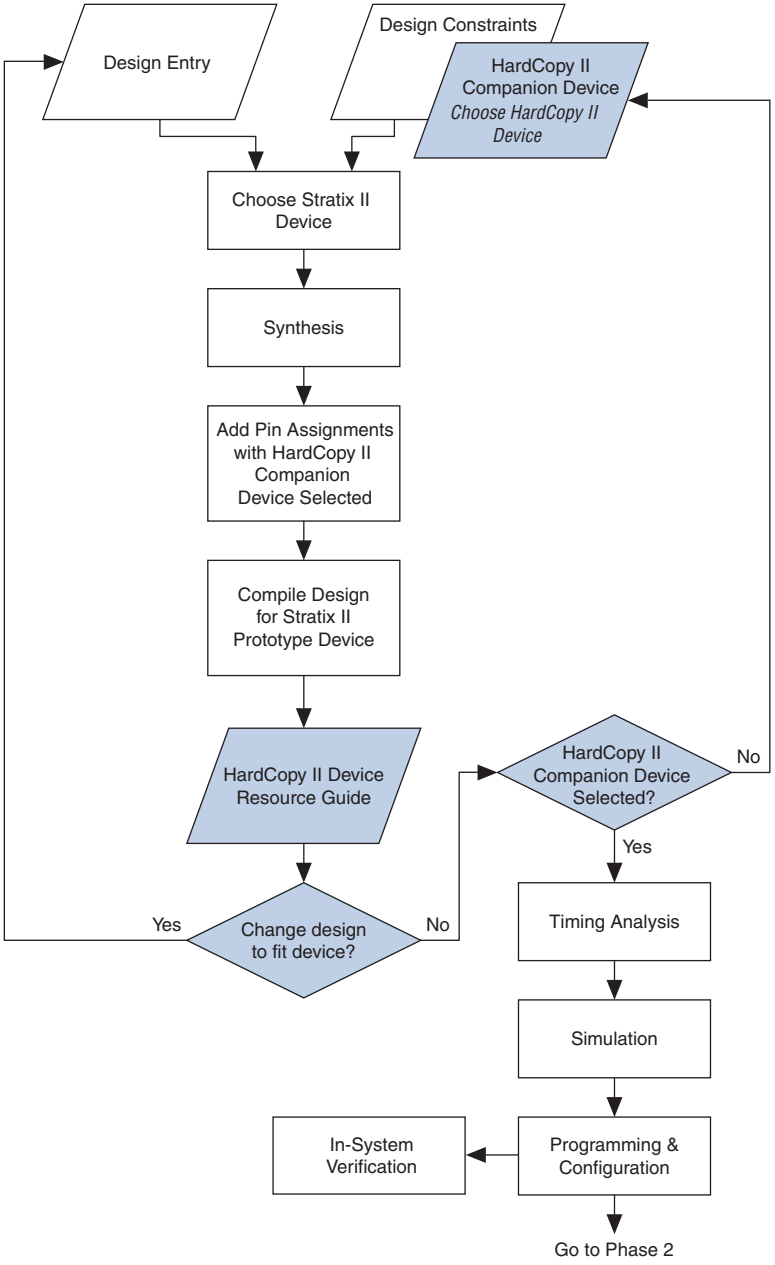
Figure 18–3. HardCopy II Device Overall Design Flow



Stratix II Prototype Device Development

The first phase of the design process for the Stratix II prototype of the HardCopy II device follows the traditional FPGA development flow using the Quartus II software in most respects. Figure 18–4 shows the high-level design methodology for prototyping HardCopy II designs using Stratix II FPGAs and the available features in the Quartus II software. Each stage is explained further in the following sections.

Figure 18–4. Stratix II Prototype Device Design Flow



For full details of the Quartus II software's features and design flow, see the *Introduction to Quartus II* manual in the **Products > Literature > Quartus II** section of the Altera web site (**www.altera.com**).

Design Entry for HardCopy II Prototypes

One of the key advantages in the HardCopy II design flow is the ability to re-use HDL code without modification between FPGA and ASIC versions of the design. For most standard-cell ASIC designs, HDL code written for the prototype FPGA needs to be customized for implementation in the ASIC vendor's design flow. The unified design methodology for HardCopy II devices and prototype FPGAs lets you maintain a single version of your HDL that is used for both the prototype FPGAs and production structured ASICs.

Prototype HardCopy II designs can be developed in VHDL and Verilog HDL languages. In addition to Verilog and VHDL development, schematic entry and system level design using SOPC Builder can be done within the Quartus II software. The HDL coding guidelines used for Stratix II devices apply to HardCopy II devices.

For more information on HDL coding guidelines, see the *Recommended HDL Coding Styles* chapter in Volume 1 of the *Quartus II Handbook*.

Constructing your HDL code for application to the Stratix II architecture and adhering to Altera's recommended HDL coding styles will help ensure a successful design migration to HardCopy II devices.

Design Constraints for HardCopy II Prototypes

In order to achieve high performance and area optimization of your design in the Quartus II software, you must add design constraints. Quartus II software has many features and constraint settings to optimize the design compilation of your prototype. Design constraints such as Logic Lock regions, clock definitions, timing constraints, I/O buffer types, pin assignments, and Fitter optimization allow you to achieve the best performance and smallest area possible in your Stratix II prototype of your HardCopy II device. Version 5.0 of the Quartus II software does not support LogicLock regions in HardCopy II devices.

For more information on the Quartus II software scripting, constraint entry, I/O planning, area optimization, and timing closure, see Volume 2 of the *Quartus II Handbook*.

Most constraint settings depend on your design and system requirements, but a few settings are required to create a HardCopy II prototype:

- Specify a Stratix II device and HardCopy II companion device.
- Turn on recommended settings in Quartus II software
- Do not assign pinouts until after selecting a HardCopy II companion device and compiling the design.

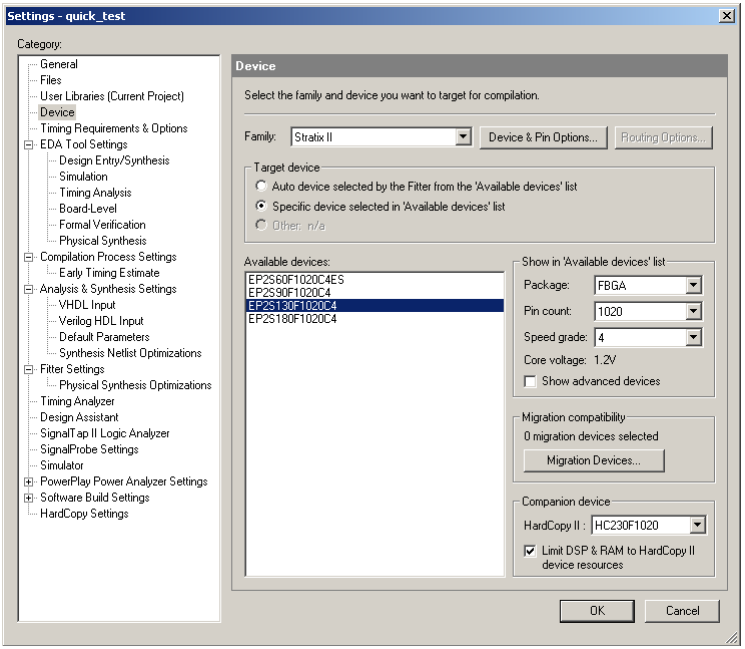
Specify a Stratix II Device & HardCopy II Companion Device

Specify a Stratix II device or, if you are not sure which device to use, specify the Stratix II family. If you specify the family, the Quartus II Fitter selects the smallest Stratix II device that fits your design. To specify a device, open the **Device** category of the **Settings** dialog box (Assignments menu).

If you know which HardCopy II device your design is targeting, you can specify the HardCopy II companion device in the Quartus II software **Settings** dialog box. Selecting a companion device limits the I/O and PLL resources to what is available in the HardCopy II device. When you set the **Limit DSP & RAM to HardCopy II device resources** option, the Quartus II software will not use M512 memory blocks and limit the use of DSP, M4K, and M-RAM blocks to guarantee your design is compatible for both your Stratix II and HardCopy II devices. You can temporarily turn off the **Limit DSP & RAM** setting for prototype verification and in-system debugging using the Signal Tap II Logic Analyzer.

Figure 18–5 shows the **Settings** dialog box.

Figure 18–5. Quartus II Settings Dialog Box



Design Rule Checking

The Quartus II Design Assistant examines the project for design rule violations that affect the implementation in Altera devices. The Design Assistant rule check can be performed for any FPGA design, but it is required for all HardCopy designs. The current Design Assistant rules apply to HardCopy II designs as well as to HardCopy Stratix and HardCopy APEX designs.

For more information on the design rules checked by the Design Assistant in the Quartus II software, see the *HardCopy Series Design Guidelines* chapter of the *HardCopy Series Handbook* or refer to topics on Design Assistant in the Quartus II Help.

Synthesis for HardCopy II Prototypes

Designing with HardCopy II devices saves you the effort of purchasing additional EDA software. The EDA tools you would use for an FPGA design can also be used for your HardCopy II device prototyping. You can synthesize your VHDL or Verilog HDL code to the Stratix II library

using Quartus II Integrated Synthesis or with the approved synthesis software from an Altera Commitment to Cooperative Engineering Solutions (ACCESS) Program partner.

For a list of ACCESS Program® partners, see the **Products > Design Software > EDA Partners** section of the Altera web site (**www.altera.com**).

For more information on using these HDL synthesis options with Altera device families, see the *Synthesis* section in Volume 1 of the *Quartus II Handbook*.

Use the Stratix II library to synthesize your HardCopy II prototype, since your initial prototype will be in a Stratix II FPGA. Synthesis of your HardCopy II prototype device will follow the same synthesis guidelines as for a Stratix II design.

Pin Assignments

Do not make pin assignments without compiling the design at least once with a HardCopy II companion device selected. After you select a companion device, you can use the Pin Planner feature or Assignment Editor to select pins on the package and place your signals. After you assign all pin locations, you should recompile the design and run the IO Assignment Analysis feature to verify that your I/O pin assignments are valid and do not have signal integrity conflicts.

Quartus II Fitter for Stratix II Prototype Device

The Stratix II device prototyping flow does not require purchasing additional place-and-route software. The Quartus II Fitter places and routes your design into the device specified in your Quartus II project. If a HardCopy II device is also specified through the **Device Settings** dialog box, the Fitter constrains the prototype's pin assignments to be fully compatible with the HardCopy II device.

After the Fitter has run, the Quartus II software generates the HardCopy II Device Resource Guide in the Fitter section of the Compilation Report. This resource guide helps you select which HardCopy II device to use.

HardCopy II Device Resource Guide

The Quartus II software provides information on your compiled design that assists you in selecting which HardCopy II device is suitable for your compiled Stratix II design. The HardCopy II Device Resource Guide is automatically generated after a successful compilation of a Stratix II

design. Using this report, you can identify which HardCopy II device meets your design needs. The Device Resource Guide highlights which categories of resources are limiting your choice of HardCopy II devices. Use this guide to make trade-off decisions about your design's functionality and what resources it uses to select the most cost-effective HardCopy II device for production. An example of the HardCopy II Device Resource Guide is shown in Figure 18–6.

Figure 18–6. HardCopy II Device Resource Guide

HardCopy II Device Resource Guide

Color Legend:
-- Green:
-- Package Resource: The HardCopy II package can be migrated from the Stratix II FPGA selected package, and the design has been fitted

	Resource	Stratix II EP2S130	HC210W*	HC210	HC220	HC220	HC230	HC240	HC240
1	Migration Compatibility			None	None	None	Medium	None	None
2	Primary Migration Constraint			Package	Package	Package	Package	Package	Package
3	Package	FBGA - 1020	FBGA - 484	FBGA - 484	FBGA - 672	FBGA - 780	FBGA - 1020	FBGA - 1020	FBGA - 1508
4	Logic	--		40%	22%	22%	15%	10%	10%
5	-- Logic cells	35640 ALUTs		--	--	--	--	--	--
6	-- DSP elements	0		--	--	--	--	--	--
7	Pins								
8	-- Total	515		515 / 335	515 / 493	515 / 495	515 / 699	515 / 743	515 / 952
9	-- Differential Input	0		0 / 70	0 / 90	0 / 90	0 / 128	0 / 224	0 / 272
10	-- Differential Output	0		0 / 50	0 / 70	0 / 70	0 / 112	0 / 200	0 / 256
11	-- PCI / PCI-X	0		0 / 167	0 / 245	0 / 247	0 / 359	0 / 367	0 / 472
12	-- DQ	0		0 / 18	0 / 44	0 / 44	0 / 178	0 / 178	0 / 178
13	-- DQS	0		0 / 8	0 / 18	0 / 18	0 / 72	0 / 72	0 / 72
14	Memory								
15	-- M-RAM	6		6 / 0	6 / 2	6 / 2	6 / 6	6 / 9	6 / 9
16	-- M4K blocks & M512 blocks	44		44 / 190	44 / 408	44 / 408	44 / 614	44 / 816	44 / 816
17	PLLs								
18	-- Enhanced	2		2 / 2	2 / 2	2 / 2	2 / 4	2 / 4	2 / 4
19	-- Fast	0		0 / 2	0 / 2	0 / 2	0 / 4	0 / 8	0 / 8
20	DLLs	0		0 / 1	0 / 1	0 / 1	0 / 2	0 / 2	0 / 2
21	SERDES								
22	-- RX	0		0 / 21	0 / 31	0 / 31	0 / 46	0 / 92	0 / 116
23	-- TX	0		0 / 19	0 / 29	0 / 29	0 / 44	0 / 88	0 / 116
24	Configuration								
25	-- CRC	0		0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
26	-- ASMI	0		0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
27	-- Remote Update	0		0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
28	-- JTAG	0		0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1

* Device is preliminary. Overall performance is expected to be degraded.

The report example in Figure 18–6 shows the resource estimates for a design compiled for a Stratix II EP2S130F1020 device. Based on the report information, the device selection is restricted due to package types being incompatible with the Stratix II device. The HC210 and HC220 devices are also restricted due to the total number of pins and the number of M-RAM memory blocks required. So the HC230F1020 device in the

1,020-pin FineLine BGA package would be an appropriate HardCopy II device for migration. If you want to target the HC220F780 device for this example design, reduce the total number of I/O pins used and the number of M-RAM blocks implemented, and change the Stratix II device to a compatible form such as the EP2S130F780 device.

For more information on the HardCopy II Device Resource Guide, see the *Quartus II Support for HardCopy II Devices* chapter of the *HardCopy Series Handbook*.

Timing Analysis for Stratix II Prototype Device

Timing analysis is performed by the Quartus II software automatically during a full compilation. No additional EDA tools are required for static timing analysis of your prototype in a Stratix II device, but you can also use Synopsys PrimeTime if you are more comfortable with that static timing analysis software. Timing analysis can be run independently for maximum and minimum operating conditions without requiring a re-compilation in the Quartus II software.

If timing and area results do not meet your requirements, modifying the constraints for synthesis or Fitter compilation may be necessary. Modifying the HDL code may also yield improved results. This is another advantage of the HardCopy II prototyping flow. The optimization you perform for the Stratix II FPGA is also implemented in your HardCopy II device because of the unified design methodology using the Quartus II software. All of your HDL and synthesis changes are maintained because you only need to maintain one version of your design to use in both FPGA prototype and ASIC production.

If timing meets your requirements, the Stratix II implementation of your prototype design can be used in a chip-level environment.

For more information on the Quartus II Timing Analyzer and Synopsys PrimeTime support, see the *Timing Analysis* section in Volume 3 of the *Quartus II Handbook*.

Simulation for Stratix II Prototype Device

Prototype verification often requires running functional simulation of RTL code in conjunction with in-system debugging and software development. The Quartus II EDA Netlist Writer writes functional simulation netlists for use in several popular third-party simulation platforms, including Mentor Graphics ModelSim, Synopsys VCS, and Cadence NC-Verilog.

For more information on using third-party simulation software for Altera devices, see the *Simulation* section in Volume 3 of the *Quartus II Handbook*.

In-System Verification for Stratix II Prototype Device

Simulation of multi-million gate ASIC designs can take a long time to run. The HardCopy II prototyping strategy is a time-saving solution for this. You can prototype your design, and verify it and your software in-system. This saves you time in the design cycle by allowing you to make fast regression tests that can be verified in the development lab. The Quartus II Assembler generates programming files in several different formats for use in prototyping evaluation and in-system verification.

On-chip debugging of your prototype can be done using several Altera features including the SignalProbe™ feature, and the SignalTap® II Embedded Logic Analyzer. Debugging by engineering change order can be done through the use of Chip Editor. Incremental compilation and in-system updating of memory and constants help save time between design iterations. These features allow for interactive debugging of the Stratix II prototype of your HardCopy II device faster than simulation testing.

Changes made through on-chip debugging will not migrate to the HardCopy II device. When you finish debugging, make the changes in the RTL source code and recompile the design. Then repeat your in-system verification.

For more information about using on-chip debugging capabilities with Stratix II devices, see the *On-Chip Debugging* section in Volume 3 of the *Quartus II Handbook*.

HardCopy II Companion Device Design Flow

After you compile the design for both a Stratix II FPGA and HardCopy II companion device, you should finalize your pin assignments and timing constraints. The Quartus II software uses the same timing constraints for the Stratix II FPGA for the HardCopy II device for timing closure. Therefore, you must constrain all parts of your design for maximum and minimum delay.

After pin assignments and timing constraints are complete, you can move to phase two of the HardCopy II design flow and create a HardCopy II companion revision of your design using the HardCopy II Utilities (Project menu). The companion revision targets the HardCopy II device. The ability to switch between FPGA and HardCopy II revisions within the same Quartus II project allows for seamless migration and verification between the two devices.

For more information on the HardCopy II Utilities, see the *Quartus II Support for HardCopy II Devices* chapter in the *HardCopy Series Device Handbook*.

Compile HardCopy II Companion Revision

After you create the HardCopy II companion revision, you can change the Quartus II project current revision to that companion revision and compile the HardCopy II device. You can change your assignments in the HardCopy II device to suit your needs, but all changes must be verified against the Stratix II FPGA design.

Compare HardCopy II Companion Revision

Once the compile of the HardCopy II device is complete, examine the HardCopy II Advisor report to see if you missed any tasks. If you discovery any warnings from the HardCopy II Advisor, you must fix them in the FPGA and/or HardCopy II device to continue.

After reviewing the HardCopy II advisor, you can compare the HardCopy II companion revision to the Stratix II FPGA prototype revision using the **Compare HardCopy II Companion Revision** feature in the HardCopy II Utilities (Project Menu). If you discover any warnings from the comparison report, you will need to fix them in the FPGA and/or HardCopy II device to continue.

Design Submission

After you compile and compare the HardCopy II companion revision of your design, you are ready to submit your design to the Altera HardCopy Design Center. In order to move to phase three of the HardCopy II design flow, you must meet the following milestones:

- Follow all recommendations in the HardCopy II Advisor so there are no warnings after compiling both the Stratix II FPGA and HardCopy II companion revisions
- An error free HardCopy II companion comparison report
- Timing constraints provided for all I/O pins and clock settings provided for all clock sources
- All critical and high-severity warnings in the Design Assistant have been corrected

If your design meets these milestones, you can archive the entire Quartus II project and submit it to Altera's HardCopy Design Center.

Conclusion

You can begin prototyping your HardCopy II design today in a Stratix II device. The ability to prototype your HardCopy II structured ASIC design in a Stratix II device gives you the fastest development cycle in the structured ASIC market. Altera's unified design methodology for HardCopy II devices preserves changes made to the prototype implemented in a Stratix II device, so no optimization work is lost when you begin the production of your HardCopy II design. You can verify the design in-system, as well as allowing software development to progress in parallel with the verification effort. This rapid verification allows you to gain early market entry with the Stratix II prototype while you migrate the design to a HardCopy II device. The HardCopy II devices provide a low-cost and low-risk ASIC solution, minimizing the total cost of design as compared to a standard-cell ASIC. HardCopy II devices also provide guaranteed functional equivalence between your prototype Stratix II FPGA and production HardCopy II structured ASIC device, reducing the risk of a costly design re-spin.