



# 1. Introduction to HardCopy Stratix Devices

H51001-2.4

## Introduction

HardCopy® Stratix® structured ASICs, Altera's second-generation HardCopy structured ASICs, are low-cost, high-performance devices with the same architecture as the high-density Stratix FPGAs. The combination of Stratix FPGAs for prototyping and design verification, HardCopy Stratix devices for high-volume production, and the Quartus® II design software beginning with version 3.0, provide a complete and powerful alternative to ASIC design and development.

HardCopy Stratix devices are architecturally equivalent and have the same features as the corresponding Stratix FPGA. They offer pin-to-pin compatibility using the same package as the corresponding Stratix FPGA prototype. Designers can prototype their design to verify functionality with Stratix FPGAs before seamlessly migrating the proven design to a HardCopy Stratix structured ASIC.

The Quartus II software provides a complete set of inexpensive and easy-to-use tools for designing HardCopy Stratix devices. Using the successful and proven methodology from HardCopy APEX™ devices, Stratix FPGA designs can be seamlessly and quickly migrated to a low-cost ASIC alternative. Designers can use the Quartus II software to design HardCopy Stratix devices to obtain an average of 50% higher performance and up to 40% lower power consumption than can be achieved in the corresponding Stratix FPGAs. The migration process is fully automated, requires minimal customer involvement, and takes approximately eight weeks to deliver fully tested HardCopy Stratix prototypes.

The HardCopy Stratix devices use the same base arrays across multiple designs for a given device density and are customized using the top two metal layers. The HardCopy Stratix family consists of the HC1S25, HC1S30, HC1S40, HC1S60, and HC1S80 devices. [Table 1-1](#) provides the details of the HardCopy Stratix devices.

**Table 1–1. HardCopy Stratix Devices and Features**

Device	LEs (1)	M512 Blocks	M4K Blocks	M-RAM Blocks	DSP Blocks (2)	PLLs (3)
HC1S25	25,660	224	138	2	10	6
HC1S30	32,470	295	171	2 (4)	12	6
HC1S40	41,250	384	183	2 (4)	14	6
HC1S60	57,120	574	292	6	18	12
HC1S80	79,040	767	364	6 (4)	22	12

**Notes to Table 1–1:**

- (1) LE: logic elements.
- (2) DSP: digital signal processing.
- (3) PLLs: phase-locked loops.
- (4) In HC1S30, HC1S40, and HC1S80 devices, there are fewer M-RAM blocks than in the equivalent Stratix FPGA. All other resources are identical to the Stratix counterpart.

## Features

HardCopy Stratix devices are manufactured on the same 1.5-V, 0.13  $\mu\text{m}$  all-layer-copper metal fabrication process (up to eight layers of metal) as the Stratix FPGAs.

- Preserves the functionality of a configured Stratix device
- Pin-compatible with the Stratix counterparts
- On average, 50% faster than their Stratix equivalents
- On average, 40% less power consumption than their Stratix equivalents
- 25,660 to 79,040 LEs
- Up to 5,658,408 RAM bits available
- TriMatrix memory architecture consisting of three RAM block sizes to implement true dual-port memory and first-in-first-out (FIFO) buffers
- Embedded high-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device which provide identical features as the FPGA counterparts, including spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, advanced multiplication, and phase shifting
- Supports numerous single-ended and differential I/O standards
- Supports high-speed networking and communications bus standards including RapidIO™, UTOPIA IV, CSIX, HyperTransport technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Differential on-chip termination support for LVDS

- Supports high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast-cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for multiple intellectual property (IP) megafunctions from Altera® MegaCore® functions, and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- Available in space-saving flip-chip FineLine BGA® and wire-bond packages (Tables 1–2 and 1–3)
- Optional emulation of original FPGA configuration sequence
- Optional instant-on power-up



The actual performance and power consumption improvements over the Stratix equivalents mentioned in this data sheet are design-dependent.

**Table 1–2. HardCopy Stratix Device Package Options and I/O Pin Counts**  
*Note (1)*

Device	672-Pin FineLine BGA (2)	780-Pin FineLine BGA (3)	1,020-Pin FineLine BGA (3)
HC1S25	473		
HC1S30		597	
HC1S40		613 (4)	
HC1S60			782
HC1S80			782

**Notes to Table 1–2:**

- (1) Quartus II I/O pin counts include one additional pin, PLEENA, which is not a general-purpose I/O pin. PLEENA can only be used to enable the PLLs.
- (2) This device uses a wire-bond package.
- (3) This device uses a flip-chip package.
- (4) In the Stratix EP1S40F780 FPGA, the I/O pins U12 and U18 are general-purpose I/O pins. In the FPGA prototype, EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE, and in the HardCopy Stratix HC1S40F780 device, U12 and U18 must be connected to ground. The EP1S40F780\_HARDCOPY\_FPGA\_PROTOTYPE and HC1S40F780 pin-outs are identical.

**Table 1–3. HardCopy Stratix Device Package Sizes**

Device	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA
Pitch (mm)	1.00	1.00	1.00
Area (mm <sup>2</sup> )	729	841	1,089
Length × width (mm × mm)	27 × 27	29 × 29	33 × 33

## Document Revision History

Table 1–4 shows the revision history for this chapter.

**Table 1–4. Document Revision History**

Date and Document Version	Changes Made	Summary of Changes
September 2008 v2.4	Revised chapter number and metadata.	—
June 2007 v2.3	Updated Introduction section. Updated Table 1–2.	—
December 2006 v2.2	Updated revision history.	—
March 2006	Formerly chapter 5; no content change.	—
October 2005 v2.1	Minor edits	—
January 2005 v2.0	Minor edits	—
June 2003 v1.0	Initial release of Chapter 5, <i>Introduction to HardCopy Stratix Devices</i> , in the <i>HardCopy Device Handbook</i> .	—