

This chapter discusses the available options for mapping from a Stratix[®] III device to a HardCopy[®] III device.

The Quartus II software limits resources to those available to both the Stratix III FPGA and the HardCopy III ASIC. It also ensures that the design revision targeting a HardCopy III device retains the same functionality as the original Stratix III design.

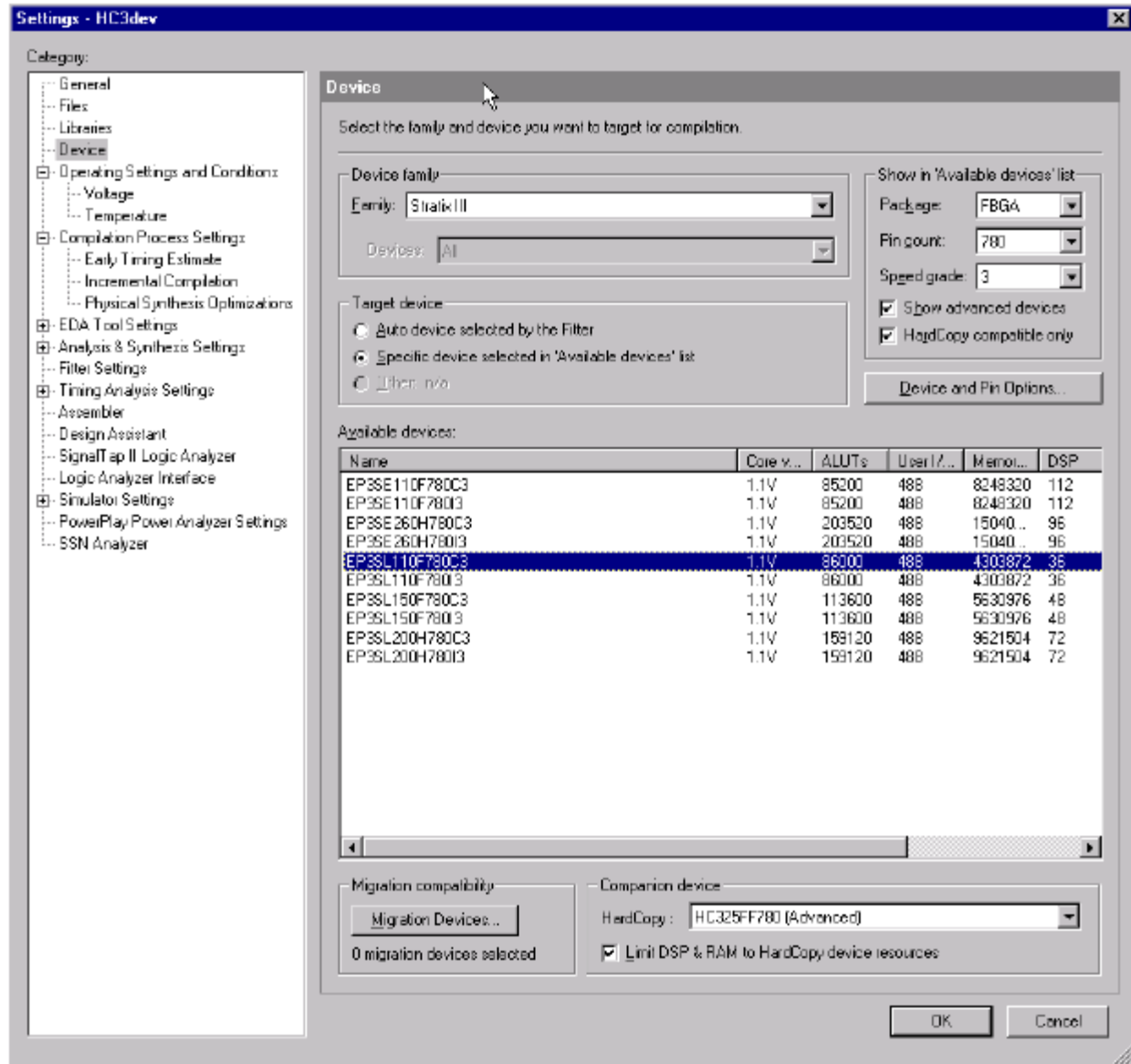
When compiling designs with the Quartus II software, you can specify one HardCopy III target device and one or more Stratix III mapping devices. When you specify at least one mapping device, the Quartus II compiler constrains I/O pins and relevant hard IP blocks to the minimum resources available in any of the selected mapping devices. This feature allows vertical mapping between devices using the same package footprint.

Selecting a HardCopy III device as a companion device is similar to adding another Stratix III device to the mapping device chain. The Quartus II software compiles the design to use the common resources available in all of the selected Stratix III and HardCopy III devices.


The HardCopy III companion device becomes the target device when you create the HardCopy companion revision.

Figure 3-1 shows the **Device** page of the **Settings** dialog box, where you choose the companion device for the target device selected. The **Device** panel lists appropriate companion devices based on the target device you select.

Figure 3-1. Quartus II Device Settings Page with HardCopy III Device Selected as Companion Device



When you select a HardCopy III companion device, the Quartus II software fits your design to common resources in the I/Os, clock structures, PLLs, memory blocks, and core logic for digital signal processing (DSP).

 For more information about compiling with Stratix III and HardCopy III companion revisions using the Quartus II software, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

HardCopy III and Stratix III Mapping Options

HardCopy III ASICs offer a wide range of family options that can map with various Stratix III FPGAs.

Table 3–1 lists the available HardCopy III and Stratix III companion pairs.

Table 3–1. HardCopy III and Stratix III Companion Devices (Part 1 of 2)

Companion Pair		HardCopy III Packages
HardCopy III ASICs	Stratix III FPGA Prototypes	
HC315WF484N	EP3SL110--F780 (1)	484-pin FineLine BGA - Wire Bond
	EP3SL150--F780 (1)	
	EP3SE110--F780 (1)	
	EP3SL200--H780 (1)	
	EP3SE260--H780 (1)	
HC325WF484N	EP3SL110--F780 (1)	484-pin FineLine BGA - Wire Bond
	EP3SL150--F780 (1)	
	EP3SE110--F780 (1)	
	EP3SL200--H780 (1)	
	EP3SE260--H780 (1)	
	EP3SL340--H1152 (2)	
HC325FF484N	EP3SL110--F780	484-pin FineLine BGA
	EP3SL150--F780	
	EP3SE110--F780	
	EP3SL200--H780	
	EP3SE260--H780	
	EP3SL340--H1152 (2)	
HC325WF780N	EP3SL110--F780	780-pin FineLine BGA - Wire Bond
	EP3SL150--F780	
	EP3SE110--F780	
	EP3SL200--H780	
	EP3SE260--H780	
	EP3SL340--H1152 (2)	
HC325FF780N	EP3SL110--F780	780-pin FineLine BGA
	EP3SL150--F780	
	EP3SE110--F780	
	EP3SL200--H780	
	EP3SE260--H780	
	EP3SL340--H1152	

Table 3-1. HardCopy III and Stratix III Companion Devices (Part 2 of 2)

Companion Pair		HardCopy III Packages
HardCopy III ASICs	Stratix III FPGA Prototypes	
HC335LF1152N	EP3SL150--F1152	1152-pin FineLine BGA
	EP3SE110--F1152	
	EP3SL200--F1152	
	EP3SE260--F1152	
	EP3SL340--H1152	
HC335FF1152N	EP3SL150--F1152	1152-pin FineLine BGA
	EP3SE110--F1152	
	EP3SL200--F1152	
	EP3SE260--F1152	
	EP3SL340--H1152	
HC335LF1517N	EP3SL200--F1517	1517-pin FineLine BGA
	EP3SE260--F1517	
	EP3SL340--F1517	
HC335FF1517N	EP3SL200--F1517	1517-pin FineLine BGA
	EP3SE260--F1517	
	EP3SL340--F1517	

Notes to Table 3-1:

- (1) This mapping is a non-socket replacement path that requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 780-pin FBGA package, while the HardCopy III device is in a 484-pin FBGA package.
- (2) This mapping is a non-socket replacement path that requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 1152-pin FBGA package, while the HardCopy III device is in a 484-pin FBGA package.

When the Quartus II software successfully compiles a design, the HardCopy Device Resource Guide in the Fitter Compilation Report contains information about mapping compatibility to a HardCopy III device. Use this information to select the optimal HardCopy III device for the prototype Stratix III device based on resource and package requirements.

Table 3-2 shows the available resources for prototyping on a Stratix III device when choosing a HardCopy III device.

Table 3-2. HardCopy III ASIC Features (Part 1 of 2)

HardCopy III ASIC	Stratix III FPGA Prototype	ASIC Equivalent Gates (1)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (2)	18 x 18 - Bit Multipliers (FIR Mode)	PLLs
HC315	EP3SL110	2.7 M	275	12	4,203 Kb	288	4
	EP3SL150	3.6 M	355	16	5,499 Kb	384	4
	EP3SE110	5.8 M	360	16	5,544 Kb	896	4
	EP3SL200	5.3 M	360	16	5,544 Kb	576	4
	EP3SE260	6.9 M	360	16	5,544 Kb	768	4

Table 3-2. HardCopy III ASIC Features (Part 2 of 2)

HardCopy III ASIC	Stratix III FPGA Prototype	ASIC Equivalent Gates (1)	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (not including MLABs) (2)	18 x 18 - Bit Multipliers (FIR Mode)	PLLs
HC325	EP3SL110	2.7 M	275	12	4,203 Kb	288	4
	EP3SL150	3.6 M	355	16	5,499 Kb	384	4
	EP3SE110	5.8 M	639	16	8,055 Kb	896	4
	EP3SL200	5.3 M	468	32	8,820 Kb	576	4
	EP3SE260	6.9 M	864	32	12,384 Kb	768	4
	EP3SL340	7.0 M	864	32	12,384 Kb	576	4
HC335	EP3SL150	3.6 M	355	16	5,499 Kb	384	8
	EP3SE110	5.8 M	639	16	8,055 Kb	896	8
	EP3SL200	5.3 M	468	36	9,396 Kb	576	12 (3)
	EP3SE260	6.9 M	864	48	14,688 Kb	768	12 (3)
	EP3SL340	7.0 M	1040	48	16,272 Kb	576	12 (3)

Notes to Table 3-2:

- (1) This is the number of ASIC equivalent gates available in the HardCopy III base array, shared between both adaptive logic module (ALM) logic and DSP functions from a Stratix III FPGA prototype. The number of ASIC equivalent gates usable is bounded by the number of ALMs in the companion Stratix III FPGA device.
- (2) HardCopy III devices do not have dedicated MLABs, but the Stratix III MLAB features and functions are fully supported in HardCopy III devices.
- (3) This device has 12 PLLs in the F1517 package and 8 PLLs in the F1152 package.

HardCopy III ASICs offer pin-to-pin compatibility to the Stratix III prototype, making them drop-in replacements for FPGAs. Due to this compatibility, the same system board and software developed for prototyping and field trials can be retained, enabling faster time-to-market for high-volume production.

HardCopy III devices also offer non-socket replacement mapping for further cost reduction. For example, the EP3SL110 device in the 780-pin FBGA package can be mapped to the HC325 device in the 484-pin FBGA package. Because the pinout for the two packages are not the same, a separate board design is required for the Stratix III device and the HardCopy III device.



For the non-socket replacement path, select I/Os in the Stratix III device that can be mapped to the HardCopy III device. Not all I/Os in the Stratix III device are available in the HardCopy III non-socket replacement device. Check pinout information for both the Stratix III device and the HardCopy III device to ensure that you can map successfully, and select the HardCopy III companion device when designing for the Stratix III device.

Table 3-3 shows available I/O pin counts by package for each Stratix III and HardCopy III companion pair.

Table 3-3. HardCopy III and Stratix III Package and I/O Pin Count Mapping (Part 1 of 2)

HardCopy III ASIC (1)	Stratix III FPGA Prototype	484-Pin FineLine BGA (2)	780-Pin FineLine BGA (2)	1152-Pin FineLine BGA (2)	1517-Pin FineLine BGA (3)	1760-Pin FineLine BGA
HC315W	EP3SL110	296 (4)	—	—	—	—
	EP3SL150	296 (4)	—	—	—	—
	EP3SE110	296 (4)	—	—	—	—
	EP3SL200	296 (5)	—	—	—	—
	EP3SE260	296 (5)	—	—	—	—
HC325W	EP3SL110	296 (4)	392	—	—	—
	EP3SL150	296 (4)	392	—	—	—
	EP3SE110	296 (4)	392	—	—	—
	EP3SL200	296 (5)	392	—	—	—
	EP3SE260	296 (5)	392	—	—	—
	EP3SL340	296 (6)	392 (7)	—	—	—
HC325F	EP3SL110	296 (4)	488	—	—	—
	EP3SL150	296 (4)	488	—	—	—
	EP3SE110	296 (4)	488	—	—	—
	EP3SL200	296 (5)	488	—	—	—
	EP3SE260	296 (5)	488	—	—	—
	EP3SL340	296 (6)	488 (7)	—	—	—
HC335L	EP3SL150	—	—	744	—	—
	EP3SE110	—	—	744	—	—
	EP3SL200	—	—	744	880	—
	EP3SE260	—	—	744	880	—
	EP3SL340	—	—	744	880	—

Table 3-3. HardCopy III and Stratix III Package and I/O Pin Count Mapping (Part 2 of 2)

HardCopy III ASIC (1)	Stratix III FPGA Prototype	484-Pin FineLine BGA (2)	780-Pin FineLine BGA (2)	1152-Pin FineLine BGA (2)	1517-Pin FineLine BGA (3)	1760-Pin FineLine BGA
HC335F	EP3SL150	—	—	744	—	—
	EP3SE110	—	—	744	—	—
	EP3SL200	—	—	744	880	—
	EP3SE260	—	—	744	880	—
	EP3SL340	—	—	744	880	—

Notes to Table 3-3:

- (1) The last letter in the HardCopy III device name refers to the following package types: F—Performance-optimized flip-chip package, L—Cost-optimized flip-chip package, W—Low-cost wirebond package.
- (2) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) that can be used for data inputs.
- (3) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.
- (4) This mapping is a non-socket replacement path and requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 780-Pin FineLine BGA package while the HardCopy III device is in a 484-Pin FineLine BGA package.
- (5) This mapping is a non-socket replacement path and requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 780-Pin Hybrid FineLine BGA package while the HardCopy III device is in a 484-Pin FineLine BGA package.
- (6) This mapping is a non-socket replacement path and requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 1152-Pin Hybrid FineLine BGA package while the HardCopy III device is in a 484-Pin FineLine BGA package.
- (7) This mapping is a non-socket replacement path and requires a different board design for the Stratix III device and the HardCopy III device. The Stratix III device is in a 1152-Pin Hybrid FineLine BGA package while the HardCopy III device is in a 780-Pin FineLine BGA package.

Summary of Differences Between HardCopy III and Stratix III Devices

HardCopy III ASICs are functionally equivalent to Stratix III FPGAs, but they have architectural differences. When implementing your design and laying out your board, consider these differences to ensure successful design mapping from the Stratix III FPGA to the HardCopy III ASIC.


Architecture differences between the Stratix III FPGA and the HardCopy III ASIC include:

- Maximum core voltage is 0.9 V in HardCopy III devices compared with selectable core voltages of 0.9 V or 1.1 V in Stratix III devices.
- Maximum V_{CCIO} power supply of 3.0 V.
- HardCopy III inputs tolerate 3.3 V levels, but you might have to use external clamping diodes on the board to keep the pins operating within specification.
- HardCopy III devices have up to 20 I/O banks and 880 I/O pins, while the largest Stratix III companion devices have up to 24 I/O banks and 976 I/O pins on a 1517-pin FPGA.
- The number of global and regional clocks is identical for Stratix III and HardCopy III devices, but Stratix III devices have up to 116 peripheral clocks, while HardCopy III devices have up to 88. The Quartus II software limits the clock availability on Stratix III and HardCopy III companion pairs to ensure device mapping.

- Configuration is not required for HardCopy III devices; therefore, these Stratix III features are not supported:
 - Programming modes and features such as remote update and .pof encryption.
 - Cyclical redundancy check (CRC) for configuration error detection.
 - 256-bit (AES) volatile and non-volatile security key to protect designs.
 - JTAG instructions used for configuration.
 - FPGA configuration emulation mode.
- Boundary scan (BSCAN) chain length is different and varies with device density.
- Memory Initialization Files (.mif) for embedded memories used as RAM are not supported.
- Stratix III LAB/MLAB and DSP functions are implemented with HCells in HardCopy III devices instead of dedicated blocks.
- Stratix III Programmable Power Technology is not supported in HardCopy III devices. However, HardCopy III ASIC architecture offers performance on par with Stratix III devices with significantly lower power.

Designing with HardCopy III Core Supply Requirements

Altera HardCopy III ASICs are manufactured with a more advanced process technology than Stratix III FPGAs. Each technology is centered on a unique core voltage requirement. HardCopy III nominal core voltage is centered at 0.9 V, whereas Stratix III devices use a typical voltage of 1.1 V. Due to the unique voltage requirements of each device family, design your board's power plane and supply to support both Stratix III and HardCopy III devices to minimize changes required when moving from Stratix III prototyping to HardCopy III devices. A number of power supply regulator manufacturers account for this requirement and require only a few components to be substituted to change the power supply level of the board.

-  For more information about designing power supply methods to account for Stratix III and HardCopy III core supply differences, refer to the *Power Supply and Temperature Sensing Diode in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

Designing with HardCopy III I/Os

HardCopy III ASICs support a wide range of industry I/O standards that match Stratix III supported standards. The exception is that HardCopy III I/O standards support a V_{CCIO} voltage range from 1.2 to 3.0 V. A V_{CCIO} of 3.3 V is not supported by HardCopy III I/O banks. For more information about this topic, refer to “[Mapping HardCopy III and Stratix III I/Os and Modular I/O Banks](#)” on page 3–9.

Aside from the V_{CCIO} requirement, HardCopy III I/O standards support the same specifications as their Stratix III companion equivalent. The I/O arrangement in HardCopy III devices matches the I/O arrangement in Stratix III devices such that I/O pins located on the left and right side I/O banks contain circuits dedicated to high-speed differential I/O interfaces, but have the ability to support external memory devices if required. The top and bottom I/O banks contain dedicated circuitry to optimize external memory interfaces. They also have the ability to support high-speed differential inputs and outputs at lesser speeds than the left and right side banks.



When you select a HardCopy III companion device to compile with your Stratix III target device (and vice versa), the Quartus II software ensures that I/O pins and I/O assignments are compatible with all selected devices.



For more information, refer to the *HardCopy III Device I/O Features* chapter in volume 1 of the *HardCopy III Device Handbook*.

Mapping HardCopy III and Stratix III I/Os and Modular I/O Banks

I/O pins in Stratix III and HardCopy III devices are arranged in groups called modular I/O banks. On Stratix III devices, the number of I/O banks can range from 16 to 24 banks. On HardCopy III devices, the number of I/O banks can range from 12 to 20 banks.

In both Stratix III and HardCopy III devices, the maximum number of I/O banks per side is four or six, depending on the device density. When migrating between devices with a different number of I/O banks per side, the middle or “B” bank is removed or inserted. For example, when moving from a 24-bank Stratix III device to a 16-bank Stratix III or HardCopy III device, the banks that are dropped are “B” banks, namely 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B.

HardCopy III devices do not have banks 1B, 2B, 5B, and 6B. When you design with a Stratix III device that has 24 banks, the Quartus II software limits the available banks common to all devices selected if a HardCopy III device is selected as a companion pair. If you try to assign I/O pins to a non-existent bank in a mapping or companion device, the Quartus II compilation halts with an error.

The following are examples of Quartus II compilation errors:

Error: I/O pins (xx) assigned in I/O bank 1B. The I/O bank does not exist in the selected device

Error: Device migration enabled -- compilation may have failed due to additional constraints when migrating

Error: Can't fit design in device

The sizes of each bank are 24, 26, 32, 40, 42, 48, or 50 I/O pins (including up to two dedicated input pins per bank). During mapping from a smaller device to a larger device, the bank size increases or remains the same but never decreases. For example, banks may increase from a size of 24 I/O to a bank of size 32, 40, 48, or 50 I/O, but will never decrease.

Table 3-4 and **Table 3-5** summarize the number of I/O pins available in each I/O bank for all companion pairs of Stratix III and HardCopy III devices.

Table 3-4. HardCopy III and Stratix III I/O Bank and Count Mapping with Socket Replacement Flow (1)

Bank	780-Pin FineLine BGA (2)		780-Pin FineLine BGA (2)		1152-Pin FineLine BGA (2)		1517-Pin FineLine BGA (3)	
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC (2)	Stratix III FPGA Prototype	HardCopy III ASIC (3)	Stratix III FPGA Prototype
	HC325W	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (4) EP3SE260 (4)	HC325F	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (4) EP3SE260 (4)	HC335	EP3SL150 EP3SE110 EP3SL200 EP3SE260 EP3SL340 (5)	HC335	EP3SL200 EP3SE260 EP3SL340
1A	24	32	32	32	48	48	50	50
1B	—	—	—	—	—	—	—	24
1C	42	26	26	26	42	42	42	42
2A	24	32	32	32	48	48	50	50
2B	—	—	—	—	—	—	—	24
2C	42	26	26	26	42	42	42	42
3A	—	40	40	40	40	40	48	48
3B	—	—	—	—	24	24	48	48
3C	32	24	24	24	32	32	32	32
4A	—	40	40	40	40	40	48	48
4B	—	—	—	—	24	24	48	48
4C	32	24	24	24	32	32	32	32
5A	24	32	32	32	48	48	50	50
5B	—	—	—	—	—	—	—	24
5C	42	26	26	26	42	42	42	42
6A	24	32	32	32	48	48	50	50
6B	—	—	—	—	—	—	—	24
6C	42	26	26	26	42	42	42	42
7A	—	40	40	40	40	40	48	48
7B	—	—	—	—	24	24	48	48
7C	32	24	24	24	32	32	32	32
8A	—	40	40	40	40	40	48	48
8B	—	—	—	—	24	24	48	48
8C	32	24	24	24	32	32	32	32
Total I/O	392	488	488	488	744	744	880	976

Notes to Table 3-4:

- (1) User I/O pin counts are preliminary.
- (2) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) that can be used for data inputs.
- (3) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.
- (4) The EP3SE260 and EP3SL200 FPGAs are offered only in the H780 package.
- (5) The EP3SL340 FPGA is offered only in the H1152 package.

HardCopy III ASICs offer the non-socket replacement flow to reduce design board space and cost. Because HardCopy III and Stratix III device packages are different, some Stratix III device I/Os are not available in the HardCopy III device. [Table 3-5](#) shows the number of I/Os of each bank on Stratix III and HardCopy III devices for the non-socket replacement flow.

Table 3-5. HardCopy III and Stratix III I/O Bank and Count Mapping with Non-Socket Replacement Flow (Note 1) (Part 1 of 2)

Bank	484-pin FineLine BGA	780-Pin FineLine BGA	484-pin FineLine BGA	1152-pin FineLine BGA	780-Pin FineLine BGA	1152-pin FineLine BGA	780-Pin FineLine BGA	1152-pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315W HC325W HC325F	EP3SL110 EP3SL150 EP3SE110 EP3SL200 EP3SE260	HC325W HC325F	EP3SL340	HC325W	EP3SL340	HC325F	EP3SL340
1A	24	32	24	48	24	48	32	48
1B	—	—	—	—	—	—	—	—
1C	26	26	26	42	42	42	26	42
2A	24	32	24	48	24	48	32	48
2B	—	—	—	—	—	—	—	—
2C	26	26	26	42	42	42	26	42
3A	—	40	—	40	—	40	40	40
3B	—	—	—	24	—	24	—	24
3C	24	24	24	32	32	32	24	32
4A	—	40	—	40	—	40	40	40
4B	—	—	—	24	—	24	—	24
4C	24	24	24	32	32	32	24	32
5A	24	32	24	48	24	48	32	48
5B	—	—	—	—	—	—	—	—
5C	26	26	26	42	42	42	26	42
6A	24	32	24	48	24	48	32	48
6B	—	—	—	—	—	—	—	—

Table 3–5. HardCopy III and Stratix III I/O Bank and Count Mapping with Non-Socket Replacement Flow (Note 1) (Part 2 of 2)

Bank	484-pin FineLine BGA	780-Pin FineLine BGA	484-pin FineLine BGA	1152-pin FineLine BGA	780-Pin FineLine BGA	1152-pin FineLine BGA	780-Pin FineLine BGA	1152-pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315W HC325W HC325F	EP3SL110 EP3SL150 EP3SE110 EP3SL200 EP3SE260	HC325W HC325F	EP3SL340	HC325W	EP3SL340	HC325F	EP3SL340
6C	26	26	26	42	42	42	26	42
7A	—	40	—	40	—	40	40	40
7B	—	—	—	24	—	24	—	24
7C	24	24	24	32	32	32	24	32
8A	—	40	—	40	—	40	40	40
8B	—	—	—	24	—	24	—	24
8C	24	24	24	32	32	32	24	32
Total I/O	296	488	296	744	392	744	488	744

Note to Table 3–5:

(1) User I/O pin counts are preliminary.

HardCopy III Supported I/O Standards

HardCopy III ASICs support the same I/O standards as Stratix III FPGAs, except 3.3 V LVTTTL/LVCMOS I/O standards.

Table 3-6 lists I/O standards that HardCopy III devices support.

Table 3-6. HardCopy III I/O Standards and Voltage Levels (Part 1 of 2) (Note 1)

I/O Standard	Standard Support	V _{CCIO} (V)				V _{CCPD} (V) (Pre-Driver Voltage)	V _{REF} (V) (Input Ref Voltage)	V _{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.0-V LVTTTL (1)	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
3.0-V LVCMOS (1)	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVTTTL/LVCMOS	JESD8-5	3.0/2.5	3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVTTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVTTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—
1.2-V LVTTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI (4)	PCI Rev 2.1	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X (4)	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—
SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II (3)	—	(2)	(2)	1.5	N/A	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II (3)	JESD8-6	(2)	(2)	1.5	N/A	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II (3)	JESD8-16A	(2)	(2)	1.2	N/A	2.5	0.6	0.6
Differential SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25
Differential SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25

Table 3-6. HardCopy III I/O Standards and Voltage Levels (Part 2 of 2) (Note 1)

I/O Standard	Standard Support	V _{CCIO} (V)				V _{CCPD} (V) (Pre-Driver Voltage)	V _{REF} (V) (Input Ref Voltage)	V _{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
Differential SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential SSTL-15 Class II (3)	—	(2)	(2)	1.5	N/A	2.5	—	0.75
Differential HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential HSTL-15 Class II	JESD8-6	(2)	(2)	1.5	N/A	2.5	—	0.75
Differential HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	—	0.60
Differential HSTL-12 Class II	JESD8-16A	(2)	(2)	1.2	N/A	2.5	—	0.60
LVDS (6)	ANSI/TIA/EIA-644	(2)	(2)	2.5	2.5	2.5	—	—
RSDS (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—
mini-LVDS (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—
LVPECL	—	(5)	2.5	—	—	2.5	—	—

Note to Table 3-6:

- HardCopy III devices do not support the 3.3-V I/O standard. V_{CCPD} is either 2.5 V or 3.0 V. For a 3.0-V I/O standard, V_{CCPD} = 3.0 V. For 2.5 V and below I/O standards, V_{CCPD} = 2.5 V. However, HardCopy III devices can interface with a 3.3 V interface. Refer to the HardCopy III Device I/O Features chapter in volume 1 of the HardCopy III Device Handbook for more information.
- Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD}. Row I/O banks support both true differential input buffers and true differential output buffers. Column I/O banks support true differential input buffers, but not true differential output buffers. I/O pins are organized in pairs to support differential standards. Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip R_D support.
- Row I/Os do not support HSTL-12 Class II output, HSTL-15 Class II output or SSTL-15 Class II output.
- Column I/O supports PCI/PCI-X with an on-chip clamping diode, and row I/O supports PCI/PCI-X with an external clamping diode.
- Column I/O banks support LVPECL I/O standards only for input clock operation. Differential clock inputs in column I/O use V_{CCCLKIN}.
- Column I/O banks support LVDS outputs using two single-ended output buffers and external one-resistor (LVDS_E_1R) and a three-resistor (LVDS_E_3R) network.
- Row I/O banks support RSDS and mini-LVDS I/O standards using a dedicated LVDS output buffer without a resistor network.
- Column I/O banks support RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

External Memory Interface I/Os in Stratix III and HardCopy III Devices

As with the Stratix III I/O structure, the redesign of the HardCopy III I/O structure provides flexible and high-performance support for existing and emerging external memory standards including DDR3, DDR2, DDR SDRAM, QDRII+, QDRII SRAM, and RLD RAM II.

HardCopy III devices offer the same external memory interface features found in Stratix III devices. These features include delay-locked loops (DLLs), phase-locked loops (PLLs), dynamic on-chip termination (OCT), trace mismatch compensation, read and write leveling, deskew circuitry, half data rate (HDR) blocks, 4- to 36-bit DQ group widths, and DDR external memory support on all sides of the HardCopy III device.

As with Stratix III devices, HardCopy III devices allow a memory interface to be located on any side of the device. The only limitation is if the left and right sides have to be reserved for high-speed I/O applications, as described in the following section.


Table 3-7 shows the number of DQ and DQS buses supported per companion device pair.

Table 3-7. Number of DQS/DQ Groups in HardCopy III Devices per Side (Note 1)

HardCopy III ASIC	Package	Side	x4 (2)	x8/x9	x16/x18	x32/x36
HC315 HC325	484-pin FineLine BGA	Left	0	0	0	0
		Bottom	0	0	0	0
		Right	0	0	0	0
		Top	0	0	0	0
HC325	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0
HC335	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
HC335	1517-pin FineLine BGA	Left	26	12	4	0
		Bottom	38	18	8	4
		Right	26	12	4	0
		Top	38	18	8	4

Notes to Table 3-7:

- (1) These numbers are preliminary.
- (2) Some of the DQS and DQ pins can also be used as R_{UP}/R_{DN} pins. You lose one DQS/DQ group if you use these pins as R_{UP}/R_{DN} pins for OCT calibration. Make sure that the DQS/DQ groups that you have chosen are not also used for OCT calibration.

 For more information about external memory interfaces, refer to the *External Memory Interfaces in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

Mapping Stratix III High-Speed Differential I/O Interfaces with HardCopy III Devices

HardCopy III ASICs have the same dedicated circuitry as Stratix III devices for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (located on left and right sides of the device)

For high-speed differential interfaces, HardCopy III devices support the following differential I/O standards:

- Low-voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- Differential HSTL
- Differential SSTL

HardCopy III ASICs support LVDS on all I/O banks. True LVDS makes use of dedicated LVDS I/O buffers that are optimized for performance. There are true LVDS input and output buffers at the left and right side I/O banks. There are true LVDS input buffers on the top and bottom I/O banks only.

You can configure all I/Os in all banks as emulated LVDS output buffers. Emulated output buffers make use of single-ended buffers and an external resistor network to mimic LVDS operation. Emulated LVDS is useful for low-speed, low-voltage differential applications.

 For more information about high-speed I/O performance, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter in volume 3 of the *HardCopy III Device Handbook*.

All dedicated circuitry for high-speed differential I/O applications are located in the left and right I/O banks of the Stratix III and HardCopy III devices. The top and bottom I/O banks also have support for high-speed receiver applications that do not require the use of the DPA, synchronizer, data realignment, and differential termination. Top and bottom differential I/O buffers have a slower data rate than the high-speed receivers on the left and right I/O banks.

Table 3-8 and Table 3-9 show the LVDS channels supported in HardCopy III and Stratix III companion devices for socket replacement and non-socket replacement flows, respectively.

Table 3-8. LVDS Channels Supported In HardCopy III and Stratix III Companion Devices with Socket Replacement Flow (Part 1 of 2) (Note 1), (2)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC335	EP3SL150 EP3SE110 EP3SL200 EP3SE260 EP3SL340 (4)	HC335	EP3SL200 EP3SE260 EP3SL340
1A	8Rx + 8Tx (5)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
1B	—	—	—	—	—	6Rx + 6Tx
1C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
2A	8Rx + 8Tx (5)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
2B	—	—	—	—	—	6Rx + 6Tx
2C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
3A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
3B (5)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
3C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
4A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
4B (5)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
4C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
5A	8Rx + 8Tx (6)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
5B	—	—	—	—	—	6Rx + 6Tx
5C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
6A	8Rx + 8Tx (6)	8Rx + 8Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx	12Rx + 12Tx
6B	—	—	—	—	—	6Rx + 6Tx

Table 3-8. LVDS Channels Supported In HardCopy III and Stratix III Companion Devices with Socket Replacement Flow (Part 2 of 2) (Note 1), (2)

Bank	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC335	EP3SL150 EP3SE110 EP3SL200 EP3SE260 EP3SL340 (4)	HC335	EP3SL200 EP3SE260 EP3SL340
6C	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx	10Rx + 10Tx
7A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
7B (5)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
7C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx
8A (5)	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	10Rx + 10eTx or 20eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
8B (5)	—	—	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	12Rx + 12eTx or 24eTx	12Rx + 12eTx or 24eTx
8C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx	8Rx + 8eTx or 16eTx

Notes to Table 3-8:

- (1) Channel counts are preliminary.
- (2) Rx = true LVDS input buffers, Tx = true LVDS output buffers and eTx = emulated-LVDS output buffers, either LVDS_E3R or LVDS_E1R.
- (3) The EP3SE260 and EP3SL200 FPGAs are offered only in the H780 package.
- (4) The EP3SL340 FPGA is offered only in the H1152 package.
- (5) Top and bottom I/O banks do not have DPA, synchronizer, data realignment, and differential termination support in Stratix III and HardCopy III devices. Use left and right I/O banks if these features and maximum performance is required.
- (6) When the HardCopy III devices mapped to use 780-pin FineLine BGA Wire Bond package, I/O banks 1A, 2A, 5A, and 6A can support 6 pairs of LVDS channel (6RX + 6Tx) only.

Table 3-9. LVDS Channels Supported In HardCopy III and Stratix III Companion Devices with Non-Socket Replacement Flow (Part 1 of 3) (Note 1), (2)

Bank	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	1152-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC325	EP3SL340 (4)	HC325	EP3SL340 (4)
1A	6Rx	8Rx + 8Tx	6Rx + 6Tx	8Rx + 8Tx	6Rx + 6Tx	12Rx + 12Tx	8Rx + 8Tx	12Rx + 12Tx
1B	—	—	—	—	—	—	—	—
1C	6Rx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	6Rx + 6Tx	10Rx + 10Tx
2A	6Rx	8Rx + 8Tx	6Rx + 6Tx	8Rx + 8Tx	6Rx + 6Tx	12Rx + 12Tx	8Rx + 8Tx	12Rx + 12Tx
2B	—	—	—	—	—	—	—	—
2C	6Rx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	6Rx + 6Tx	10Rx + 10Tx
3A (5)	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	6Rx + 6eTx or 12eTx	10Rx + 10eTx or 20eTx
3B (5)	—	—	—	—	—	6Rx + 6eTx or 12eTx	—	6Rx + 6eTx or 12eTx
3C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx
4A (5)	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	6Rx + 6eTx or 12eTx	10Rx + 10eTx or 20eTx
4B (5)	—	—	—	—	—	6Rx + 6eTx or 12eTx	—	6Rx + 6eTx or 12eTx
4C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx

Table 3-9. LVDS Channels Supported In HardCopy III and Stratix III Companion Devices with Non-Socket Replacement Flow (Part 2 of 3) (Note 1), (2)

Bank	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	1152-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC325	EP3SL340 (4)	HC325	EP3SL340 (4)
5A	6Rx	8Rx + 8Tx	6Rx + 6Tx	8Rx + 8Tx	6Rx + 6Tx	12Rx + 12Tx	8Rx + 8Tx	12Rx + 12Tx
5B	—	—	—	—	—	—	—	—
5C	6Rx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	6Rx + 6Tx	10Rx + 10Tx
6A	6Rx	8Rx + 8Tx	6Rx + 6Tx	8Rx + 8Tx	6Rx + 6Tx	12Rx + 12Tx	8Rx + 8Tx	12Rx + 12Tx
6B	—	—	—	—	—	—	—	—
6C	6Rx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	6Rx + 6Tx	10Rx + 10Tx	6Rx + 6Tx	10Rx + 10Tx
7A (5)	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	6Rx + 6eTx or 12eTx	10Rx + 10eTx or 20eTx
7B (5)	—	—	—	—	—	6Rx + 6eTx or 12eTx	—	6Rx + 6eTx or 12eTx
7C (5)	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx	6Rx + 6eTx or 12eTx	8Rx + 8eTx or 16eTx
8A (5)	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	—	10Rx + 10eTx or 20eTx	6Rx + 6eTx or 12eTx	10Rx + 10eTx or 20eTx
8B (5)	—	—	—	—	—	6Rx + 6eTx or 12eTx	—	6Rx + 6eTx or 12eTx

Table 3–9. LVDS Channels Supported In HardCopy III and Stratix III Companion Devices with Non-Socket Replacement Flow (Part 3 of 3) (Note 1), (2)

Bank	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	1152-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3)) EP3SE260 (3))	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (3) EP3SE260 (3)	HC325	EP3SL340 (4)	HC325	EP3SL340 (4)
8C (5)	6Rx	6Rx	6Rx	6Rx	6Rx	8Rx	6Rx	8Rx

Notes to Table 3–9:

- (1) Channel counts are preliminary.
- (2) Rx = true LVDS input buffers, Tx = true LVDS output buffers and eTx = emulated-LVDS output buffers, either LVDS_E3R or LVDS_E1R.
- (3) The EP3SE260 and EP3SL200 FPGAs are offered only in the H780 package.
- (4) The EP3SL340 FPGA is offered only in the H1152 package.
- (5) Top and bottom I/O banks do not have DPA, synchronizer, data realignment, and differential termination support in Stratix III and HardCopy III devices. Use left and right I/O banks if these features and maximum performance is required.

HardCopy III PLL Planning and Utilization

HardCopy III devices offer up to 12 PLLs that support the same features as Stratix III PLLs. The same nomenclature is used for HardCopy III and Stratix III PLLs that follow their geographical location in the device floorplan. The PLLs that reside on the top and bottom sides of the device are named PLL_T1, PLL_T2, PLL_B1, and PLL_B2; the PLLs that reside on the left and right sides of the device are named PLL_L1, PLL_L2, PLL_L3, PLL_L4, PLL_R1, PLL_R2, PLL_R3, and PLL_R4, respectively. Table 3–10 lists the number of PLLs available in HardCopy III devices and their companion Stratix III devices for the socket replacement flow.

Table 3–10. HardCopy III and Stratix III PLL Mapping Options for Socket Replacement Flow (Part 1 of 2) (Note 1)

PLL	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (2) EP3SE260 (2)	HC335	EP3SL150 EP3SE110 EP3SL200 EP3SE260 EP3SL340 (3)	HC335	EP3SL200 EP3SE260 EP3SL340
PLL_L1	—	—	—	—	✓	✓
PLL_L2	✓	✓	✓	✓	✓	✓
PLL_L3	—	—	✓	✓	✓	✓

Table 3-10. HardCopy III and Stratix III PLL Mapping Options for Socket Replacement Flow (Part 2 of 2) (Note 1)

PLL	780-Pin FineLine BGA		1152-Pin FineLine BGA		1517-Pin FineLine BGA	
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 ⁽²⁾ EP3SE260 ⁽²⁾	HC335	EP3SL150 EP3SE110 EP3SL200 EP3SE260 EP3SL340 ⁽³⁾	HC335	EP3SL200 EP3SE260 EP3SL340
PLL_L4	—	—	—	—	✓	✓
PLL_T1	✓	✓	✓	✓	✓	✓
PLL_T2	—	—	✓	✓	✓	✓
PLL_B1	✓	✓	✓	✓	✓	✓
PLL_B2	—	—	✓	✓	✓	✓
PLL_R1	—	—	—	—	✓	✓
PLL_R2	✓	✓	✓	✓	✓	✓
PLL_R3	—	—	✓	✓	✓	✓
PLL_R4	—	—	—	—	✓	✓

Notes to Table 3-10:

- (1) The PLL availability table is preliminary. It is best to design with the Quartus II software to check if your design can use all available PLLs.
- (2) The EP3SE260 and EP3SL200 FPGAs are offered only in the H780 package.
- (3) The EP3SL340 FPGA is offered only in the H1152 package.

Table 3-11 lists the number of PLLs available in HardCopy III devices and their companion Stratix III devices for the non-socket replacement flow.

Table 3-11. HardCopy III and Stratix III PLL Mapping Options for Non-Socket Replacement Flow (Part 1 of 2) (Note 1)

PLL	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	1152-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315 HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 ⁽²⁾ EP3SE260 ⁽²⁾	HC325	EP3SL340 ⁽³⁾	HC325	EP3SL340 ⁽³⁾
PLL_L1	—	—	—	—	—	—
PLL_L2	✓	✓	✓	✓	✓	✓
PLL_L3	—	—	—	✓	—	✓
PLL_L4	—	—	—	—	—	—
PLL_T1	✓	✓	✓	✓	✓	✓
PLL_T2	—	—	—	✓	—	✓
PLL_B1	✓	✓	✓	✓	✓	✓
PLL_B2	—	—	—	✓	—	✓
PLL_R1	—	—	—	—	—	—

Table 3-11. HardCopy III and Stratix III PLL Mapping Options for Non-Socket Replacement Flow (Part 2 of 2) (Note 1)

PLL	484-Pin FineLine BGA	780-Pin FineLine BGA	484-Pin FineLine BGA	1152-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA
	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype	HardCopy III ASIC	Stratix III FPGA Prototype
	HC315 HC325	EP3SL110 EP3SL150 EP3SE110 EP3SL200 (2) EP3SE260 (2)	HC325	EP3SL340 (3)	HC325	EP3SL340 (3)
PLL_R2	✓	✓	✓	✓	✓	✓
PLL_R3	—	—	—	✓	—	✓
PLL_R4	—	—	—	—	—	—

Notes to Table 3-11:


- (1) The PLL availability table is preliminary. It is best to design with the Quartus II software to check if your design can use all available PLLs.
- (2) The EP3SL200 and EP3SE260 FPGAs are offered only in the H780 package.
- (3) The EP3SL340 FPGA is offered only in the H1152 package.

 For more information about HardCopy III PLLs, refer to the *Clock Networks and PLLs in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

HardCopy III Memory Blocks

TriMatrix memory in HardCopy III devices supports the same memory functions and features as Stratix III devices. You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register using the MegaWizard™ Plug-In Manager in the Quartus II software.

HardCopy III embedded memory consists of MLAB, M9K, and M144K memory blocks, and has one-to-one mapping from Stratix III memory. However, the number of available memory blocks differs based on physical density, package, and Stratix III device to HardCopy III ASIC mapping paths. The Quartus II software may not allow all available Stratix III memory types to fit into a selected HardCopy III device if your design has a very high resource utilization and performance target.

 Altera recommends that you compile your design with the Quartus II software and verify the device resource guide to check for available resources in the HardCopy III device.

 For information about using the HardCopy Device Resource Guide, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

Functionally, memory in HardCopy III and Stratix III devices is identical. Memory blocks can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO.



When using the memory blocks in ROM, single-port, simple dual-port, or true dual-port mode, you can corrupt the memory contents if you violate the setup or hold-time on any of the memory block input registers. This applies to both read and write operations.

MLAB Implementation

In Stratix III devices, MLABs are dedicated blocks and can be configured for regular logic functions or memory functions. In HardCopy III devices, MLAB memory blocks are implemented using HCells. The Quartus II software maps the Stratix III MLAB function to the appropriate memory HCell macro that preserves memory function. This allows you to use the HardCopy III core fabric more efficiently, freeing up unused HCells for ALM or DSP functions.

MLAB, M9K, and M144K Utilization

HardCopy III MLAB, M9K, and M144K block functionality is similar to Stratix III memory blocks; however, you cannot pre-load HardCopy III MLAB, M9K, and M144K blocks with a .mif file when using them as RAM. Ensure that your Stratix III design does not require .mif files if the memory blocks are used as RAM. However, if memory blocks are used as ROM, they are mask-programmed to the design's ROM contents.



You can use the ALTMEM_INIT megafunction to initialize a RAM block after power-up for Stratix III and HardCopy III devices. This megafunction reads from a ROM defined with the megafunction and writes to the RAM after power-up. This function allows you to have initialized contents on a RAM block. Refer to the Quartus II Help for implementation information about this function.

Unlike Stratix III FPGAs, HardCopy III MLAB, M9K, and M144K RAM contents are unknown after power-up. However, like Stratix III devices, all HardCopy III memory output registers power-up cleared, if used. When designing HardCopy III memory blocks as RAM, Altera recommends a write-before-read of the memory block to avoid reading unknown initial power-up data conditions. If the HardCopy III memory block is designated as ROM, it powers up with the ROM contents.

One advantage over Stratix III RAM blocks is that unused M9K and M144K blocks are disconnected from the power rails and MLABs are only implemented as required by your design. These unused resources do not contribute to overall power consumption on HardCopy III devices.



For a list of supported features in HardCopy III memory blocks, refer to the *TriMatrix Embedded Memory Blocks in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

Using JTAG Features in HardCopy III Devices

HardCopy III ASICs support the same boundary-scan test (BST) functionality as Stratix III FPGAs. However, no reconfiguration is possible because HardCopy III devices are mask-programmed. Therefore, HardCopy III devices do not support instructions to reconfigure the device through the JTAG pins. HardCopy III boundary scan lengths also differ from Stratix III devices.

 For information about HardCopy III JTAG functionality and support, refer to the *IEEE 1149.1 JTAG Boundary Scan Testing in HardCopy III Devices* chapter in volume 1 of the *HardCopy III Device Handbook*.

Power-Up and Configuration Pin Compatibility with Stratix III Devices

When designing a board for both HardCopy III and Stratix III devices, most configuration pins required by the Stratix III device are not required by the HardCopy III device. The functions of these Stratix III configuration pins are not carried over to the HardCopy III companion device because HardCopy III devices are not programmable. To simplify the board connection for these configuration pins, Altera recommends minimizing the power-up and configuration pins that do not carry over from a Stratix III device to a HardCopy III device. You should ensure that the board can be used for both Stratix III and HardCopy III devices. Configuration pins for both devices must be properly connected. Otherwise, separate boards are required for the two devices.

Table 3-12 lists the main and optional functions on the configuration pins used by Stratix III and HardCopy III devices.

Table 3-12. Mapping Configuration Pins into HardCopy III Devices (Part 1 of 2) (Note 1), (2), (3), (4)

Stratix III FPGA Prototype		HardCopy III ASIC		Board Connection
Main Function	Optional Function	Main Function	Optional Function	
MSEL [2..0]	—	—	—	Not required and no connection on board.
nCONFIG (5)	—	nCONFIG	—	Required connection.
I/O pin	DATA0	I/O pin	DATA0	DATA[0] retains both user I/O and optional EPCS access functions. DATA [7..1] retains user I/O functions only.
I/O pin	DATA [7..1]	I/O pin	—	
DCLK	—	DCLK	—	No Connection on Board, except when EPCS access is required in user mode.
I/O pin	INIT_DONE (6)	I/O pin	INIT_DONE	Retains the same I/O functions from Stratix III.
I/O pin	CLKUSR	I/O pin	—	Retains the same I/O functions from Stratix III except CLKUSR, because no device programming is required.
nSTATUS (5)	—	nSTATUS	—	Required connection.
CONF_DONE (5)	—	CONF_DONE	—	Required connection.
nCE	—	nCE	—	Required connection.
nCEO	—	nCEO	—	Not required and no connection on board.
PORSEL	—	PORSEL	—	Required connection.
I/O pin	ASDO	I/O pin	ASDO	No connection on board, except when EPCS access is required in user mode.
I/O pin	nCSO	I/O pin	nCSO	No connection on board, except when EPCS access is required in user mode.
nIO_PULLUP	—	nIO_PULLUP	—	Required connection.
I/O pin	CRC_ERROR (4)	I/O pin	—	Retains the same I/O functions from Stratix III, but not CRC_ERROR, because no device programming is required.

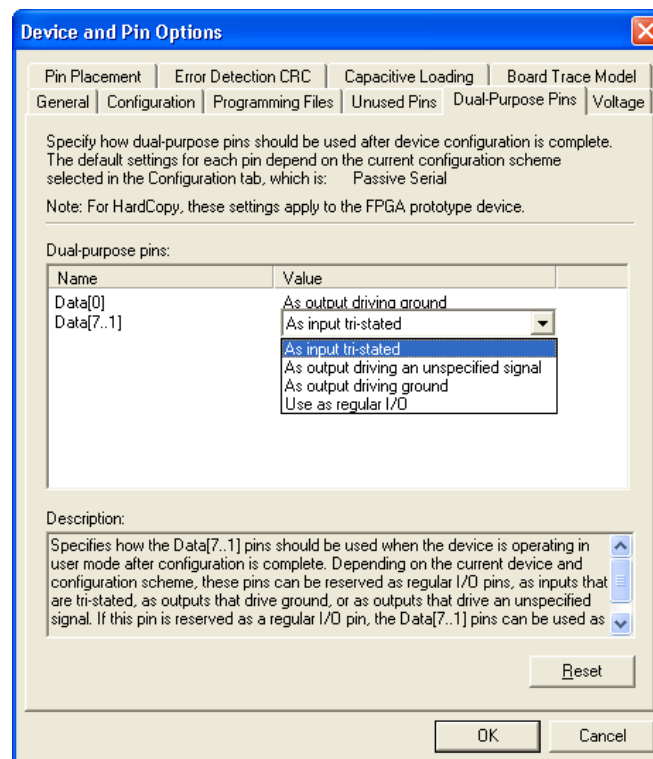
Table 3-12. Mapping Configuration Pins into HardCopy III Devices (Part 2 of 2) (Note 1), (2), (3), (4)

Stratix III FPGA Prototype		HardCopy III ASIC		Board Connection
Main Function	Optional Function	Main Function	Optional Function	
I/O pin	DEV_CLRn	I/O pin	DEV_CLRn	Retains the same I/O functions from Stratix III.
I/O pin	DEV_OE	I/O pin	DEV_OE	Retains the same I/O functions from Stratix III.

Notes to Table 3-12:

- (1) For correct operation of a HardCopy III device, pull the `nSTATUS`, `nCONFIG`, and `CONF_DONE` pins to V_{CCPGM} . In HardCopy III devices, these pins are designed with weak internal resistors pulled up to V_{CCPGM} . Stratix III configuration schemes require pull-up resistors on these I/O pins, so they may already be present on the board. You can remove these external pull-up resistors, if doing so does not affect other FPGAs on the board.
- (2) HardCopy III devices have a maximum V_{CCIO} voltage of 3.0 V, but the input I/O pin can tolerate a 3.3 V level. This applies to V_{CCPGM} voltage and all dedicated and dual-purpose pins.
- (3) For HardCopy III devices, there is weak pull-up on the `nSTATUS`, `CONF_DONE`, `nCONFIG`, and `DCLK` pins. Therefore, these pins can be left floating or remain connected to external pull-up resistors. If the EPCS is used in user mode as a boot-up RAM or data access for a Nios® II processor, `DCLK`, `DATA[0]`, `ASDO`, and `nCSO` must be connected to the EPCS device.
- (4) In HardCopy III devices, `CRC_ERROR` is hard-wired to logic 0 if the CRC feature is enabled in Stratix III devices.
- (5) The `PORSEL` pin setting delays the POR sequence for both HardCopy III and Stratix III devices.
- (6) The `INIT_DONE` settings option is mask-programmed into the device. You must submit these settings to Altera with the final design prior to mapping to a HardCopy III device. The use of the `INIT_DONE` option and other dual-purpose pins (for example, `DEV_CLRn` device-wide reset and `DEV_OE` device-wide output enable) are available in the **Fitter Device Options** section of the Quartus II report file.

For both the Stratix III and HardCopy III devices, the Quartus II software allows you to set the I/O pins listed in Table 3-12 as dual-purpose pins (as shown in Figure 3-2). As dual-purpose pins, they have I/O functionality when the device enters user mode (when `INIT_DONE` is asserted).

Figure 3-2. Device and Pin Options Dialog Box

If these dual-purpose pins are required to configure the Stratix III device, but will be unused after configuration, these pins remain unused on the HardCopy III device. It is important to consider the state of these pins after power-up and when the device is in user mode. For example, when replacing the Stratix III device with a HardCopy III device, these pins may be left floating when the configuration device is removed if you assign such pins as inputs. In this case, you will either require an external means to drive them to a stable level, or set the pins to output driving ground.

Revision History

Table 3-13 shows the revision history for this document.

Table 3-13. Document Revision History

Date	Version	Changes
January 2011	3.2	Minor text edits.
January 2010	3.1	<ul style="list-style-type: none"> ■ Updated Table 3-20, Table 3-21, and Table 3-29.
June 2009	3.0	<ul style="list-style-type: none"> ■ Updated the following tables: Table 3-1, Table 3-4, Table 3-7, Table 3-10, Table 3-6, Table 3-16, Table 3-18, Table 3-10, and Table 3-12 ■ Added the following tables: Table 3-11, Table 3-19, Table 3-11 ■ Updated Figure 3-1 ■ Updated “HardCopy III and Stratix III Mapping Options” on page 3-3 ■ Updated “Mapping HardCopy III and Stratix III I/Os and Modular I/O Banks” on page 3-9 ■ Removed “Referenced Documents” ■ This chapter was listed as p/n 52003 in document release version 2.0
December 2008	2.0	Minor text edits.
May 2008	1.0	Initial release.

