

This chapter provides guidelines for you to improve your system's signal integrity and layout guidelines to successfully implement an RLDRAM II interface in your system.

The RLDRAM II Controller with UniPHY intellectual property (IP) enables you to implement Common I/O (CIO) RLDRAM II interfaces with Arria® V, Stratix® III, Stratix IV, and Stratix V devices. You can implement Separate I/O (SIO) RLDRAM II interfaces with the ALTDQ_DQS or ALTDQ_DQS2 megafunctions.


This chapter focuses on the following key factors that affect signal integrity:

- I/O standards
- RLDRAM II configurations
- Signal terminations
- Printed circuit board (PCB) layout guidelines

I/O Standards

RLDRAM II interface signals use one of the following JEDEC I/O signalling standards:

- HSTL-15—provides the advantages of lower power and lower emissions.
- HSTL-18—provides increased noise immunity with slightly greater output voltage swings.

 To select the most appropriate standard for your interface, refer to the *Device Datasheet for Arria II Devices* chapter in the *Arria II Device Handbook*, the *Device Datasheet for Arria V Devices* chapter in the *Arria V Device Handbook*, the *Stratix III Device Datasheet: DC and Switching Characteristics* chapter in the *Stratix III Device Handbook*, the *DC and Switching Characteristics for Stratix IV Devices* chapter in the *Stratix IV Device Handbook*, or the *DC and Switching Characteristics for Stratix V Devices* chapter in the *Stratix V Device Handbook*.

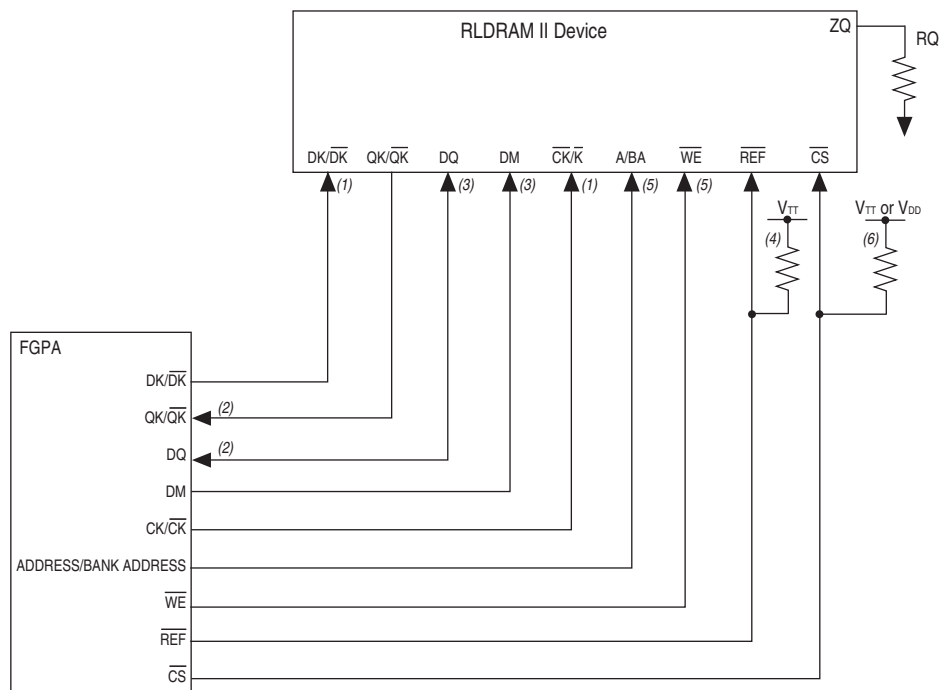
The RLDRAM II Controller with UniPHY IP defaults to HSTL 1.8 V Class I outputs and HSTL 1.8 V inputs.

RLDRAM II Configurations

The RLD RAM II Controller with UniPHY IP supports interfaces for CIO RLD RAM II with a single device, and two devices in a width expansion configuration up to maximum width of 72 bits. This chapter focuses on the layout and guidelines for CIO RLD RAM II interfaces. However, the termination and layout principles for SIO RLD RAM II interfaces are similar to CIO RLD RAM II, except that SIO RLD RAM II interfaces have unidirectional data buses.

Figure 6-1 shows the main signal connections between the FPGA and a single CIO RLD RAM II component.

Figure 6-1. Configuration with a Single CIO RLD RAM II Component

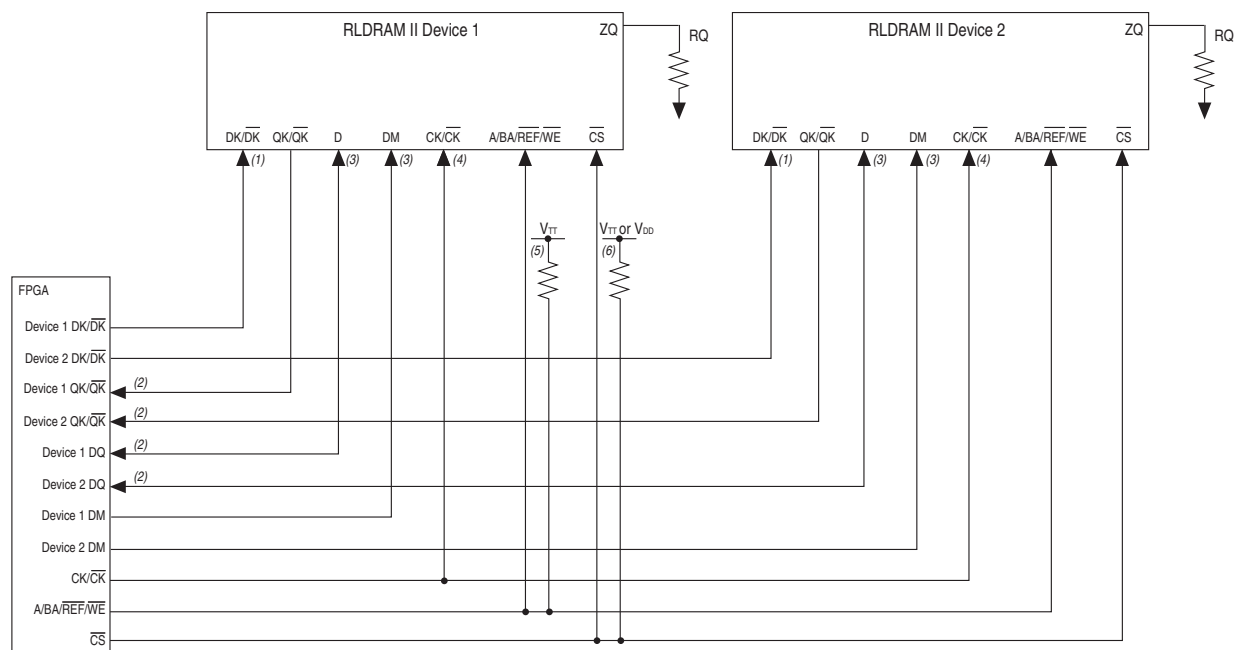


Notes to Figure 6-1:

- (1) Use external differential termination on DK/DK# and CK/CK#.
- (2) Use FPGA parallel on-chip termination (OCT) for terminating QK/QK# and DQ on reads.
- (3) Use RLD RAM II component on-die termination (ODT) for terminating DQ and DM on writes.
- (4) Use external discrete termination with fly-by placement to avoid stubs.
- (5) Use external discrete termination for this signal, as shown for REF.
- (6) Use external discrete termination, as shown for REF, but you may require a pull-up resistor to V_{DD} as an alternative option. Refer to the RLD RAM II device data sheet for more information about RLD RAM II power-up sequencing.

Figure 6–2 shows the main signal connections between the FPGA and two CIO RLD RAM II components in a width expansion configuration.

Figure 6–2. Configuration with Two CIO RLD RAM II Components in a Width Expansion Configuration



Notes to Figure 6–2:

- (1) Use external differential termination on DK/DK#.
- (2) Use FPGA parallel OCT for terminating QK/QK# and DQ on reads.
- (3) Use RLD RAM II component ODT for terminating DQ and DM on writes.
- (4) Use external dual 200 Ω differential termination.
- (5) Use external discrete termination at the trace split of the balanced T or Y topology.
- (6) Use external discrete termination at the trace split of the balanced T or Y topology, but you may require a pull-up resistor to V_{DD} as an alternative option. Refer to the RLD RAM II device data sheet for more information about RLD RAM II power-up sequencing.

Signal Terminations

Stratix III, Stratix IV, and Stratix V devices offer OCT technology.

Table 6–1 lists the extent of OCT support for each device.

Table 6–1. On-Chip Termination Schemes (Part 1 of 2)

| Termination Scheme | HSTL-15 and HSTL-18 | FPGA Device | |
|--|---------------------|--|-----------------------|
| | | Arria II GZ, Stratix III, and Stratix IV | Arria V and Stratix V |
| | | Row/Column I/O | Row/Column I/O |
| On-Chip Series Termination without Calibration | Class I | 50 | 50 |
| On-Chip Series Termination with Calibration | Class I | 50 | 50 ⁽¹⁾ |

Table 6-1. On-Chip Termination Schemes (Part 2 of 2)

| Termination Scheme | HSTL-15 and HSTL-18 | FPGA Device | |
|---|---------------------|--|-----------------------|
| | | Arria II GZ, Stratix III, and Stratix IV | Arria V and Stratix V |
| | | Row/Column I/O | Row/Column I/O |
| On-Chip Parallel Termination with Calibration | Class I | 50 | 50 ⁽¹⁾ |

Note to Table 6-1:

- (1) Although 50 Ω is the recommended option, Stratix V devices offer a wider range of calibrated termination impedances.

On-chip series (R_S) termination supports output buffers, and bidirectional buffers only when they are driving output signals. On-chip parallel (R_T) termination supports input buffers, and bidirectional buffers only when they are input signals. RLDRAM II CIO interfaces have bidirectional data paths. The UniPHY IP uses dynamic OCT on the datapath, which switches between series OCT for memory writes and parallel OCT for memory reads.

For Arria II GZ, Stratix III, and Stratix IV devices, the HSTL Class I I/O calibrated terminations are calibrated against 50 Ω 1% resistors connected to the R_{UP} and R_{DN} pins in an I/O bank with the same V_{CCIO} as the RLDRAM II interface. For Arria V and Stratix V devices, the HSTL Class I I/O calibrated terminations are calibrated against 100 Ω 1% resistors connected to the R_{ZQ} pins in an I/O bank with the same V_{CCIO} as the RLDRAM II interface.

The calibration occurs at the end of the device configuration.

RLDRAM II memory components have a ZQ pin which connects through a resistor R_Q to ground. Typically the RLDRAM II output signal impedance is $0.2 \times R_Q$. Refer to the RLDRAM II device data sheet for more information.



For information about OCT, refer to the *I/O Features in Arria II Devices* chapter in the *Arria II Device Handbook*, *I/O Features in Arria V Devices* chapter in the *Arria V Device Handbook*, *Stratix III Device I/O Features* chapter in the *Stratix III Device Handbook*, the *I/O Features in Stratix IV Devices* chapter in the *Stratix IV Device Handbook*, or the *I/O Features in Stratix V Devices* chapter in the *Stratix V Device Handbook*.

The following section shows HyperLynx simulation eye diagrams to demonstrate signal termination options. Altera strongly recommends signal terminations to optimize signal integrity and timing margins, and to minimize unwanted emissions, reflections, and crosstalk.

All of the eye diagrams shown in this section are for a 50 Ω trace with a propagation delay of 600 ps which is approximately a 3.3-inch trace on a standard FR4 PCB. The signal I/O standard is HSTL-18.

The eye diagrams shown in this section show the best case achievable and do not take into account PCB vias, crosstalk and other degrading effects such as variations in the PCB structure due to manufacturing tolerances.



Simulate your design to ensure correct functionality.

Outputs from the FPGA to the RLD RAM II Component

The following output signals are from the FPGA to the RLD RAM II component:

- write data (DQ on the bidirectional data signals for CIO RLD RAM II)
- data mask (DM)
- address, bank address
- command (CS, WE, and REF)
- clocks (CK/CK# and DK/DK#)

For point-to-point single-ended signals requiring external termination, Altera recommends that you place a fly-by termination by terminating at the end of the transmission line after the receiver to avoid unterminated stubs. The guideline is to place the fly-by termination within 100 ps propagation delay of the receiver.

Although not recommended, you can place the termination before the receiver, which leaves an unterminated stub. The stub delay is critical because the stub between the termination and the receiver is effectively unterminated, causing additional ringing and reflections. Stub delays should be less than 50 ps.

Altera recommends that the differential clocks, CK, CK# and DK, DK#, use a differential termination at the end of the trace of the RLD RAM II component. Alternatively, you can terminate each clock output with a parallel termination to V_{TT} .

The HyperLynx simulation eye diagrams show simulation cases of write data, address, and chip-select signals with termination options. All eye diagrams are shown at the connection to the receiver device die.

Figure 6-3 shows the double data rate write data using a Stratix IV Class I HSTL-18 with calibrated $50\ \Omega$ OCT output driver and the nominal RLD RAM II ODT of $150\ \Omega$

Figure 6-3. Write Data Simulation at 400 MHz with RLD RAM II ODT

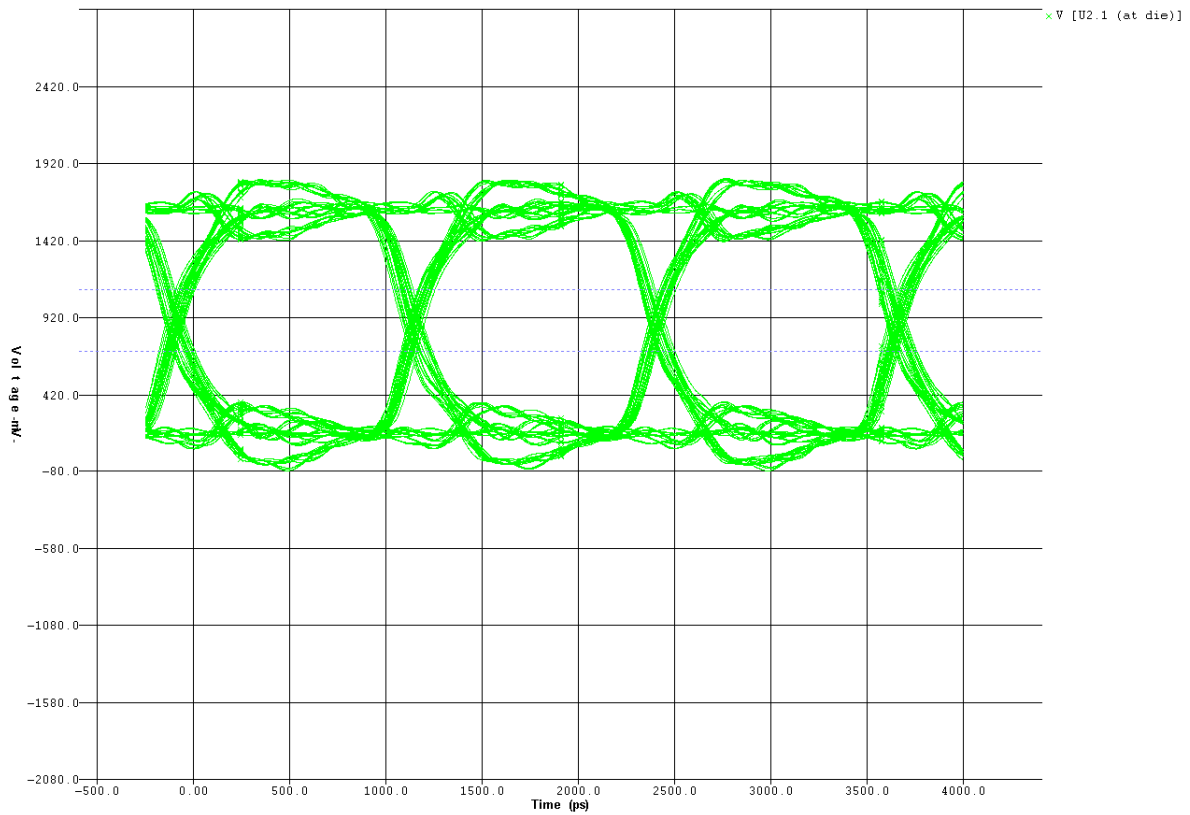


Figure 6-4 shows an address signal at a frequency of 200 MHz using Stratix IV Class I HSTL-18 with a calibrated 50 Ω OCT driver and a 100 ps fly-by 50 Ω parallel termination to V_{TT} .

Figure 6-4. Address Simulation Using Stratix IV Class I HSTL-18 50 Ω Calibration Driver and Fly-by 50 Ω Parallel Termination

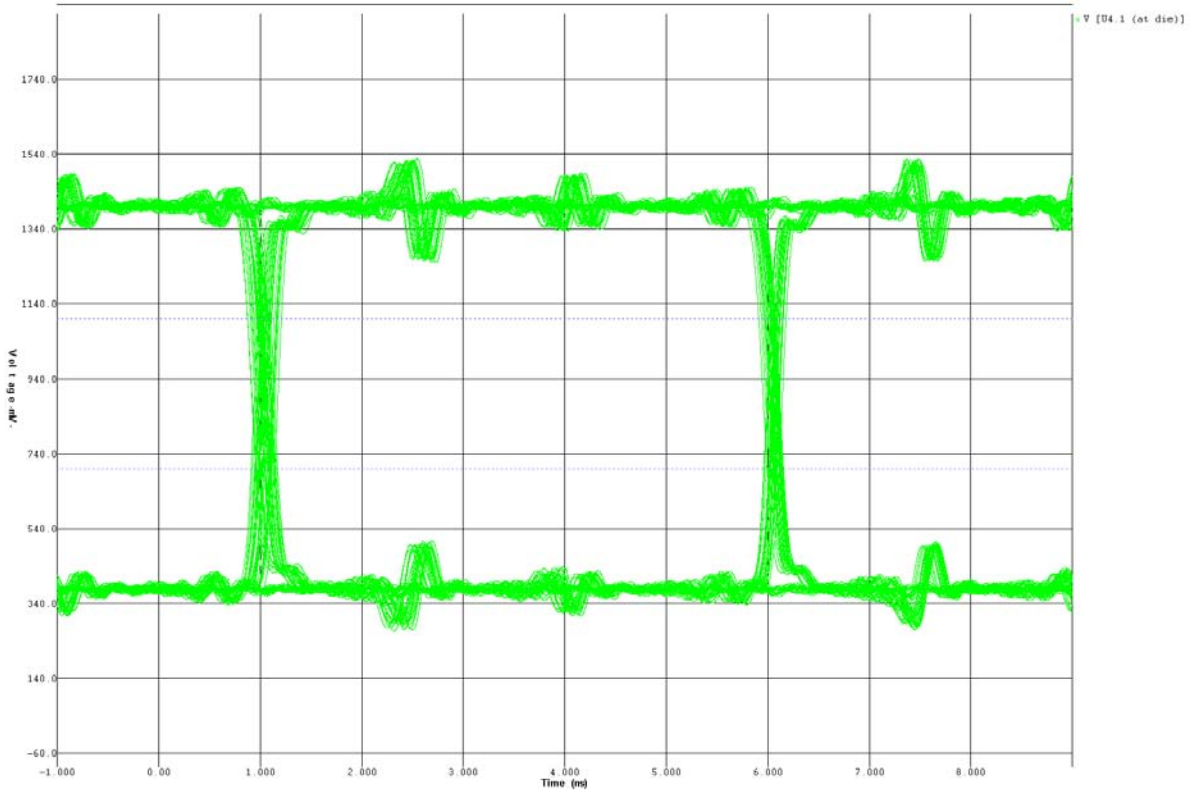


Figure 6-5 shows an address signal at a frequency of 200 MHz using Stratix IV Class I HSTL-18 12 mA driver and a 50 ps stub 50 Ω parallel termination to V_{TT} .

Figure 6-5. Address Simulation Using Stratix IV Class I HSTL-18 50 Ω Calibration Driver and Stub 50 Ω Parallel Termination to V_{TT}

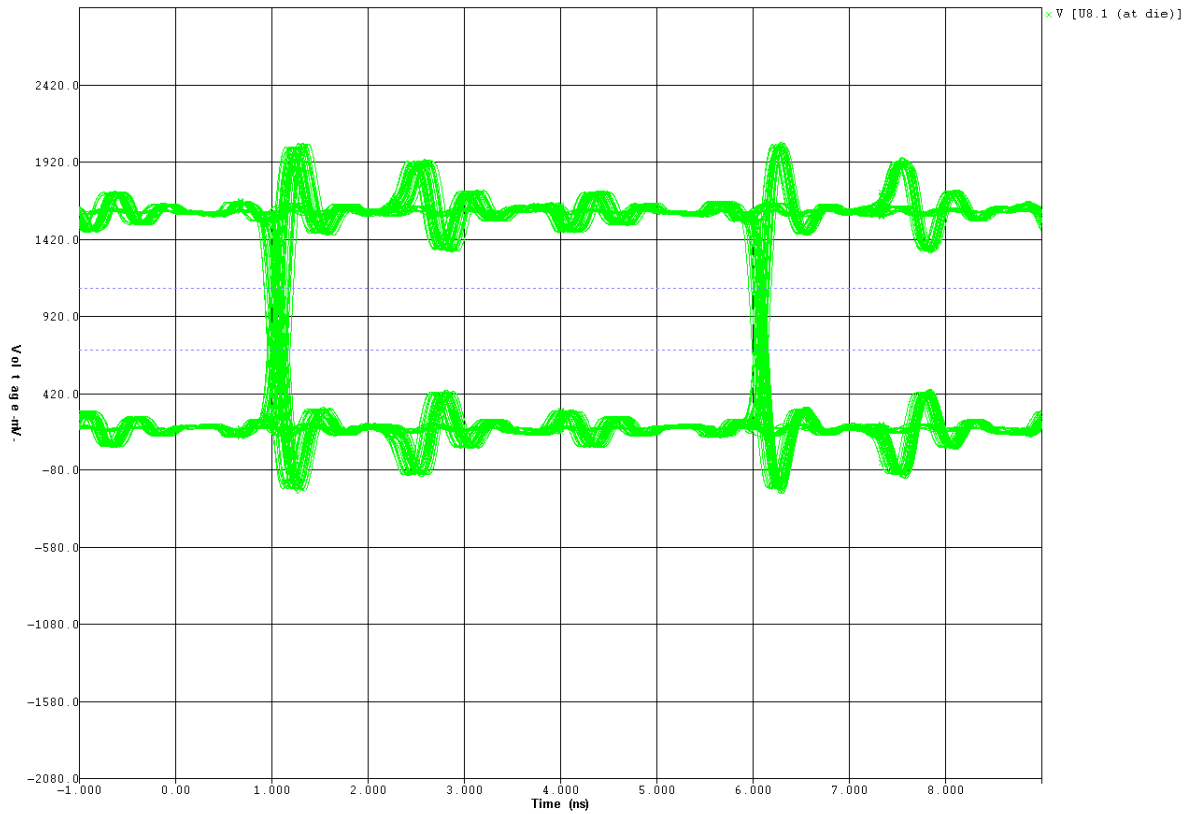
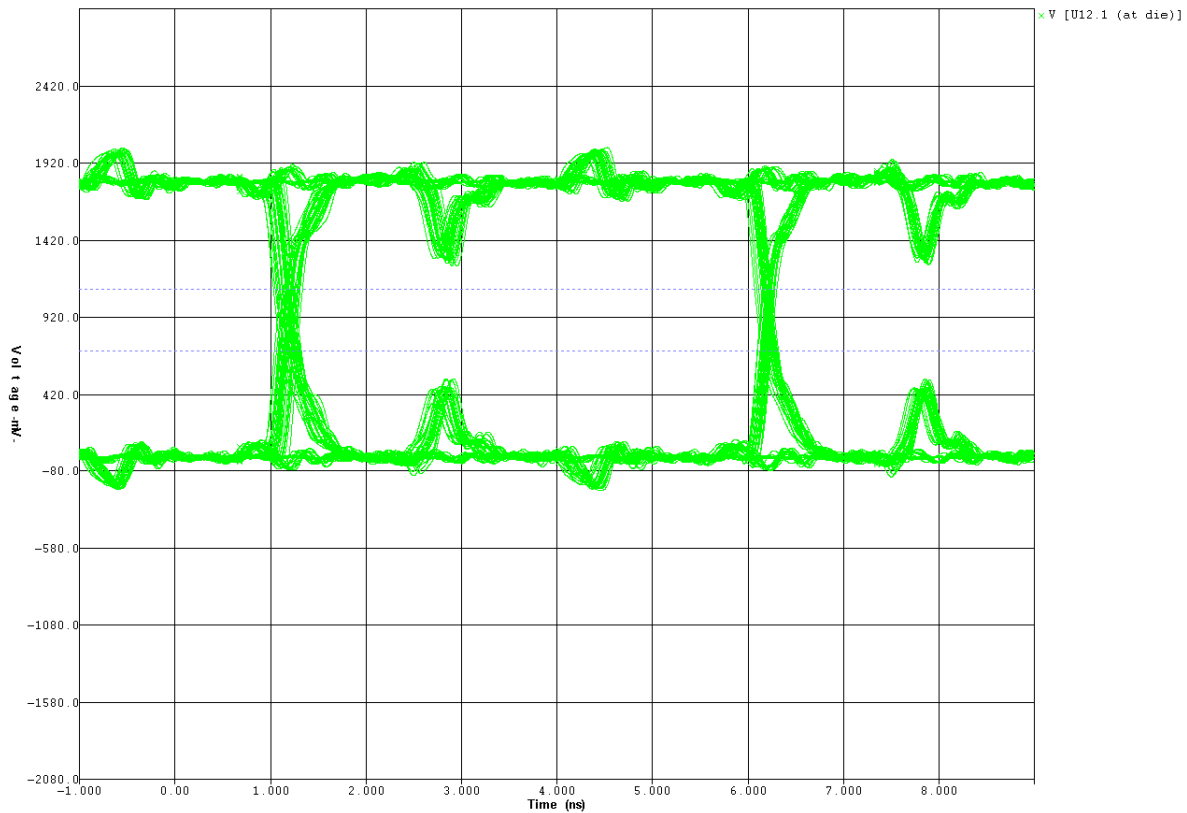


Figure 6-6 shows the chip-select signal at a frequency of 200 MHz using Stratix IV Class I HSTL-18 with a calibrated 50 Ω driver and a 10 K pull-up resistor to V_{DD} . The RLD RAM II power sequencing may require the chip selects to have a pull-up resistor. Refer to the RLD RAM II data sheet for further details.

Figure 6-6. Chip-Select Simulation Using Stratix IV Class I HSTL-18 50 Ω Calibration Driver and 10 K Pull-up Resistor to V_{DD}



For the RLD RAM II width expansion configuration for address and command, use the same principles recommended for “QDR II SRAM Board Design Guidelines” on page 7-1.

For external parallel termination recommended for a balanced T topology, refer to Figure 7-3 on page 7-4, and for HyperLynx simulation diagrams of the width expansion topology for address and command signals, refer to Figure 7-8 through Figure 7-11 on page 7-13.

Input to the FPGA from the RLD RAM II Component

The RLD RAM II component drives the following input signals into the FPGA:

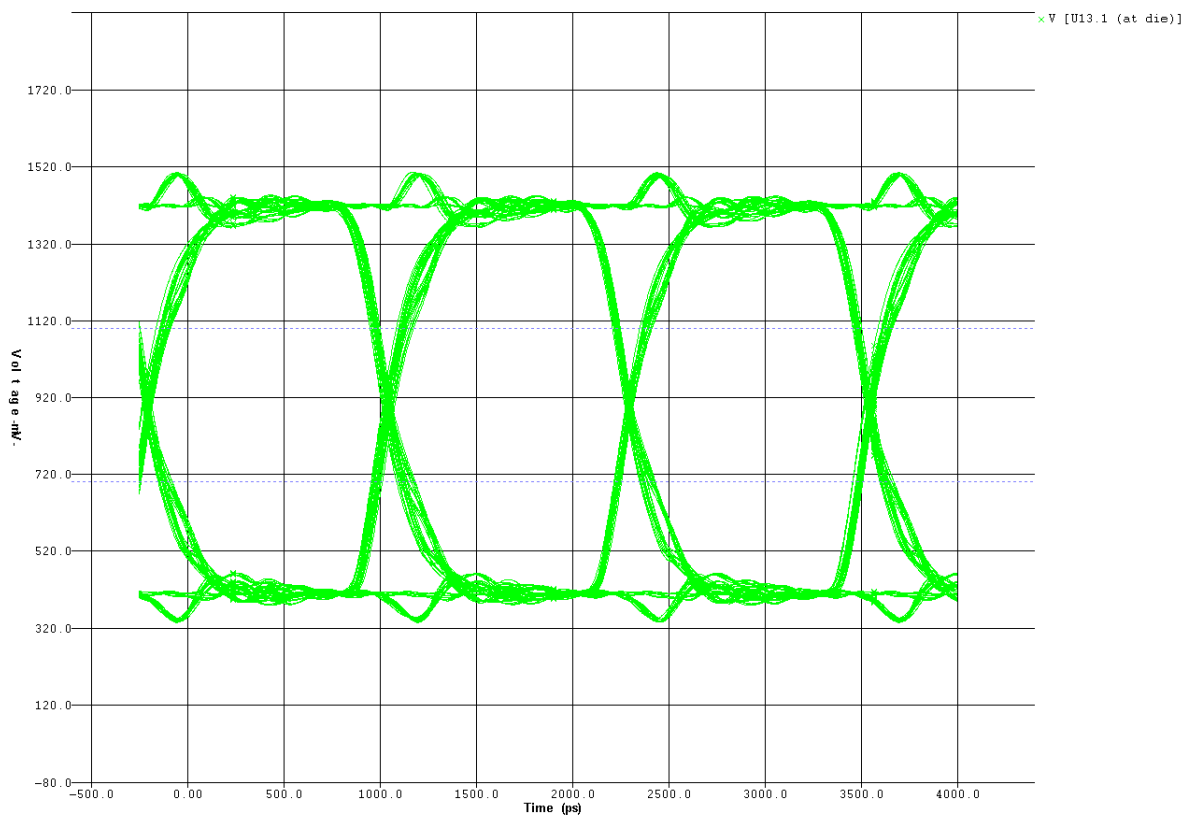
- read data (DQ on the bidirectional data signals for CIO RLD RAM II)
- read clocks (QK/QK#)

Altera recommends that you use the FPGA parallel OCT to terminate the data on reads and read clocks.

The eye diagrams are shown at the FPGA die pin, and the RLD RAM II output driver is Class I HSTL-18 using its ZQ calibration of $50\ \Omega$. The RLD RAM II read data is double data rate.

Figure 6-7 shows the ideal case of a fly-by terminated signal using $50\ \Omega$ calibrated parallel OCT for a Stratix IV device.

Figure 6-7. Read Data Simulation at 400 MHz with $50\ \Omega$ Parallel OCT Termination



Termination Schemes

Table 6–2 lists the recommended termination schemes for major CIO RLDRAM II memory interface signals, which include data (DQ), data mask (DM), clocks (CK, CK#, DK, DK#, QK, and QK#), address, bank address, and command (WE#, REF#, and CS#).

Table 6–2. Termination Recommendations for Arria II GZ, Arria V, Stratix III, Stratix IV, and Stratix V Devices

| Signal Type | HSTL 15/18 Standard ^{(1), (2), (3), (4)} | Memory End Termination |
|--|---|---|
| DK/DK# Clocks | Class I R50 NO CAL | 100 Ω Differential |
| QK/QK# Clocks | Class I P50 CAL | ZQ50 |
| Data (Write) | Class I R50 CAL | ODT |
| Data (Read) | Class I P50 CAL | ZQ50 |
| Data Mask | Class I R50 CAL | ODT |
| CK/CK# Clocks | Class I R50 NO CAL | $\times 1 = 100 \Omega$ Differential ⁽⁹⁾ $\times 2 = 200 \Omega$ Differential ⁽¹⁰⁾ |
| Address/Bank Address ^{(5), (6)} | Class I Max Current | 50 Ω Parallel to V_{TT} |
| Command (WE#, REF#) ^{(5), (6)} | Class I Max Current | 50 Ω Parallel to V_{TT} |
| Command (CS#) ^{(5), (6), (7)} | Class I Max Current | 50 Ω Parallel to V_{TT} or Pull-up to V_{DD} |
| QVLD ⁽⁸⁾ | Class I P50 CAL | ZQ50 |

Notes to Table 6–2:

- (1) R is effective series output impedance.
- (2) P is effective parallel input impedance.
- (3) CAL is OCT with calibration.
- (4) NO CAL is OCT without calibration.
- (5) For width expansion configuration, the address and control signals are routed to 2 devices. Recommended termination is 50 Ω parallel to V_{TT} at the trace split of a balanced T or Y routing topology. Use a clamshell placement of the two RLDRAM II components to achieve minimal stub delays and optimum signal integrity. Clamshell placement is when two devices overlay each other by being placed on opposite sides of the PCB.
- (6) The UniPHY default IP setting for this output is Max Current. A Class I 50 Ω output with calibration output is typically optimal in single load topologies.
- (7) Altera recommends that you use a 50 Ω parallel termination to V_{TT} if your design meets the power sequencing requirements of the RLDRAM II component. Refer to the RLDRAM II data sheet for further information.
- (8) QVLD is not used in the RLDRAM II Controller with UniPHY implementations.
- (9) $\times 1$ is a single-device load.
- (10) $\times 2$ is a double-device load. An alternative option is to use a 100 Ω differential termination at the trace split.



Altera recommends that you simulate your specific design for your system to ensure good signal integrity.

PCB Layout Guidelines

Table 6-3 lists the RLD RAM II general routing layout guidelines.



The following layout guidelines include several +/- length based rules. These length-based guidelines are for first order timing approximations if you cannot simulate the actual delay characteristics of your PCB implementation. They do not include any margin for crosstalk.



Altera recommends that you get accurate time base skew numbers when you simulate your specific implementation.

Table 6-3. RLD RAM II Layout Guidelines (Part 1 of 2)

| Parameter | Guidelines |
|----------------------|--|
| Impedance | <ul style="list-style-type: none"> ■ All signal planes must be 50 Ω, single-ended, $\pm 10\%$. ■ All signal planes must be 100 Ω, differential $\pm 10\%$. ■ Remove all unused via pads, because they cause unwanted capacitance. |
| Decoupling Parameter | <ul style="list-style-type: none"> ■ Use 0.1 μF in 0402 size to minimize inductance. ■ Make V_{TT} voltage decoupling close to pull-up resistors. ■ Connect decoupling caps between V_{TT} and ground. ■ Use a 0.1 μF cap for every other V_{TT} pin. ■ Verify your capacitive decoupling using the Altera Power Distribution Network (PDN) Design tool. |
| Power | <ul style="list-style-type: none"> ■ Route GND, 1.5 V/1.8 V as planes. ■ Route V_{CCIO} for memories in a single split plane with at least a 20-mil (0.020 inches or 0.508 mm) gap of separation. ■ Route V_{TT} as islands or 250-mil (6.35-mm) power traces. ■ Route oscillators and PLL power as islands or 100-mil (2.54-mm) power traces. |
| General Routing | <ul style="list-style-type: none"> ■ All specified delay matching requirements include PCB trace delays, different layer propagation, velocity variance, and crosstalk. To minimize PCB layer propagation variance, Altera recommends that signals from the same net group always be routed on the same layer. If you must route signals of the same net group on different layers with the same impedance characteristic, simulate your worst case PCB trace tolerances to ascertain actual propagation delay differences. Typical layer to layer trace delay variations are of 15 ps/inch order. ■ Use 45° angles (not 90° corners). ■ Avoid T-Junctions for critical nets or clocks. ■ Avoid T-junctions greater than 150 ps (approximately 500 mils, 12.7 mm). ■ Disallow signals across split planes. ■ Restrict routing other signals close to system reset signals. ■ Avoid routing memory signals closer than 0.025 inch (0.635 mm) to PCI or system clocks. ■ Match all signals within a given DQ group with a maximum skew of ± 10 ps or approximately ± 50 mils (0.254 mm) and route on the same layer. |

Table 6-3. RLD RAM II Layout Guidelines (Part 2 of 2)

| Parameter | Guidelines |
|-------------------------------|---|
| Clock Routing | <ul style="list-style-type: none"> ■ Route clocks on inner layers with outer-layer run lengths held to under 150 ps (approximately 500 mils, 12.7 mm). ■ These signals should maintain a 10-mil (0.254 mm) spacing from other nets. ■ Clocks should maintain a length-matching between clock pairs of ± 5 ps or approximately ± 25 mils (0.635 mm). ■ Differential clocks should maintain a length-matching between P and N signals of ± 2 ps or approximately ± 10 mils (0.254 mm). ■ Space between different clock pairs should be at least three times the space between the traces of a differential pair. |
| Address and Command Routing | <ul style="list-style-type: none"> ■ To minimize crosstalk, route address, bank address, and command signals on a different layer than the data and data mask signals. ■ Do not route the differential clock signals close to the address signals. ■ Keep the distance from the pin on the RLD RAM II component to the stub termination resistor (V_{TT}) to less than 50 ps (approximately 250 mils, 6.35 mm) for the address/command signal group. ■ Keep the distance from the pin on the RLD RAM II component to the fly-by termination resistor (V_{TT}) to less than 100 ps (approximately 500 mils, 12.7 mm) for the address/command signal group. |
| External Memory Routing Rules | <ul style="list-style-type: none"> ■ Apply the following parallelism rules for the RLD RAM II data/address/command groups: <ul style="list-style-type: none"> ■ 4 mils for parallel runs < 0.1 inch (approximately 1\times spacing relative to plane distance). ■ 5 mils for parallel runs < 0.5 inch (approximately 1\times spacing relative to plane distance). ■ 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2\times spacing relative to plane distance). ■ 15 mils for parallel runs between 1.0 and 3.3 inch (approximately 3\times spacing relative to plane distance). |
| Maximum Trace Length | <ul style="list-style-type: none"> ■ Keep the maximum trace length of all signals from the FPGA to the RLD RAM II components to 600 ps (approximately 3,300 mils, 83.3 mm). |

Using the layout guidelines in [Table 6-3](#), Altera recommends the following layout approach:

1. If the RLD RAM II interface has multiple DQ groups ($\times 18$ or $\times 36$ RLD RAM II component or width expansion configuration), match all the $DK/DK\#$ and $QK/QK\#$ clocks as tightly as possible to optimize the timing margins in your design.
2. Route the $DK/DK\#$ write clock and $QK/QK\#$ read clock associated with a DQ group on the same PCB layer. Match these clock pairs to within ± 5 ps.
3. Set the $DK/DK\#$ or $QK/QK\#$ clock as the target trace propagation delay for the associated data and data mask signals.
4. Route the data and data mask signals for the DQ group ideally on the same layer as the associated $QK/QK\#$ and $DK/DK\#$ clocks to within ± 10 ps skew of the target clock.
5. Route the $CK/CK\#$ clocks and set as the target trace propagation delays for the address/command signal group. Match the $CK/CK\#$ clock to within ± 50 ps of all the $DK/DK\#$ clocks.

6. Route the address/control signal group (address, bank address, CS, WE, and REF) ideally on the same layer as the CK/CK# clocks, to within ± 20 ps skew of the CK/CK# traces.

This layout approach provides a good starting point for a design requirement of the highest clock frequency supported for the RLD RAM II interface.



Altera recommends that you create your project in the Quartus® II software with a fully implemented RLD RAM II Controller with UniPHY interface, and observe the interface timing margins to determine the actual margins for your design.

Although the recommendations in this chapter are based on simulations, you can apply the same general principles when determining the best termination scheme, drive strength setting, and loading style to any board designs. Even armed with this knowledge, it is still critical that you perform simulations, either using IBIS or HSPICE models, to determine the quality of signal integrity on your designs.

Document Revision History

Table 6-4 lists the revision history for this document.

Table 6-4. Document Revision History

| Date | Version | Changes |
|---------------|---------|------------------------------|
| November 2011 | 3.0 | Added Arria V information. |
| June 2011 | 2.0 | Added Stratix V information. |
| December 2010 | 1.0 | Initial release. |