


This chapter provides guidelines for you to improve your system's signal integrity and layout guidelines to help successfully implement a QDR II or QDR II+ SRAM interface in your system.

The QDR II and QDR II+ SRAM Controller with UniPHY intellectual property (IP) enables you to implement QDR II and QDR II+ interfaces with Arria® II GX, Arria V, Stratix® III, Stratix IV, and Stratix V devices.

 In this chapter, QDR II SRAM refers to both QDR II and QDR II+ SRAM unless stated otherwise.


This chapter focuses on the following key factors that affect signal integrity:

- I/O standards
- QDR II SRAM configurations
- Signal terminations
- Printed circuit board (PCB) layout guidelines

I/O Standards

QDR II SRAM interface signals use one of the following JEDEC I/O signalling standards:

- HSTL-15—provides the advantages of lower power and lower emissions.
- HSTL-18—provides increased noise immunity with slightly greater output voltage swings.

 To select the most appropriate standard for your interface, refer to the *Arria II GX Devices Data Sheet: Electrical Characteristics* chapter in the *Arria II Device Handbook*, *Stratix III Device Datasheet: DC and Switching Characteristics* chapter in the *Stratix III Device Handbook*, or the *Stratix IV Device Datasheet DC and Switching Characteristics* chapter in the *Stratix IV Device Handbook*.

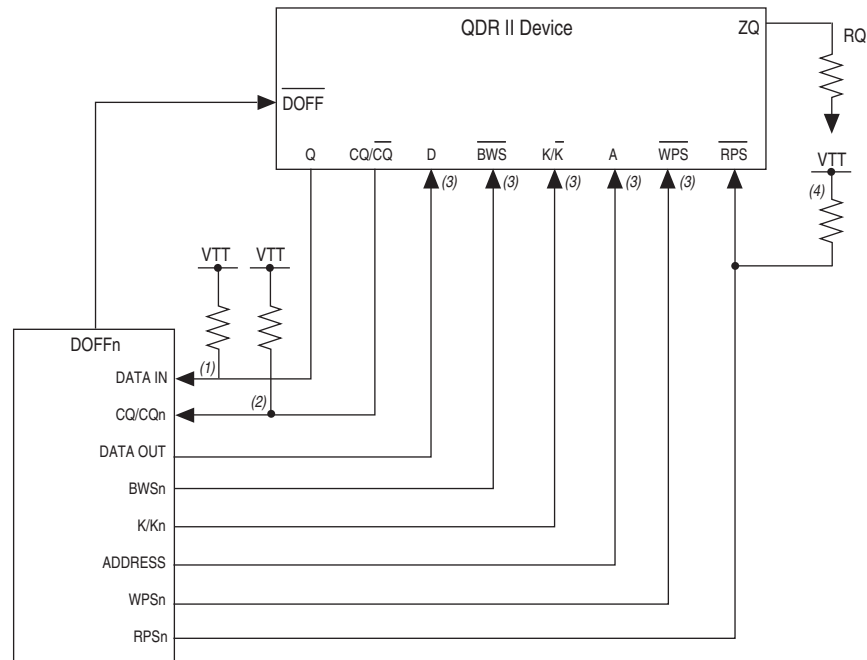
Altera® QDR II SRAM Controller with UniPHY IP defaults to HSTL 1.5 V Class I outputs and HSTL 1.5 V inputs.

QDR II SRAM Configurations

The QDR II SRAM Controller with UniPHY IP supports interfaces with a single device, and two devices in a width expansion configuration up to maximum width of 72 bits.

Figure 7-1 shows the main signal connections between the FPGA and a single QDR II SRAM component.

Figure 7-1. Configuration With A Single QDR II SRAM Component

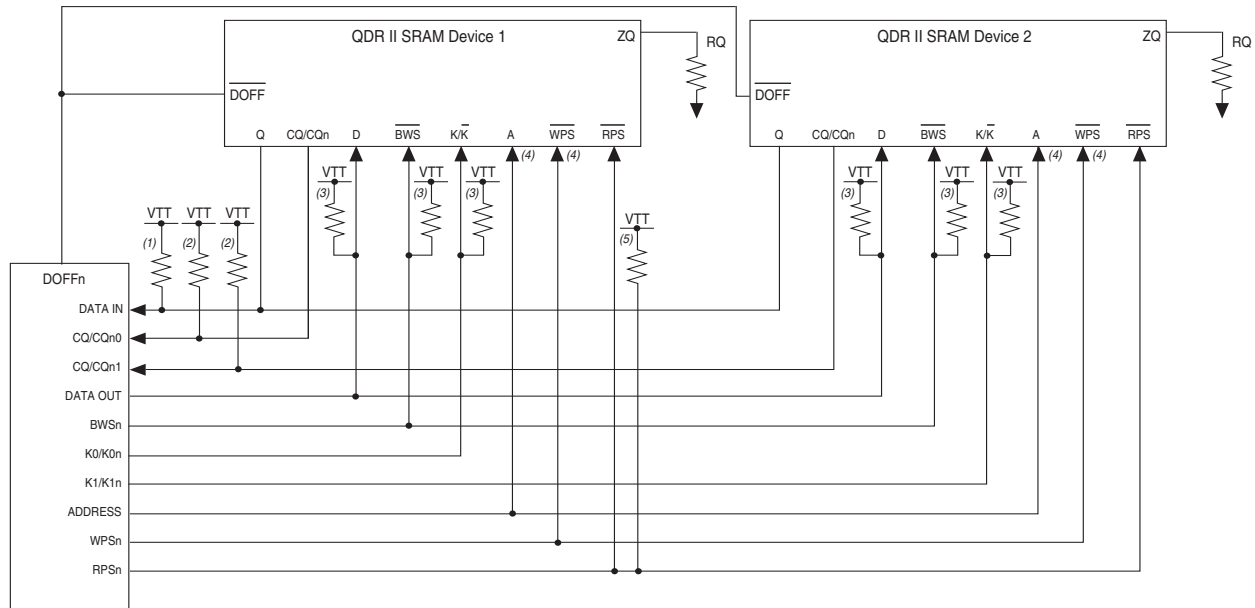


Notes to Figure 7-1:

- (1) Use external discrete termination only for data inputs targeting Arria II GX devices that do not support parallel OCT. For Stratix III and Stratix IV devices, use parallel OCT.
- (2) Use external discrete termination only for CQ/CQ# targeting Arria II GX devices, or for any device using ×36 emulated mode.
- (3) Use external discrete termination for this signal, as shown for RPS.
- (4) Use external discrete termination with fly-by placement to avoid stubs.

Figure 7-2 shows the main signal connections between the FPGA and two QDR II SRAM components in a width expansion configuration.

Figure 7-2. Configuration With Two QDR II SRAM Components In A Width Expansion Configuration

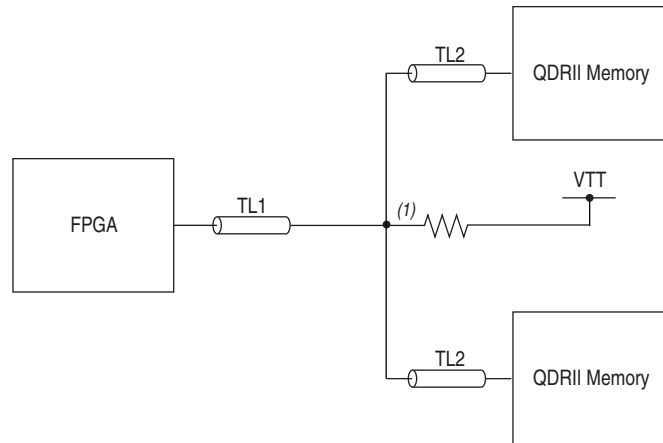


Notes to Figure 7-2:

- (1) Use external discrete termination only for data inputs targeting Arria II GX devices that do not support parallel OCT. For Stratix III and Stratix IV devices, use parallel OCT.
- (2) Use external discrete termination only for CQ/CQ# targeting Arria II GX devices, or for any device using x36 emulated mode.
- (3) Use external discrete termination for data outputs, BWSn, and K/K# clocks with fly-by placement to avoid stubs.
- (4) Use external discrete termination for this signal, as shown for RPS.
- (5) Use external discrete termination at the trace split of the balanced T or Y topology.

Figure 7-3 shows the detailed balanced topology recommended for the address and command signals in the width expansion configuration.

Figure 7-3. External Parallel Termination for Balanced Topology



Note to Figure 7-3:

- (1) To minimize the reflections and parallel impedance discontinuity seen by the signal, place the trace split close to the QDR II SRAM memory components. Keep TL2 short so that the QDR II SRAM components appear as a lumped load.

Signal Terminations

Arria II GX, Stratix III and Stratix IV devices offer on-chip termination (OCT) technology.

Table 7-1 summarizes the extent of OCT support for each device.

Table 7-1. On-Chip Termination Schemes ⁽¹⁾

Termination Scheme	HSTL-15 and HSTL-18	FPGA Device					
		Arria II GX		Arria II GZ, Stratix III, and Stratix IV		Arria V and Stratix V	
		Column I/O	Row I/O	Column I/O	Row I/O	Column I/O	Row I/O
On-Chip Series Termination without Calibration	Class I	50	50	50	50	—	—
On-Chip Series Termination with Calibration	Class I	50	50	50	50	—	—
On-Chip Parallel Termination with Calibration	Class I	—	—	50	50	50	50

Note to Table 7-1:

- (1) This table provides information about HSTL-15 and HSTL-18 standards because these are the supported I/O standards for QDR II SRAM memory interfaces by Altera FPGAs.

On-chip series (R_S) termination is supported only on output and bidirectional buffers, while on-chip parallel (R_T) termination is supported only on input and bidirectional buffers. Because QDR II SRAM interfaces have unidirectional data paths, dynamic OCT is not required.

For Arria II GX, Stratix III and Stratix IV devices, the HSTL Class I I/O calibrated terminations are calibrated against $50\ \Omega$ 1% resistors connected to the R_{UP} and R_{DN} pins in an I/O bank with the same VCCIO as the QDR II SRAM interface. The calibration occurs at the end of the device configuration.

QDR II SRAM controllers have a ZQ pin which is connected via a resistor R_Q to ground. Typically the QDR II SRAM output signal impedance is $0.2 \times R_Q$. Refer to the QDR II SRAM device data sheet for more information.



For information about OCT, refer to the *I/O Features in Arria II GX Devices* chapter in the *Arria II GX Device Handbook*, *I/O Features in Arria V Devices* chapter in the *Arria V Device Handbook*, *Stratix III Device I/O Features* chapter in the *Stratix III Device Handbook*, *I/O Features in Stratix IV Devices* chapter in the *Stratix IV Device Handbook*, and the *I/O Features in Stratix V Devices* chapter in the *Stratix V Device Handbook*

The following section shows HyperLynx simulation eye diagrams to demonstrate signal termination options. Altera strongly recommends signal terminations to optimize signal integrity and timing margins, and to minimize unwanted emissions, reflections, and crosstalk.

All of the eye diagrams shown in this section are for a $50\ \Omega$ trace with a propagation delay of 720 ps which is approximately a 4-inch trace on a standard FR4 PCB. The signal I/O standard is HSTL-15.

For point-to-point signals, Altera recommends that you place a fly-by termination by terminating at the end of the transmission line after the receiver to avoid unterminated stubs. The guideline is to place the fly-by termination within 100 ps propagation delay of the receiver.

Although not recommended, you can place the termination before the receiver, which leaves an unterminated stub. The stub delay is critical because the stub between the termination and the receiver is effectively unterminated, causing additional ringing and reflections. Stub delays should be less than 50 ps.

The eye diagrams shown in this section show the best case achievable and do not take into account PCB vias, crosstalk and other degrading effects such as variations in the PCB structure due to manufacturing tolerances.



Simulate your design to ensure correct functionality.

Output from the FPGA to the QDR II SRAM Component

The following output signals are from the FPGA to the QDR II SRAM component:

- write data
- byte write select (BWSn)
- address
- control (WPSn and RPSn)
- clocks, $\kappa/\kappa\#$

Altera recommends that you terminate the write clocks, κ and $\kappa\#$, with a single-ended fly-by $50\ \Omega$ parallel termination to V_{TT} . However, simulations show that you can consider a differential termination if the clock pair is well matched and routed differentially.

The HyperLynx simulation eye diagrams show simulation cases of write data and address signals with termination options. The QDR II SRAM write data is double data rate. The QDR II SRAM address is either double data rate (burst length of 2) or single data rate (burst length of 4).

Simulations show that lowering the drive strength does not make a significant difference to the eye diagrams. All eye diagrams are shown at the QDR II SRAM device receiver pin.

Figure 7-4 shows the fly-by terminated signal using Stratix IV Class I HSTL-15 with calibrated $50\ \Omega$ OCT output driver.

Figure 7-4. Write Data Simulation at 400 MHz with Fly-By $50\ \Omega$ Parallel Termination to V_{TT}

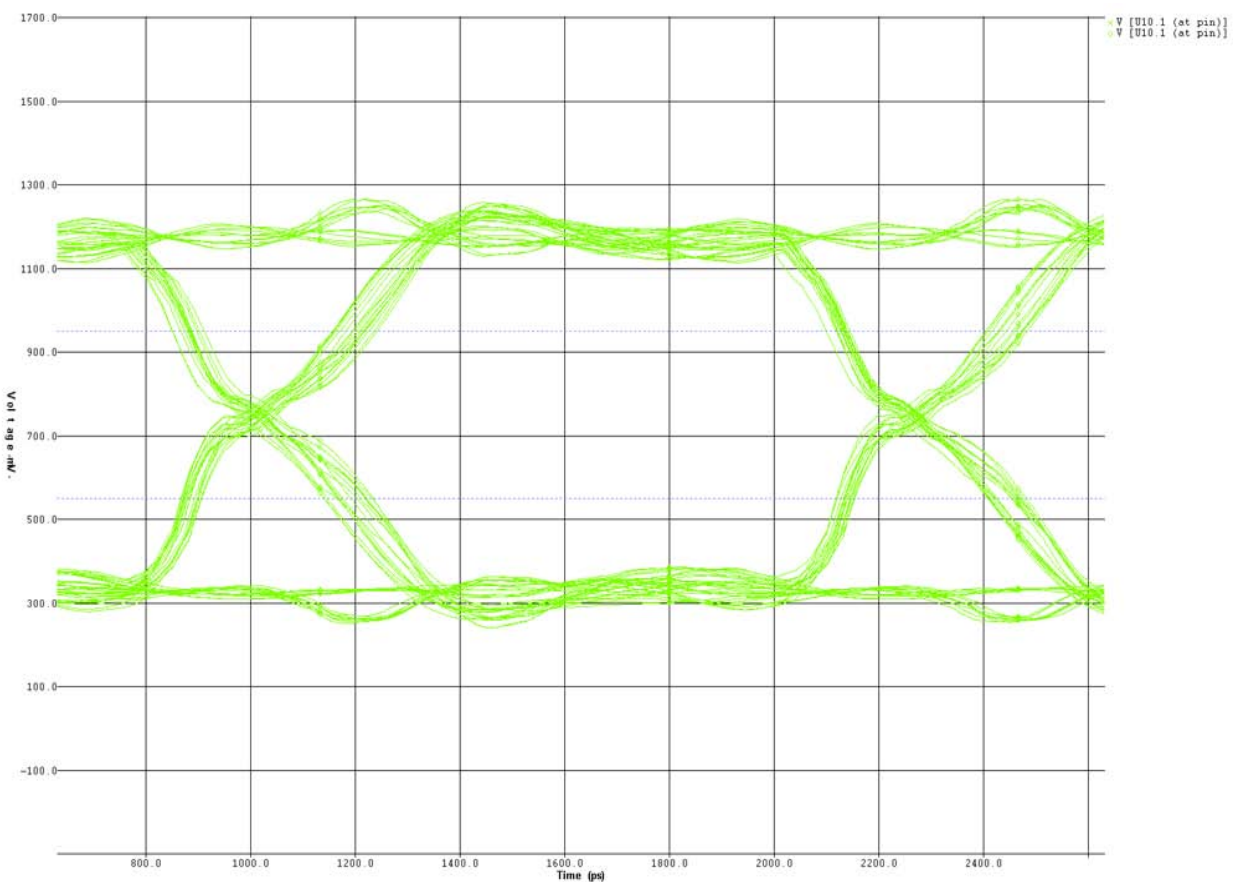


Figure 7-5 shows an unterminated signal using Stratix IV Class I HSTL-15 with a calibrated $50\ \Omega$ OCT output driver. This unterminated solution is not recommended.

Figure 7-5. Write Data Simulation at 400 MHz with No Far-End Termination

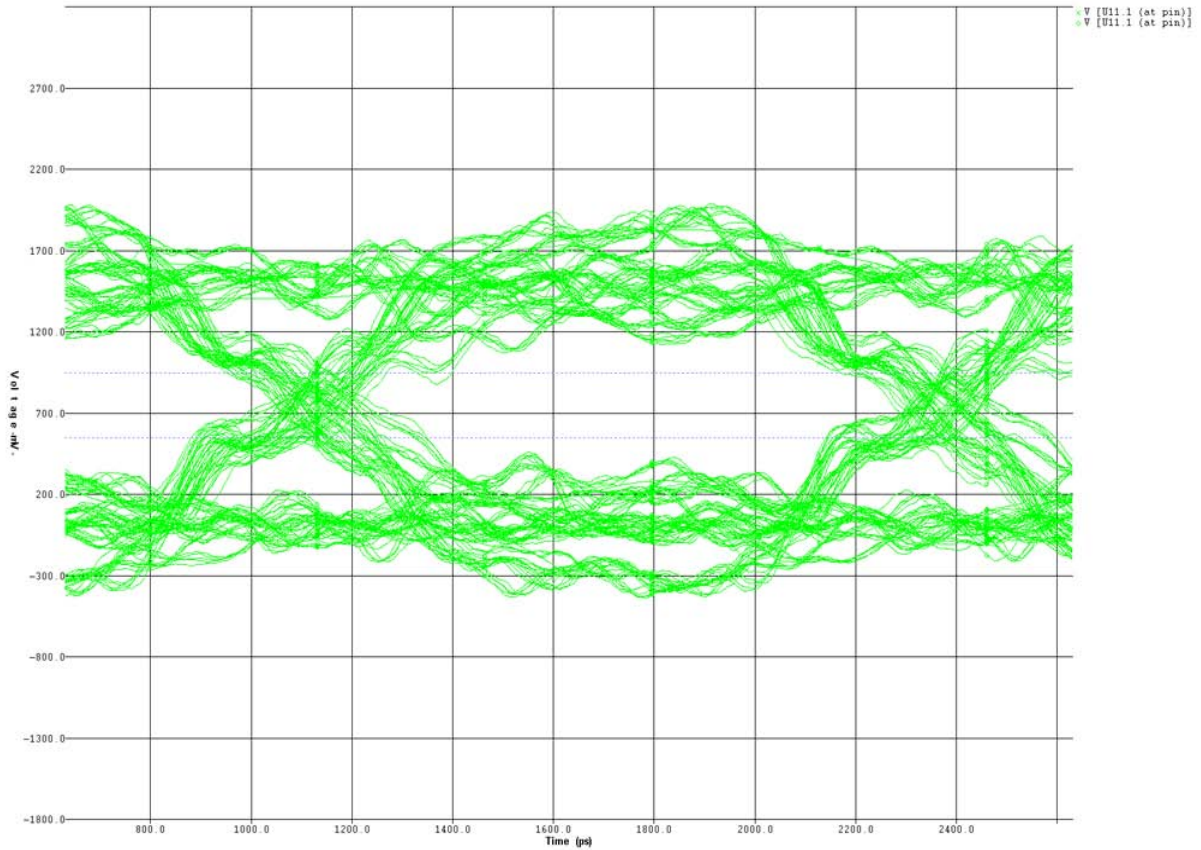


Figure 7-6 shows an unterminated signal at a lower frequency of 250 MHz using Arria II GX Class I HSTL-15 with calibrated 50 Ω OCT output driver. This unterminated solution may be passable for some systems, but is shown so that you can compare against the superior quality of the terminated signal in Figure 7-4.

Figure 7-6. Write Data Simulation at 250 MHz with No Far-End Termination

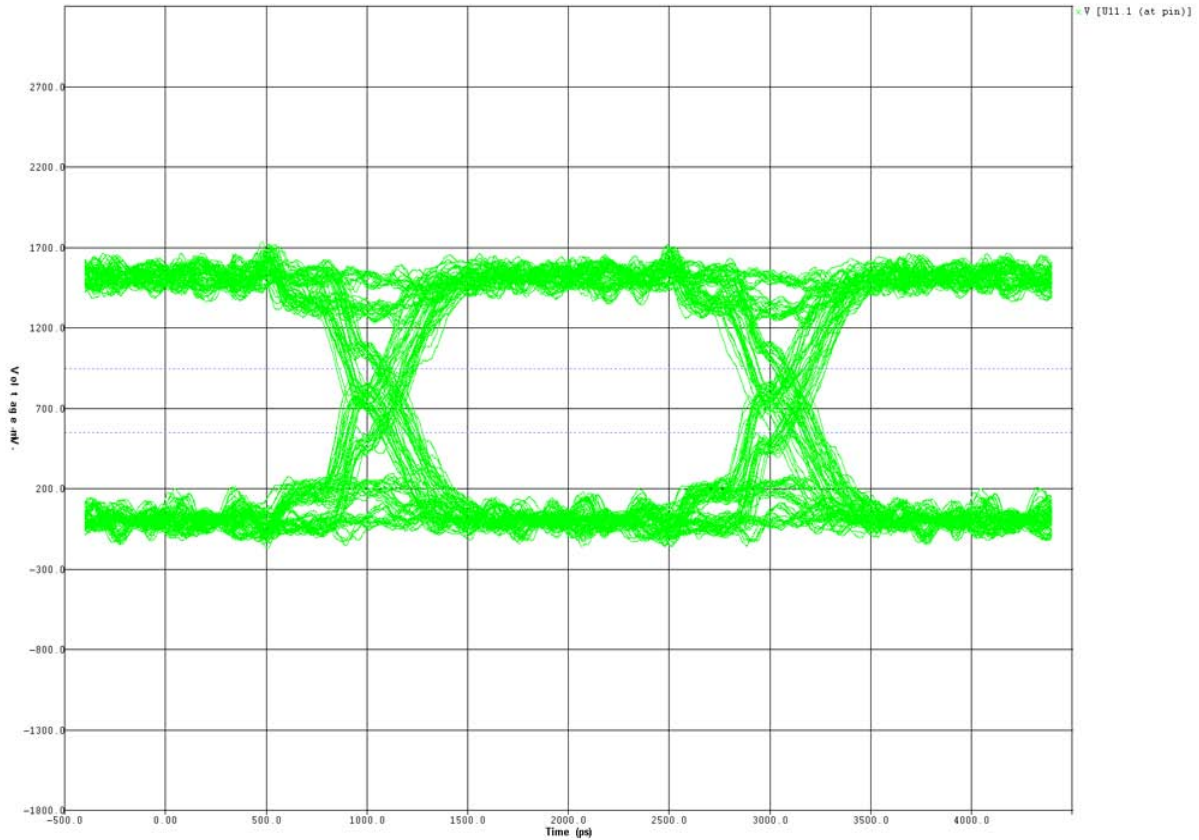


Figure 7-7 shows an unterminated signal at a frequency of 175 MHz with a point-to-point connection. QDR II SRAM interfaces using Stratix IV devices have a maximum supported frequency of 350 MHz. For QDR II SRAM with burst length of four interfaces, the address signals are effectively single data rate at 175 MHz. This unterminated solution is not recommended but can be considered. The FPGA output driver is Class I HSTL-15 with a calibrated 50 Ω OCT.

Figure 7-7. Address Simulation for QDR II SRAM Burst Length of 4 at 175 MHz with No Far-End Termination

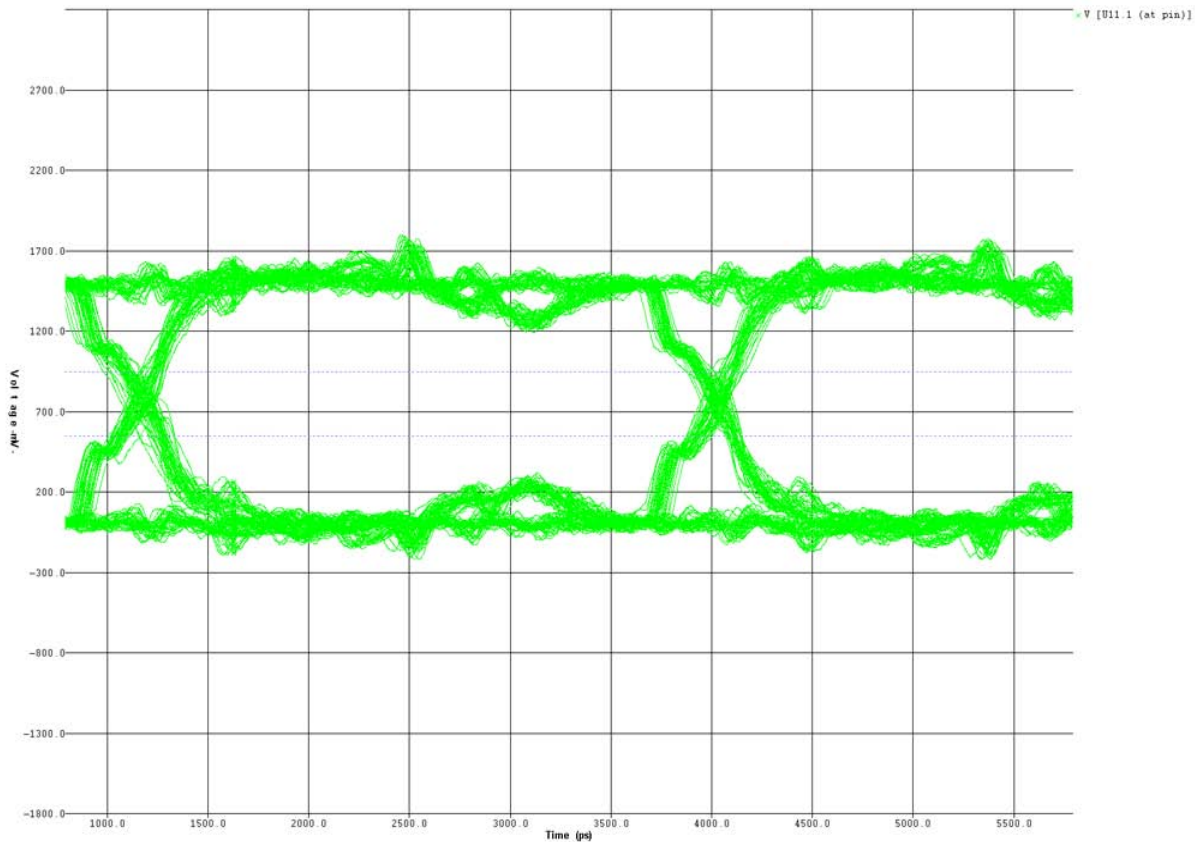
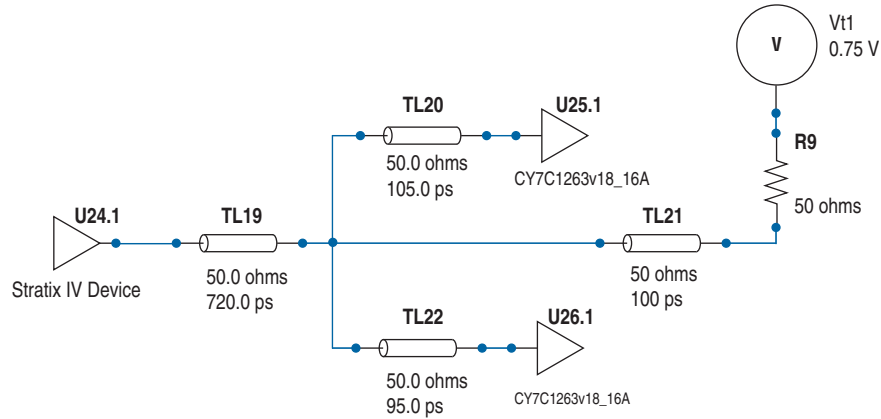


Figure 7-8 shows a typical topology, which are used for two components in width expansion mode. Altera recommends that you match the stubs TL20 and TL22, but you can allow small differences allowed to achieve acceptable signal integrity.

Figure 7-8. Address for QDR II SRAM Burst Length of 2 in Width Expansion Mode Topology



The eye diagrams in Figure 7-9 and Figure 7-10 use the topology shown in Figure 7-8. The eye diagram in Figure 7-11 uses the topology shown in Figure 7-8 without the V_{TT} termination, R9 and TL21.

Figure 7-9 shows an address signal at a frequency of 400 MHz with parallel $50\ \Omega$ termination to V_{TT} for QDR II SRAM burst length of 2 width expansion using Stratix IV Class I HSTL-15 12 mA driver and fly-by $50\ \Omega$ parallel termination to V_{TT} .

Figure 7-9. Address Simulation Using Stratix IV Class I HSTL-15 12 mA Driver and Fly-by $50\ \Omega$ Parallel Termination to V_{TT}

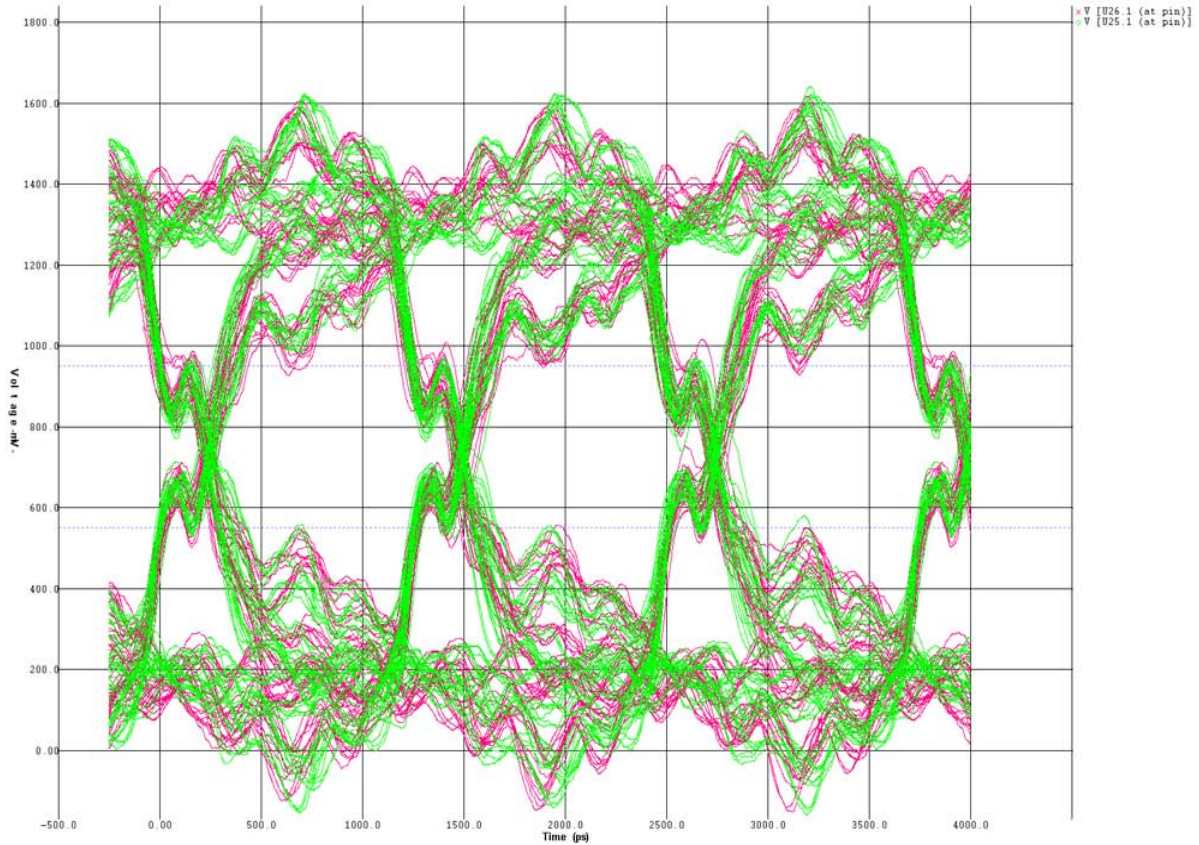


Figure 7-10 shows an address signal at a frequency of 400 MHz with parallel $50\ \Omega$ termination to V_{TT} for QDR II SRAM burst length of 2 width expansion using Stratix IV Class I HSTL-15 with $50\ \Omega$ calibration driver and fly-by $50\ \Omega$ parallel termination to V_{TT} . The waveform eye is significantly improved compared to the maximum (12mA) drive strength case.

Figure 7-10. Address Simulation Using Stratix IV Class I HSTL-15 $50\ \Omega$ Calibration Driver and Fly-by $50\ \Omega$ Parallel Termination to V_{TT}

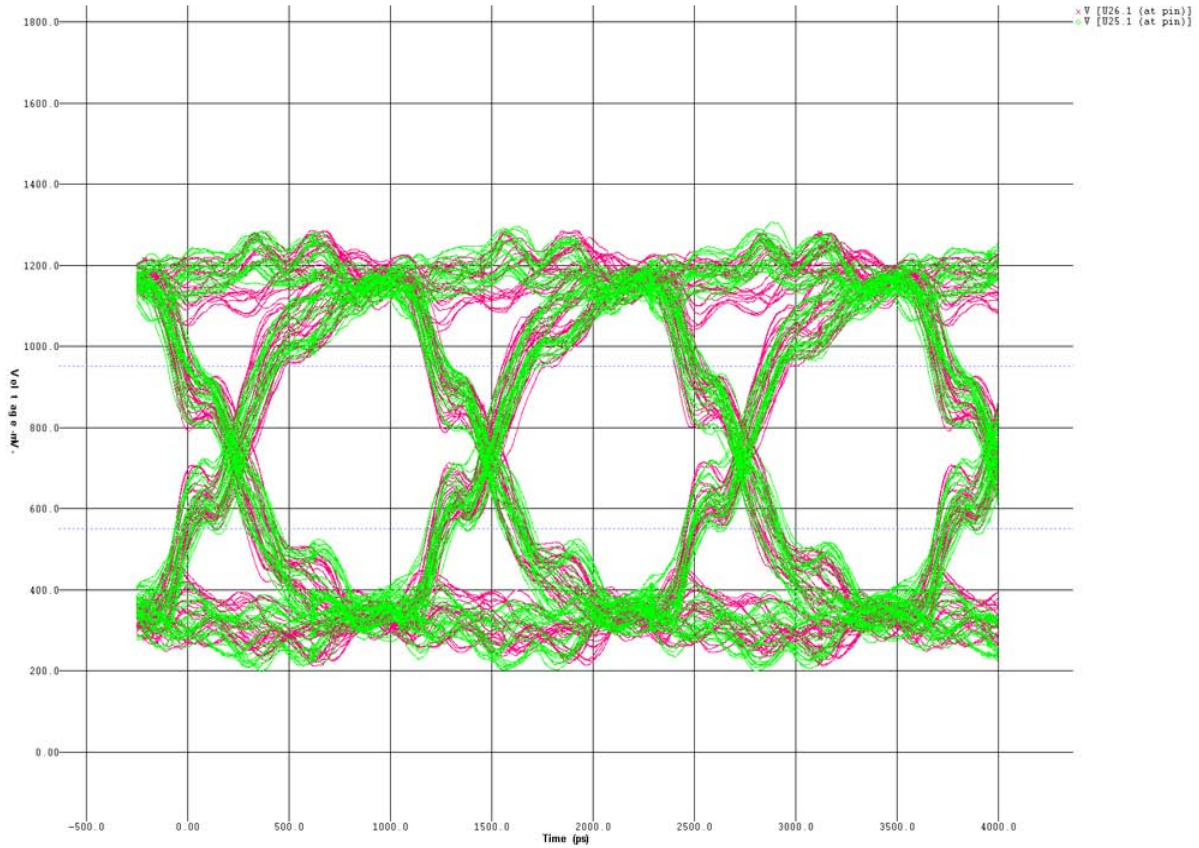
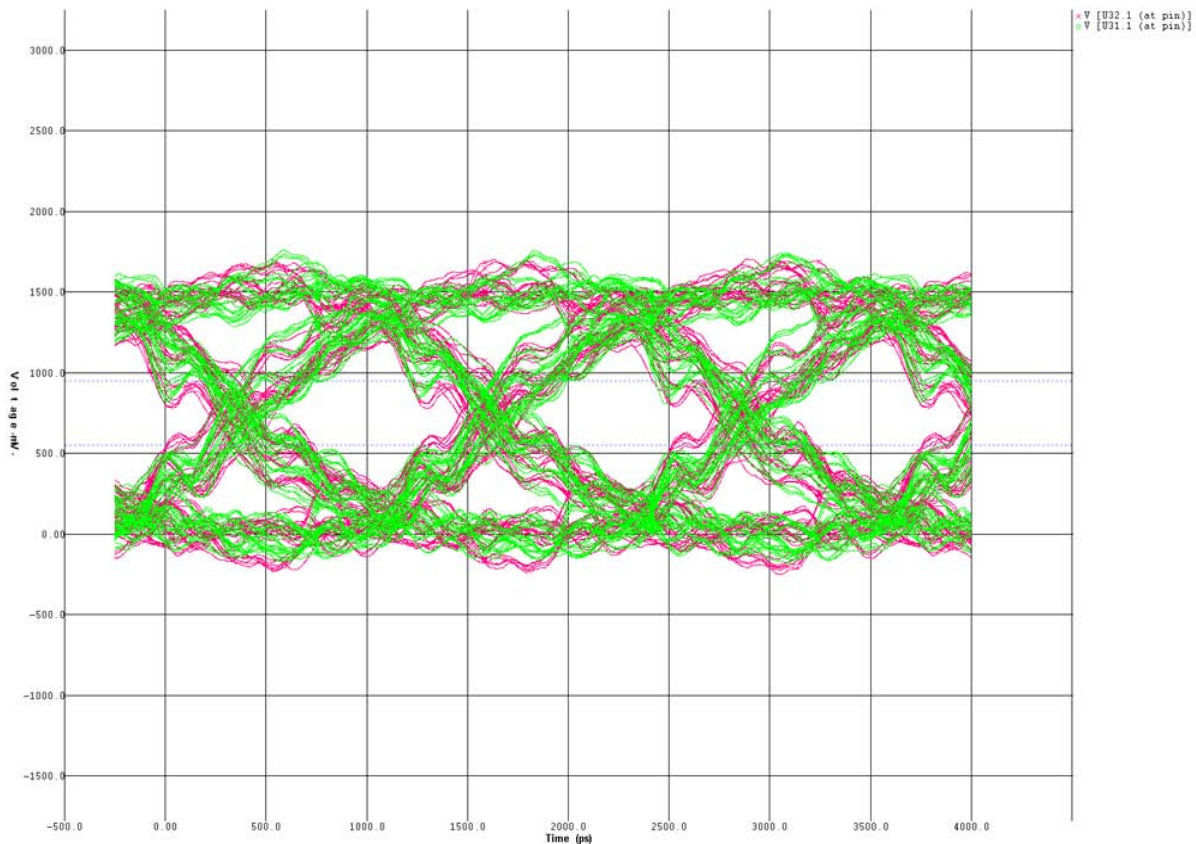


Figure 7-11 shows an unterminated address signal at a frequency of 400 MHz for QDR II SRAM burst length of 2 width expansion using Stratix IV Class I HSTL-15 with 50 Ω calibration driver. This unterminated address has small eye and is not recommended.

Figure 7-11. Address Simulation Using Stratix IV Class I HSTL-15 50 Ω Calibration Driver and No Termination



Input to the FPGA from the QDR II SRAM Component

The QDR II SRAM component drives the following input signals into the FPGA:

- read data
- echo clocks, CQ/CQ#

For point-to-point signals, Altera recommends that you use the FPGA parallel OCT wherever possible. For devices that do not support parallel OCT (Arria II GX), and for $\times 36$ emulated configuration CQ/CQ# termination, Altera recommends that you use a fly-by 50 Ω parallel termination to V_{TT} . Although not recommended, you can use parallel termination with a short stub of less than 50 ps propagation delay as an alternative option. The input echo clocks, CQ and CQ# must not use a differential termination.

The eye diagrams are shown at the FPGA receiver pin, and the QDR II SRAM output driver is Class I HSTL-15 using its ZQ calibration of 50 Ω . The QDR II SRAM read data is double data rate.

Figure 7-12 shows the ideal case of a fly-by terminated signal using 50 Ω calibrated parallel OCT with Stratix IV device.

Figure 7-12. Read Data Simulation at 400 MHz with 50 Ω Parallel OCT Termination

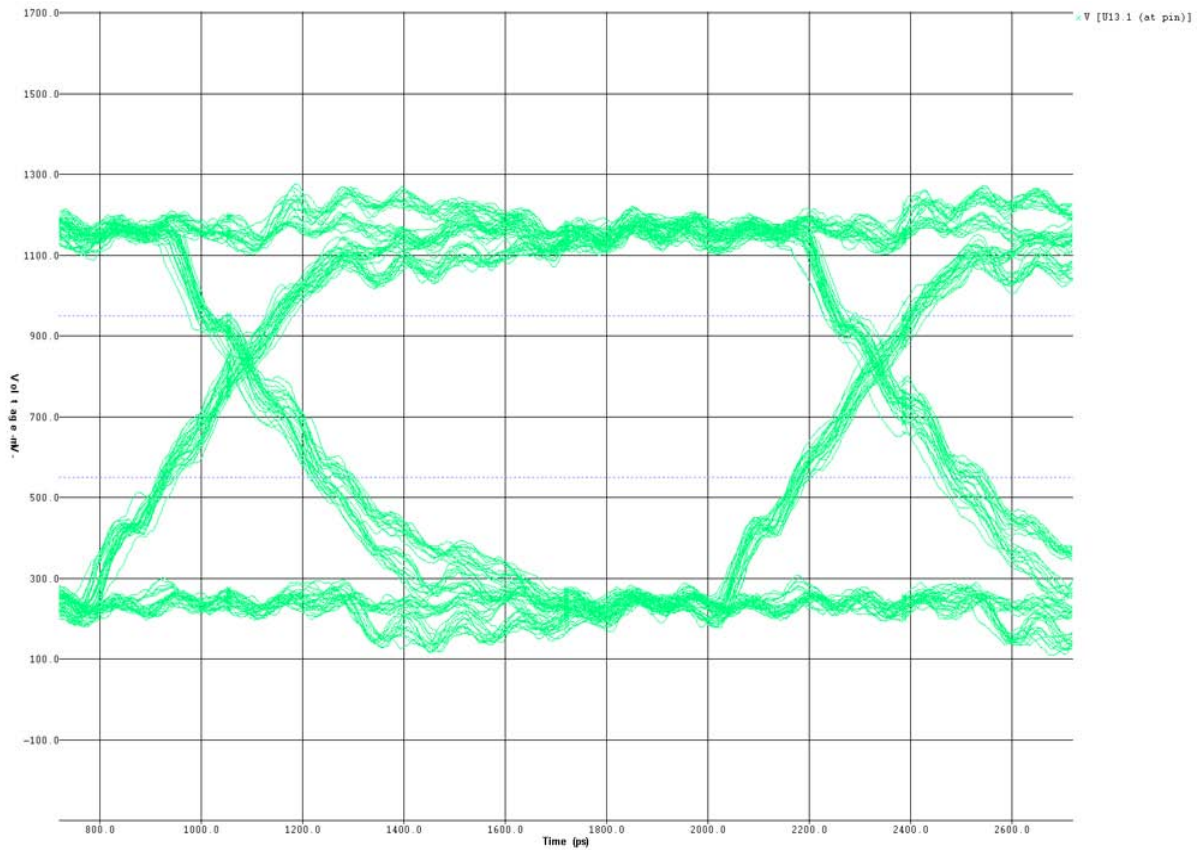


Figure 7-13 shows an external discrete component fly-by terminated signal at a lower frequency of 250 MHz using an Arria II GX device.

Figure 7-13. Read Data Simulation at 250 MHz with Fly-By Parallel 50 Ω Termination

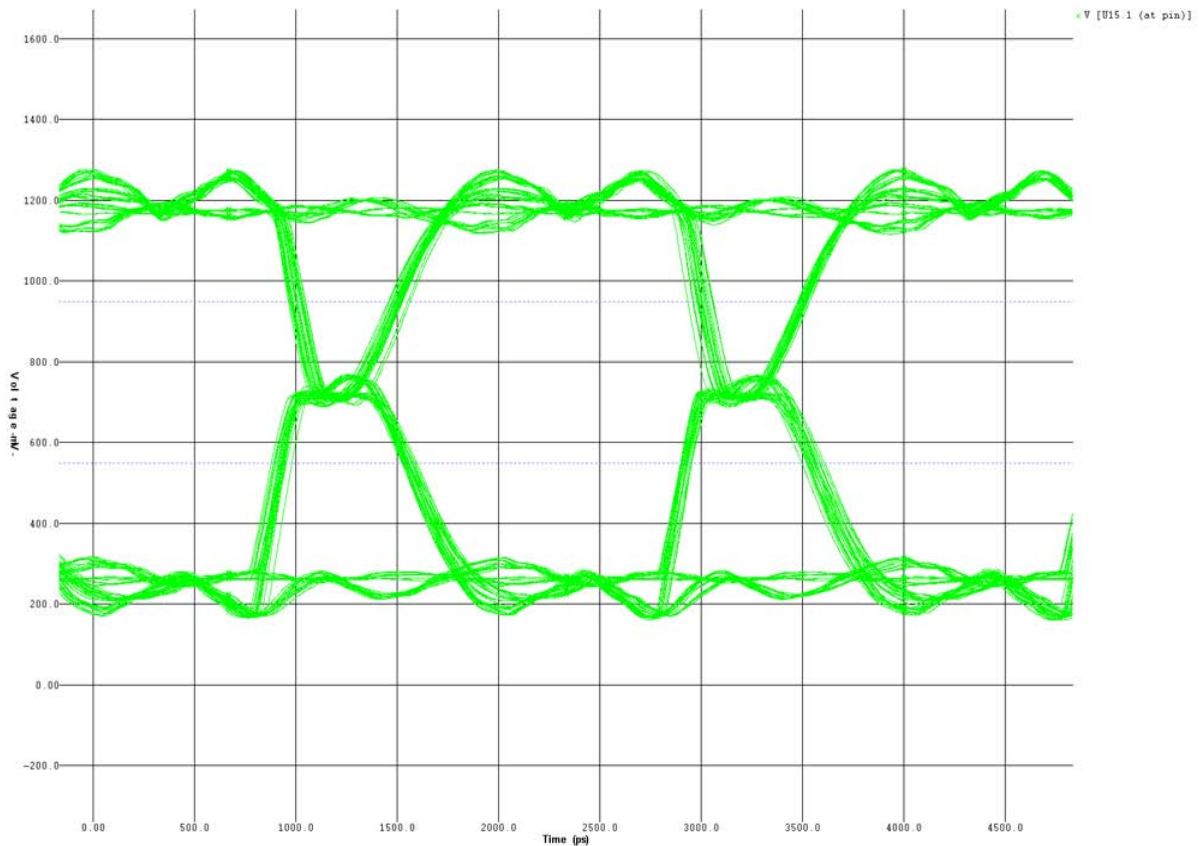
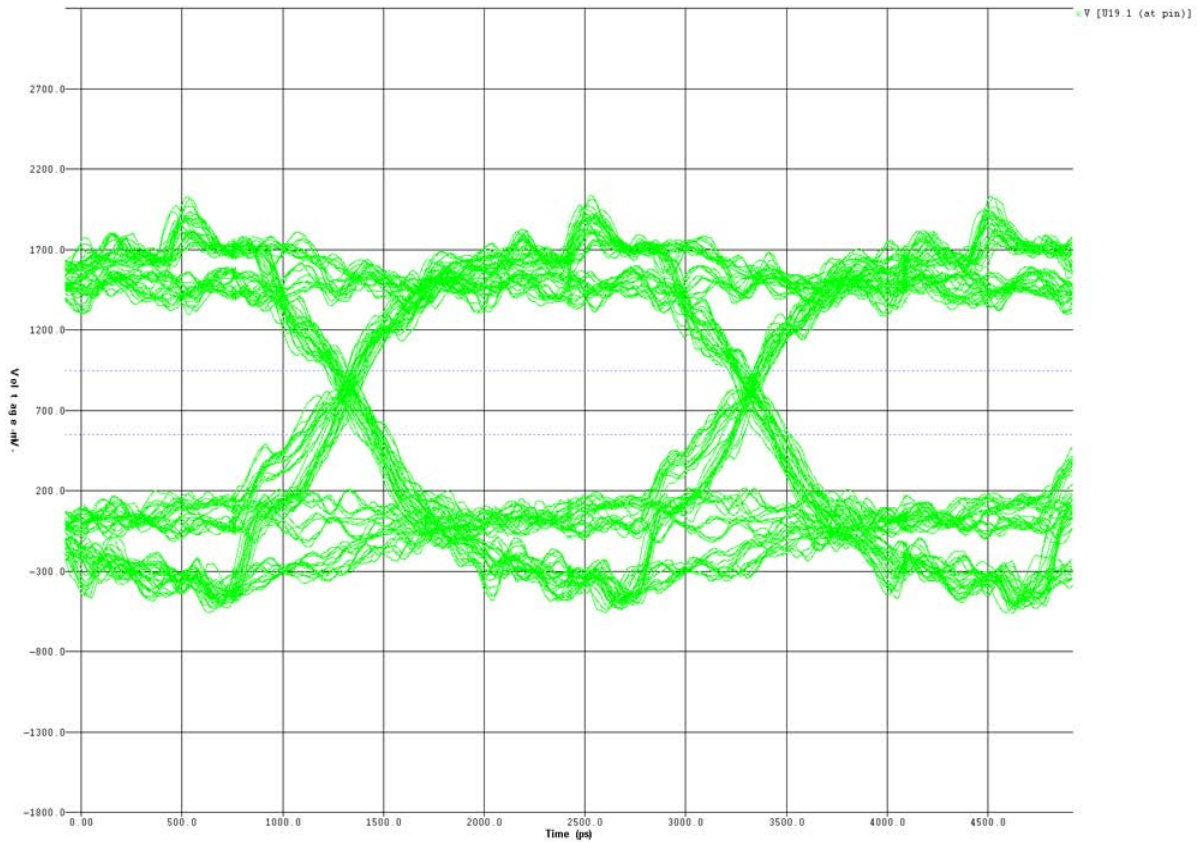


Figure 7-14 shows an unterminated signal at a lower frequency of 250 MHz using an Arria II GX device. This unterminated solution is not recommended but is shown so that you can compare against the superior quality of the terminated signal in Figure 7-13.

Figure 7-14. Read Data Simulation at 250 MHz with No Far-End Termination



Termination Schemes

Table 7-2 and Table 7-3 list the recommended termination schemes for major QDR II SRAM memory interface signals, which include write data (D), byte write select (BWS), read data (Q), clocks (K, K#, CQ, and CQ#), address and command (WPS and RPS).

Table 7-2. Termination Recommendations for Arria II GX Devices

Signal Type	HSTL 15/18 Standard (1), (2)	FPGA End Discrete Termination	Memory End Termination
K/K# Clocks	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
Write Data	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
BWS	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
Address (3), (4)	Class I Max Current	—	50 Ω Parallel to V_{TT}
WPS, RPS (3), (4)	Class I Max Current	—	50 Ω Parallel to V_{TT}
CQ/CQ#	Class I	50 Ω Parallel to V_{TT}	ZQ50
CQ/CQ# ×36 emulated (5)	Class I	50 Ω Parallel to V_{TT}	ZQ50
Read Data (Q)	Class I	50 Ω Parallel to V_{TT}	ZQ50
QVLD (6)	—	—	ZQ50

Notes to Table 7-2:

- (1) R is effective series output impedance.
- (2) CAL is calibrated OCT.
- (3) For width expansion configuration, the address and control signals are routed to 2 devices. Recommended termination is 50 Ω parallel to V_{TT} at the trace split of a balanced T or Y routing topology. For 400 MHz burst length 2 configurations where the address signals are double data rate, it is recommended to use a clamshell placement of the two QDR II SRAM components to achieve minimal stub delays and optimum signal integrity. Clamshell placement is when two devices overlay each other by being placed on opposite sides of the PCB.
- (4) The UniPHY default IP setting for this output is Max Current. A Class I 50 Ω output with calibration output is typically optimal in single load topologies.
- (5) For ×36 emulated mode, the recommended termination for the CQ/CQ# signals is a 50 Ω parallel termination to V_{TT} at the trace split, refer to Figure 7-15. Altera recommends that you use this termination when ×36 DQ/DQS groups are not supported in the FPGA.
- (6) QVLD is not used in the QDR II or QDR II+ SRAM with UniPHY implementations.

Table 7-3. Termination Recommendations for Arria V, Stratix III, Stratix IV, and Stratix V Devices (Part 1 of 2)

Signal Type	HSTL 15/18 Standard (1), (2), (3)	FPGA End Discrete Termination	Memory End Termination
K/K# Clocks	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
Write Data	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
BWS	Class I R50 CAL	—	50 Ω Parallel to V_{TT}
Address (4), (5)	Class I Max Current	—	50 Ω Parallel to V_{TT}
WPS, RPS (4), (5)	Class I Max Current	—	50 Ω Parallel to V_{TT}
CQ/CQ#	Class I P50 CAL	—	ZQ50
CQ/CQ# ×36 emulated (6)	—	50 Ω Parallel to V_{TT}	ZQ50
Read Data (Q)	Class I P50 CAL	—	ZQ50

Table 7-3. Termination Recommendations for Arria V, Stratix III, Stratix IV, and Stratix V Devices (Part 2 of 2)

Signal Type	HSTL 15/18 Standard (1), (2), (3)	FPGA End Discrete Termination	Memory End Termination
QVLD (7)	Class I P50 CAL	—	ZQ50

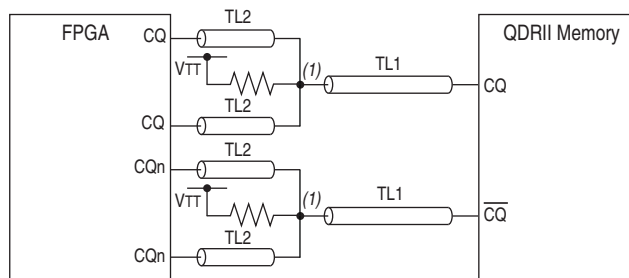
Notes to Table 7-3:

- (1) R is effective series output impedance.
- (2) P is effective parallel input impedance.
- (3) CAL is calibrated OCT.
- (4) For width expansion configuration, the address and control signals are routed to 2 devices. Recommended termination is $50\ \Omega$ parallel to V_{TT} at the trace split of a balanced T or Y routing topology. For 400 MHz burst length 2 configurations where the address signals are double data rate, it is recommended to use a "clam shell" placement of the two QDR II SRAM components to achieve minimal stub delays and optimum signal integrity. "Clam shell" placement is when two devices overlay each other by being placed on opposite sides of the PCB.
- (5) The UniPHY default IP setting for this output is Max Current. A Class 1 $50\ \Omega$ output with calibration output is typically optimal in single load topologies.
- (6) For $\times 36$ emulated mode, the recommended termination for the $CQ/CQ\#$ signals is a $50\ \Omega$ parallel termination to V_{TT} at the trace split, refer to Figure 7-15. Altera recommends that you use this termination when $\times 36$ DQ/DQS groups are not supported in the FPGA.
- (7) QVLD is not used in the QDR II or QDR II+ SRAM Controller with UniPHY implementations.



Altera recommends that you simulate your specific design for your system to ensure good signal integrity.

For a $\times 36$ QDR II SRAM interface that uses an emulated mode of two $\times 18$ DQS groups in the FPGA, there are two $CQ/CQ\#$ connections at the FPGA and a single $CQ/CQ\#$ output from the QDR II SRAM device. Altera recommends that you use a balanced T topology with the trace split close to the FPGA and a parallel termination at the split, as shown in Figure 7-15.

Figure 7-15. Emulated $\times 36$ Mode CQ/CQn Termination Topology**Note to Figure 7-15:**


- (1) To minimize the reflections and parallel impedance discontinuity seen by the signal, place the trace split close to the FPGA device. Keep TL2 short so that the FPGA inputs appear as a lumped load.



For more information about $\times 36$ emulated modes, refer to the "Exceptions for $\times 36$ Emulated QDR II and QDR II+ SRAM Interfaces in Arria II GX, Stratix III, and Stratix IV Devices" section in the *Planning Pin and Resource* chapter.

PCB Layout Guidelines

Table 7-4 summarizes QDR II and QDR II SRAM general routing layout guidelines.

 The following layout guidelines include several +/- length based rules. These length based guidelines are for first order timing approximations if you cannot simulate the actual delay characteristics of your PCB implementation. They do not include any margin for crosstalk.


 Altera recommends that you get accurate time base skew numbers when you simulate your specific implementation.

Table 7-4. QDR II and QDR II+ SRAM Layout Guidelines (Part 1 of 2)

Parameter	Guidelines
Impedance	<ul style="list-style-type: none"> ■ All signal planes must be 50 Ω, single-ended, $\pm 10\%$. ■ All signal planes must be 100 Ω, differential $\pm 10\%$. ■ Remove all unused via pads, because they cause unwanted capacitance.
Decoupling Parameter	<ul style="list-style-type: none"> ■ Use 0.1 μF in 0402 size to minimize inductance. ■ Make V_{TT} voltage decoupling close to pull-up resistors. ■ Connect decoupling caps between V_{TT} and ground. ■ Use a 0.1 μF cap for every other V_{TT} pin. ■ Verify your capacitive decoupling using the Altera Power Distribution Network (PDN) Design tool.
Power	<ul style="list-style-type: none"> ■ Route GND, 1.5 V/1.8 V as planes. ■ Route V_{CCIO} for memories in a single split plane with at least a 20-mil (0.020 inches or 0.508 mm) gap of separation. ■ Route V_{TT} as islands or 250-mil (6.35-mm) power traces. ■ Route all oscillators and PLL power as islands or 100-mil (2.54-mm) power traces.
General Routing	<ul style="list-style-type: none"> ■ All specified delay matching requirements include PCB trace delays, different layer propagation, velocity variance, and crosstalk. To minimize PCB layer propagation variance, Altera recommends that signals from the same net group always be routed on the same layer. If signals of the same net group must be routed on different layers with the same impedance characteristic, you must simulate your worst case PCB trace tolerances to ascertain actual propagation delay differences. Typical later to later trace delay variations are of 15 ps/inch order. ■ Use 45° angles (not 90° corners). ■ Avoid T-Junctions for critical nets or clocks. ■ Avoid T-junctions greater than 150 ps (approximately 500 mils, 12.7 mm). ■ Disallow signals across split planes. ■ Restrict routing other signals close to system reset signals. ■ Avoid routing memory signals closer than 0.025 inch (0.635 mm) to PCI or system clocks.

Table 7-4. QDR II and QDR II+ SRAM Layout Guidelines (Part 2 of 2)

Parameter	Guidelines
Clock Routing	<ul style="list-style-type: none"> ■ Route clocks on inner layers with outer-layer run lengths held to under 150 ps (approximately 500 mils, 12.7 mm). ■ These signals should maintain a 10-mil (0.254 mm) spacing from other nets. ■ Clocks should maintain a length-matching between clock pairs of ± 5 ps or approximately ± 25 mils (0.635 mm). ■ Complementary clocks should maintain a length-matching between P and N signals of ± 2 ps or approximately ± 10 mils (0.254 mm). ■ Keep the distance from the pin on the QDR II SRAM component to stub termination resistor (V_{TT}) to less than 50 ps (approximately 250 mils, 6.35 mm) for the κ, $\kappa\#$ clocks. ■ Keep the distance from the pin on the QDR II SRAM component to fly-by termination resistor (V_{TT}) to less than 100 ps (approximately 500 mils, 12.7 mm) for the κ, $\kappa\#$ clocks. ■ Keep the distance from the pin on the FPGA component to stub termination resistor (V_{TT}) to less than 50 ps (approximately 250 mils, 6.35 mm) for the echo clocks, C_Q, $C_Q\#$, if they require an external discrete termination. ■ Keep the distance from the pin on the FPGA component to fly-by termination resistor (V_{TT}) to less than 100 ps (approximately 500 mils, 12.7 mm) for the echo clocks, C_Q, $C_Q\#$, if they require an external discrete termination.
External Memory Routing Rules	<ul style="list-style-type: none"> ■ Keep the distance from the pin on the QDR II SRAM component to stub termination resistor (V_{TT}) to less than 50 ps (approximately 250 mils, 6.35 mm) for the write data, byte write select and address/command signal groups. ■ Keep the distance from the pin on the QDR II SRAM component to fly-by termination resistor (V_{TT}) to less than 100 ps (approximately 500 mils, 12.7 mm) for the write data, byte write select and address/command signal groups. ■ Keep the distance from the pin on the FPGA (Arria II GX) to stub termination resistor (V_{TT}) to less than 50 ps (approximately 250 mils, 6.35 mm) for the read data signal group. ■ Keep the distance from the pin on the FPGA (Arria II GX) to fly-by termination resistor (V_{TT}) to less than 100 ps (approximately 500 mils, 12.7 mm) for the read data signal group. ■ Parallelism rules for the QDR II SRAM data/address/command groups are as follows: <ul style="list-style-type: none"> ■ 4 mils for parallel runs < 0.1 inch (approximately 1\times spacing relative to plane distance). ■ 5 mils for parallel runs < 0.5 inch (approximately 1\times spacing relative to plane distance). ■ 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2\times spacing relative to plane distance). ■ 15 mils for parallel runs between 1.0 and 6.0 inch (approximately 3\times spacing relative to plane distance).
Maximum Trace Length	<ul style="list-style-type: none"> ■ Keep the maximum trace length of all signals from the FPGA to the QDR II SRAM components to 6 inches.

Using the layout guidelines in [Table 7-4](#), Altera recommends the following layout approach:

1. Route the $\kappa/\kappa\#$ clocks and set the clocks as the target trace propagation delays for the output signal group.
2. Route the write data output signal group (write data, byte write select), ideally on the same layer as the $\kappa/\kappa\#$ clocks, to within ± 10 ps skew of the $\kappa/\kappa\#$ traces.

3. Route the address/control output signal group (address, RPS, WPS), ideally on the same layer as the $K/K\#$ clocks, to within ± 20 ps skew of the $K/K\#$ traces.
4. Route the $CQ/CQ\#$ clocks and set the clocks as the target trace propagation delays for the input signal group.
5. Route the read data output signal group (read data), ideally on the same layer as the $CQ/CQ\#$ clocks, to within ± 10 ps skew of the $CQ/CQ\#$ traces.
6. The output and input groups do not need to have the same propagation delays, but they must have all the signals matched closely within the respective groups.

Table 7-5 and Table 7-6 list the typical margins for QDR II and QDR II+ SRAM interfaces, with the assumption that there is zero skew between the signal groups.

Table 7-5. Typical Worst Case Margins for QDR II SRAM Interfaces of Burst Length 2

Device	Speed Grade	Frequency (MHz)	Typical Margin Address/Command (ps)	Typical Margin Write Data (ps)	Typical Margin Read Data (ps)
Arria II GX	I5	250	± 240	± 80	± 170
Arria II GX x36 emulated	I5	200	± 480	± 340	± 460
Stratix IV	—	350	—	—	—
Stratix IV x36 emulated	C2	300	± 320	± 170	± 340

Table 7-6. Typical Worst Case Margins for QDR II+ SRAM Interfaces of Burst Length 4

Device	Speed Grade	Frequency (MHz)	Typical Margin Address/Command (ps) ⁽¹⁾	Typical Margin Write Data (ps)	Typical Margin Read Data (ps)
Arria II GX	I5	250	± 810	± 150	± 130
Arria II GX x36 emulated	I5	200	± 1260	± 410	± 420
Stratix IV	C2	400	± 550	± 10	± 80
Stratix IV x36 emulated	C2	300	± 860	± 180	± 300

Note to Table 7-6:

(1) The QDR II+ SRAM burst length of 4 designs have greater margins on the address signals because they are single data rate.

Other devices and speed grades typically show higher margins than the ones in Table 7-5 and Table 7-6.



Altera recommends that you create your project with a fully implemented QDR II or QDR II+ SRAM Controller with UniPHY interface, and observe the interface timing margins to determine the actual margins for your design.

Although the recommendations in this chapter are based on simulations, you can apply the same general principles when determining the best termination scheme, drive strength setting, and loading style to any board designs. Even armed with this knowledge, it is still critical that you perform simulations, either using IBIS or HSPICE models, to determine the quality of signal integrity on your designs.

Document Revision History

Table 7-7 lists the revision history for this document.

Table 7-7. Document Revision History

Date	Version	Changes
November 2011	4.0	Added Arria V information.
June 2011	3.0	Added Stratix V information.
December 2010	2.0	Maintenance update.
July 2010	1.0	Initial release.