


Ensuring that your external memory interface meets the various timing requirements of today's high-speed memory devices can be a challenge. Altera addresses this challenge by offering external memory physical layer (PHY) interface IPs—ALTMEMPHY and UniPHY, which employ a combination of source-synchronous and self-calibrating circuits to maximize system timing margins. This PHY interface is a plug-and-play solution that the Quartus® II TimeQuest Timing Analyzer timing constrains and analyzes. The ALTMEMPHY and UniPHY IP, and the numerous device features offered by Arria® II, Arria V, Cyclone® III, Cyclone IV, Cyclone V, Stratix® III, Stratix IV, and Stratix V FPGAs, greatly simplifies the implementation of an external memory interface. All the information presented in this document for Stratix III and Stratix IV devices is applicable to HardCopy® III and HardCopy IV devices, respectively.

This chapter details the various timing paths that determine overall external memory interface performance, and describes the timing constraints and assumptions that the PHY IP uses to analyze these paths.

 This chapter focuses on timing constraints for external memory interfaces based on the ALTMEMPHY and UniPHY IP. For information about timing constraints and analysis of external memory interfaces and other source-synchronous interfaces based on the ALTDQ_DQS and ALTDQ_DQS2 megafunctions, refer to [AN 433: Constraining and Analyzing Source-Synchronous Interfaces](#) and the [Quartus II TimeQuest Timing Analyzer](#) chapter in volume 3 of the *Quartus II Handbook*.


External memory interface timing analysis is supported only by the TimeQuest Timing Analyzer, for the following reasons:

- The wizard-generated timing constraint scripts only support the TimeQuest analyzer.
- The Classic Timing Analyzer does not offer analysis of source-synchronous outputs. For example, write data, address, and command outputs.
- The Classic Timing Analyzer does not support detailed rise and fall delay analysis.

The performance of an FPGA interface to an external memory device is dependent on the following items:

- Read datapath timing
- Write datapath timing
- Address and command path timing
- Clock to strobe timing (t_{DQSS} in DDR and DDR2 SDRAM, and $t_{KH\#H}$ in QDR II and QDR II+ SRAM)

- Read resynchronization path timing (applicable for DDR, DDR2, and DDR3 SDRAM in Arria II, Arria V, Stratix III, Stratix IV, and Stratix V devices)
- Read postamble path timing (applicable for DDR and DDR2 SDRAM in Stratix II devices)
- Write leveling path timing (applicable for DDR3 SDRAM with ALTMEMPHY and DDR2 and DDR3 SDRAM with UniPHY)
- PHY timing paths between I/O element and core registers
- PHY and controller internal timing paths (core f_{MAX} and reset recovery/removal)
- I/O toggle rate
- Output clock specifications
- Bus turnaround timing (applicable for RLDRAM II and DDR2 and DDR3 SDRAM with UniPHY)

 External memory interface performance depends on various timing components, and overall system level performance is limited by performance of the slowest link (that is, the path with the smallest timing margins).

Memory Interface Timing Components


There are several categories of memory interface timing components, including source-synchronous timing paths, calibrated timing paths, internal FPGA timing paths, and other FPGA timing parameters.

Understanding the nature of timing paths enables you to use an appropriate timing analysis methodology and constraints. The following section examines these aspects of memory interface timing paths.

Source-Synchronous Paths

These are timing paths where clock and data signals pass from the transmitting device to the receiving device.

An example of such a path is the FPGA-to-memory write datapath. The FPGA device transmits DQ output data signals to the memory along with a center-aligned DQS output strobe signal. The memory device uses the DQS signal to clock the data on the DQ pins into its internal registers.

 For brevity, the remainder of this chapter refers to data signals and strobe and clock signals as DQ signals and DQS signals, respectively. While the terminology is formally correct only for DDR-type interfaces and does not match QDR II, QDR II+ and RLDRAM II pin names, the behavior is similar enough that most timing properties and concepts apply to both. The clock that captures address and command signals is always referred to as CK/CK# too.

Calibrated Paths

These are timing paths where the clock used to capture data is dynamically positioned within the data valid window (DVW) to maximize timing margin.

For Arria II FPGAs interfacing with a DDR2 and DDR3 SDRAM controller with ALTMEMPHY IP, the resynchronization of read data from the DQS-based capture registers to the FPGA system clock domain is implemented using a self-calibrating circuit. On initialization, the sequencer block analyzes all path delays between the read capture and resynchronization registers to set up the resynchronization clock phase for optimal timing margin.

In Cyclone III and Cyclone IV FPGAs, the ALTMEMPHY IP performs the initial data capture from the memory device using a self-calibrating circuit. The ALTMEMPHY IP does not use the DQS strobes from the memory for capture; instead, it uses a dynamic PLL clock signal to capture DQ data signals into core LE registers.

For UniPHY-based controllers, the sequencer block analyzes all path delays between the read capture registers and the read FIFO buffer to set up the FIFO write clock phase for optimal timing margin. The read postamble calibration process is implemented in a similar manner to the read resynchronization calibration. In addition, the sequencer block calibrates a read data valid signal to the delay between a controller issuing a read command and read data returning to controller.

In DDR2 and DDR3 SDRAM and RLDRAM II with UniPHY, the UniPHY IP calibrates the write-leveling chains and programmable output delay chain to align the DQS edge with the CK edge at memory to meet the t_{DQSS} , t_{DSS} , and t_{DSH} specifications.

UniPHY IP enables the dynamic deskew calibration with NIOS sequencer for read and write paths. Dynamic deskew process uses the programmable delay chains that exist within the read and write data paths to adjust the delay of each DQ and DQS pin to remove the skew between different DQ signals and to centre-align the DQS strobe in the DVW of the DQ signals. This process occurs at power up for the read and the write paths.

Internal FPGA Timing Paths

Other timing paths that have an impact on memory interface timing include FPGA internal f_{MAX} paths for PHY and controller logic. This timing analysis is common to all FPGA designs. With appropriate timing constraints on the design (such as clock settings), the TimeQuest Timing Analyzer reports the corresponding timing margins.





For more information about the TimeQuest Timing Analyzer, refer to the [Quartus II TimeQuest Timing Analyzer](#) chapter in volume 3 of the *Quartus II Handbook*.

Other FPGA Timing Parameters

Some FPGA data sheet parameters, such as I/O toggle rate and output clock specifications, can limit memory interface performance.

I/O toggle rates vary based on speed grade, loading, and I/O bank location—top/bottom versus left/right. This toggle rate is also a function of the termination used (OCT or external termination) and other settings such as drive strength and slew rate.

-  Ensure you check the I/O performance in the overall system performance calculation. Altera recommends that you perform signal integrity analysis for the specified drive strength and output pin load combination.
-  For information about signal integrity, refer to the board design guidelines chapters and *AN 476: Impact of I/O Settings on Signal Integrity in Stratix III Devices*.

Output clock specifications include clock period jitter, half-period jitter, cycle-to-cycle jitter, and skew between FPGA clock outputs. You can obtain these specifications from the FPGA data sheet and must meet memory device requirements. You can use these specifications to determine the overall data valid window for signals transmitted between the memory and FPGA device.

FPGA Timing Paths

This topic describes the FPGA timing paths, the timing constraints examples, and the timing assumptions that the constraint scripts use.

In Arria II, Arria V, Stratix III, Stratix IV, and Stratix V devices, the interface margin is reported based on a combination of the TimeQuest Timing Analyzer and further steps to account for calibration that occurs at runtime. First the TimeQuest analyzer returns the base setup and hold slacks, and then further processing adjusts the slacks to account for effects which cannot be modeled in TimeQuest.

Arria II Device PHY Timing Paths

Table 10-1 lists all Arria II devices external memory interface timing paths.

Table 10-1. Arria II Devices External Memory Interface Timing Paths ⁽¹⁾ (Part 1 of 2)

Timing Path	Circuit Category	Source	Destination
Read Data ^{(2), (7)}	Source-Synchronous	Memory DQ, DQS Pins	DQ Capture Registers in IOE
Write Data ^{(2), (7)}	Source-Synchronous	FPGA DQ, DQS Pins	Memory DQ, DM, and DQS Pins
Address and command ⁽²⁾	Source-Synchronous	FPGA CK/CK# and Addr/Cmd Pins	Memory Input Pins
Clock-to-Strobe ⁽²⁾	Source-Synchronous	FPGA CK/CK# and DQS Output Pins	Memory Input Pins
Read Resynchronization ^{(2), (3)}	Calibrated	IOE Capture Registers	IOE Resynchronization Registers
Read Resynchronization ^{(2), (6)}	Calibrated	IOE Capture Registers	Read FIFO in FPGA Core
PHY IOE-Core Paths ^{(2), (3)}	Source-Synchronous	IOE Resynchronization Registers	FIFO in FPGA Core
PHY and Controller Internal Paths ⁽²⁾	Internal Clock f_{MAX}	Core Registers	Core Registers
I/O Toggle Rate ⁽⁴⁾	I/O	FPGA Output Pin	Memory Input Pins

Table 10–1. Arria II Devices External Memory Interface Timing Paths ⁽¹⁾ (Part 2 of 2)

Timing Path	Circuit Category	Source	Destination
Output Clock Specifications (Jitter, DCD) ⁽⁵⁾	I/O	FPGA Output Pin	Memory Input Pins

Notes to Table 10–1:

- (1) Timing paths applicable for an interface between Arria II devices and SDRAM component.
- (2) Timing margins for this path are reported by the TimeQuest Timing Analyzer Report DDR function.
- (3) Only for ALTMEMPHY megafunctions.
- (4) Altera recommends that you perform signal integrity simulations to verify I/O toggle rate.
- (5) For output clock specifications, refer to the *Arria II Device Data Sheet* chapter of the *Arria II Handbook*.
- (6) Only for UniPHY IP.
- (7) Arria II GX devices use source-synchronous and calibrated path.

Figure 10–1 shows the Arria II GX devices input datapath registers and circuit types.


 UniPHY IP interfaces bypass the synchronization registers.

Figure 10–1. Arria II GX Devices Input Data Path Registers and Circuit Types in SDRAM Interface

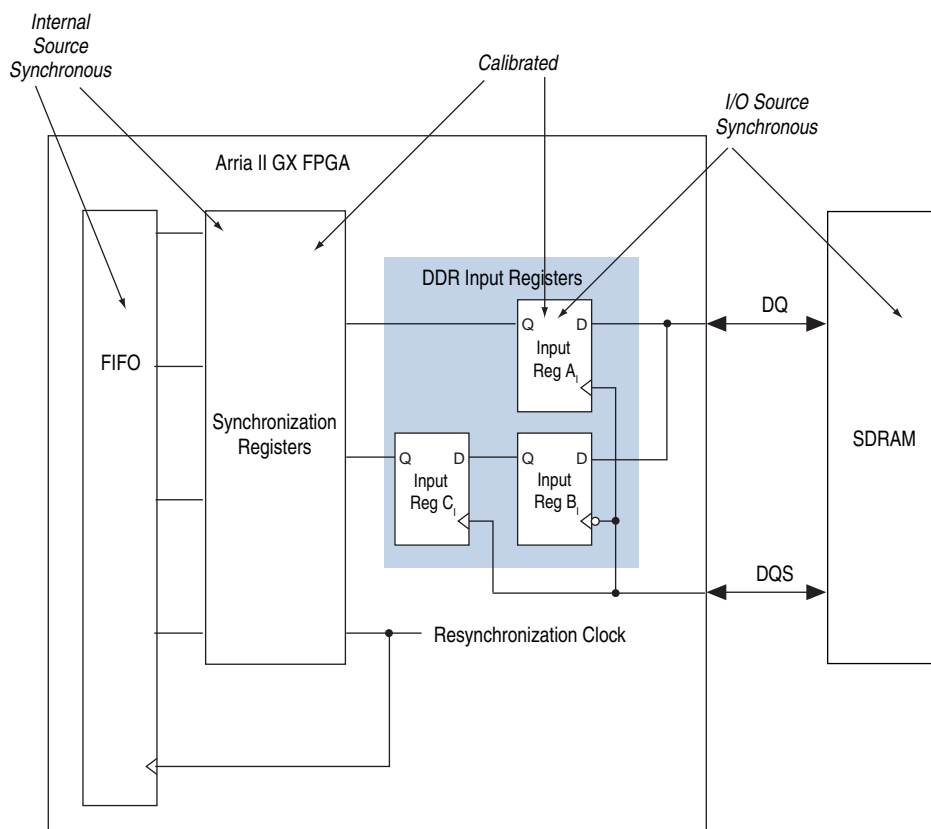
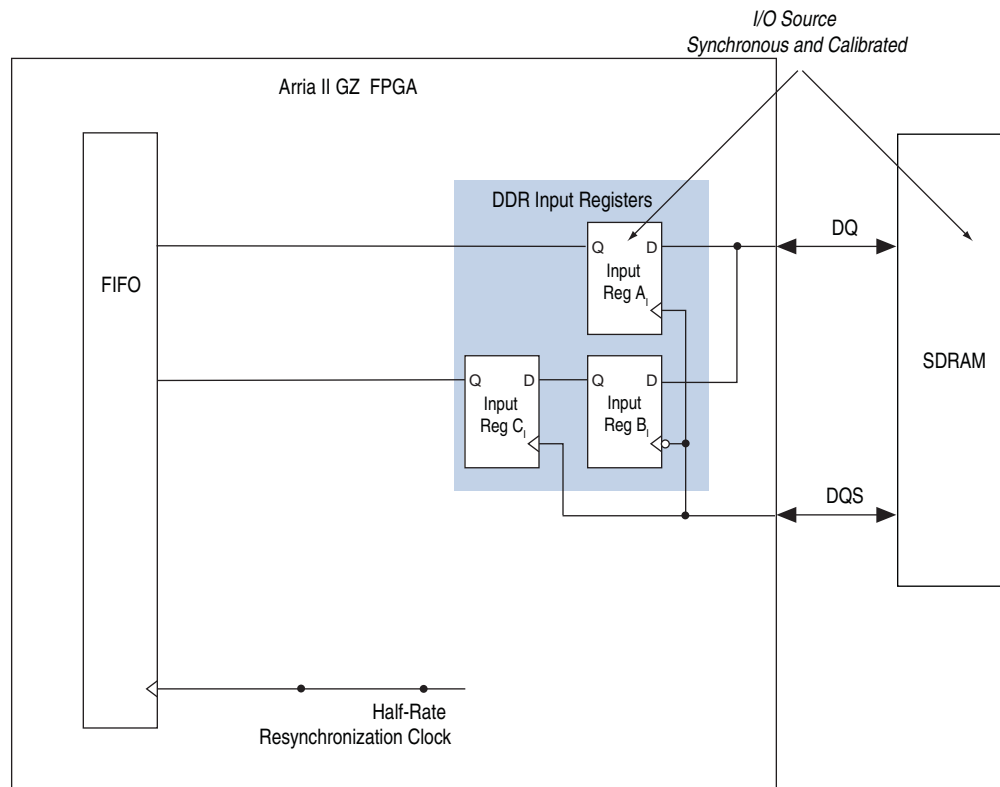


Figure 10-2 shows the Arria II GZ devices input datapath registers and circuit types.

Figure 10-2. Arria II GZ Devices Input Data Path Registers and Circuit Types in SDRAM Interface



Stratix III and Stratix IV PHY Timing Paths

A closer look at all the register transfers occurring in the Stratix III and Stratix IV input datapath reveals many source-synchronous and calibrated circuits.


-  The information in Figure 10-3 and Table 10-2 are based on Stratix IV devices, but they are applicable to Stratix III devices.

Figure 10-3 shows a block diagram of this input path with some of these paths identified for Stratix IV devices. The output datapath contains a similar set of circuits.


 UniPHY IP interfaces bypass the alignment and synchronization registers.

Figure 10-3. Stratix IV Input Path Registers and Circuit Types in SDRAM Interface

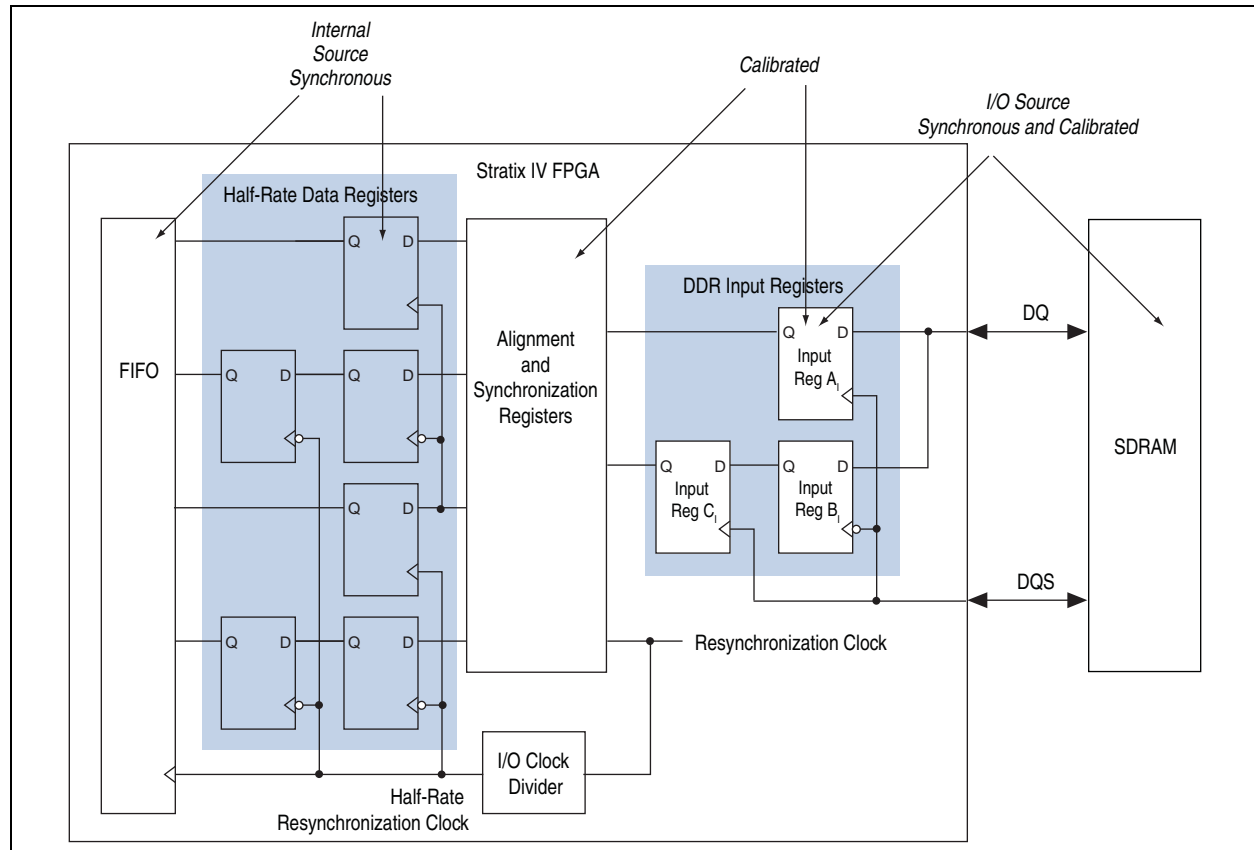


Table 10-2 lists the timing paths applicable for an interface between Stratix IV devices and half-rate SDRAM components.


 The timing paths are also applicable to Stratix III devices, but Stratix III devices use only source-synchronous path for read and write data paths.

Table 10-2. Stratix IV External Memory Interface Timing Paths (Part 1 of 2)

Timing Path	Circuit Category	Source	Destination
Read Data ⁽¹⁾	Source-Synchronous and Calibrated	Memory DQ, DQS Pins	DQ Capture Registers in IOE
Write Data ⁽¹⁾	Source-Synchronous and Calibrated	FPGA DQ, DQS Pins	Memory DQ, DM, and DQS Pins
Address and command ⁽¹⁾	Source-Synchronous	FPGA CK/CK# and Addr/Cmd Pins	Memory Input Pins
Clock-to-Strobe ⁽¹⁾	Source-Synchronous	FPGA CK/CK# and DQS Output Pins	Memory Input Pins

Table 10-2. Stratix IV External Memory Interface Timing Paths (Part 2 of 2)

Timing Path	Circuit Category	Source	Destination
Read Resynchronization (1), (2)	Calibrated	IOE Capture Registers	IOE Alignment and Resynchronization Registers
Read Resynchronization (1), (5)	Calibrated	IOE Capture Registers	Read FIFO in FPGA Core
PHY IOE-Core Paths (1), (2)	Source-Synchronous	IOE Half Data Rate Registers and Half-Rate Resynchronization Clock	FIFO in FPGA Core
PHY & Controller Internal Paths (1)	Internal Clock f_{MAX}	Core registers	Core registers
I/O Toggle Rate (3)	I/O – Data sheet	FPGA Output Pin	Memory Input Pins
Output Clock Specifications (Jitter, DCD) (4)	I/O – Data sheet	FPGA Output Pin	Memory Input Pins

Notes to Table 10-2:

- (1) Timing margins for this path are reported by the TimeQuest Timing Analyzer Report DDR function.
- (2) Only for ALTMEMPHY megafunctions.
- (3) Altera recommends that you perform signal integrity simulations to verify I/O toggle rate.
- (4) For output clock specifications, refer to the *DC and Switching Characteristics* chapter of the *Stratix IV Device Handbook*.
- (5) Only for UniPHY IP.

Arria V, Cyclone V, and Stratix V Timing paths

Figure 10-4 shows a block diagram of the Stratix V input data path.

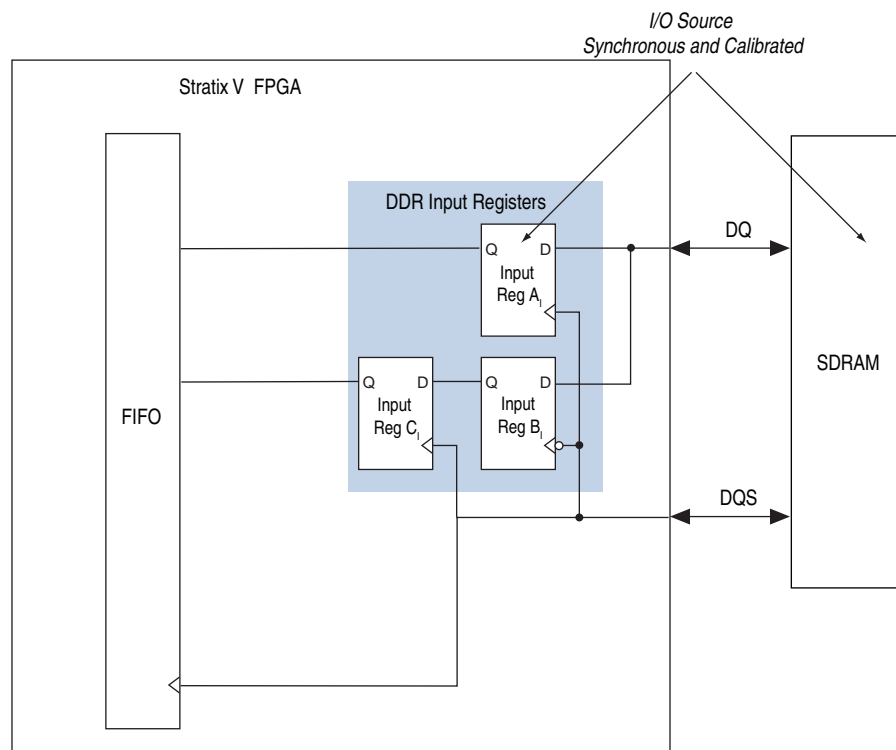
Figure 10-4. Arria V, Cyclone V, and Stratix V Input Data Path

Table 10-3 lists all Stratix V devices external memory interface timing paths.

Table 10-3. Stratix V External Memory Interface Timing Paths ⁽¹⁾

Timing Path	Circuit Category	Source	Destination
Read Data ⁽²⁾	Source-Synchronous and Calibrated	Memory DQ, DQS Pins	DQ Capture Registers in IOE
Write Data ⁽²⁾	Source-Synchronous and Calibrated	FPGA DQ, DM, DQS Pins	Memory DQ, DM, and DQS Pins
Address and command ⁽²⁾	Source-Synchronous	FPGA CK/CK# and Addr/Cmd Pins	Memory Input Pins
Clock-to-Strobe ⁽²⁾	Source-Synchronous	FPGA CK/CK# and DQS Output Pins	Memory Input Pins
Read Resynchronization ⁽²⁾	Source-Synchronous	IOE Capture Registers	Read FIFO in IOE
PHY & Controller Internal Paths ⁽²⁾	Internal Clock f_{MAX}	Core Registers	Core Registers
i/O Toggle Rate ⁽³⁾	I/O – Data sheet	FPGA Output Pin	Memory Input Pins
Output Clock Specifications (Jitter, DCD) ⁽⁴⁾	I/O – Data sheet	FPGA Output Pin	Memory Input Pins

Notes to Table 10-3:

- (1) This table lists the timing paths applicable for an interface between Arria V, Cyclone V, and Stratix V devices and half-rate SDRAM components.
- (2) Timing margins for this path are reported by the TimeQuest Timing Analyzer Report DDR function.
- (3) Altera recommends that you perform signal integrity simulations to verify I/O toggle rate.
- (4) For output clock specifications, refer to the *DC and Switching Characteristics* chapter of the Stratix V Device Handbook.

Cyclone III and Cyclone IV PHY Timing Paths

Table 10-4 lists the various timing paths in a Cyclone III and Cyclone IV memory interface. Cyclone III and Cyclone IV devices use a calibrated PLL output clock for data capture and ignore the DQS strobe from the memory. Therefore, read resynchronization and postamble timing paths do not apply to Cyclone III and Cyclone IV designs. The read capture is implemented in LE registers specially placed next to the data pin with fixed routing, and data is transferred from the capture clock domain to the system clock domain using a FIFO block. Figure 10-5 shows the Cyclone III and Cyclone IV input datapath registers and circuit types.

Table 10-4. Cyclone III and Cyclone IV SDRAM External Memory Interface Timing Paths ⁽¹⁾ (Part 1 of 2)

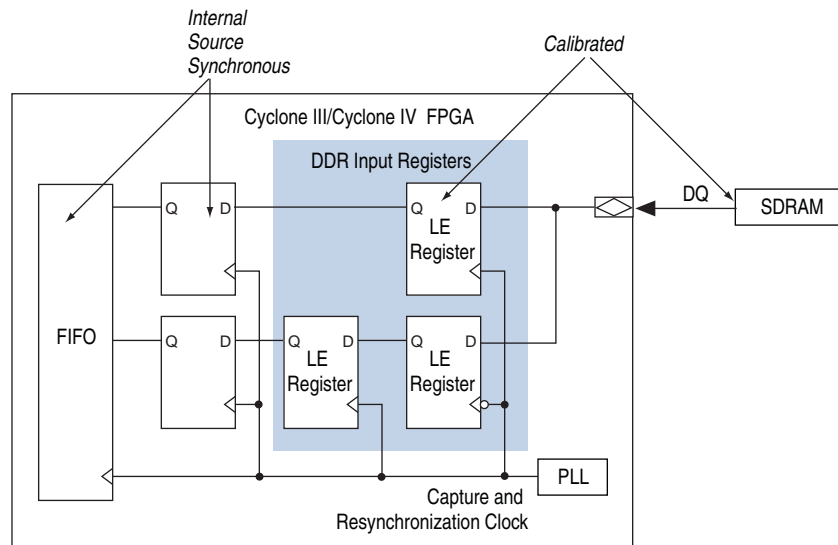
Timing Path	Circuit Category	Source	Destination
Read Data ⁽²⁾	Calibrated	Memory DQ, DQS Pins	FPGA DQ Capture Registers in LEs
Write Data ⁽²⁾	Source-Synchronous	FPGA DQ, DQS Pins	Memory DQ, DM, and DQS Pins
Address and command ⁽²⁾	Source-Synchronous	FPGA CK/CK# and Addr/Cmd Pins	Memory Input Pins
Clock-to-Strobe ⁽²⁾	Source-Synchronous	FPGA CK/CK# and DQS Output Pins	Memory Input Pins
PHY Internal Timing ⁽²⁾	Internal Clock f_{MAX}	LE Half Data Rate Registers	FIFO in FPGA Core
I/O Toggle Rate ⁽³⁾	I/O – Data sheet I/O Timing section	FPGA Output Pin	Memory Input Pins

Table 10-4. Cyclone III and Cyclone IV SDRAM External Memory Interface Timing Paths ⁽¹⁾ (Part 2 of 2)

Timing Path	Circuit Category	Source	Destination
Output Clock Specifications (Jitter, DCD) ⁽⁴⁾	I/O – Data sheet <i>Switching Characteristics</i> section	FPGA Output Pin	Memory Input Pins

Notes to Table 10-4:

- (1) Table 10-4 lists the timing paths applicable for an interface between Cyclone III and Cyclone IV devices and SDRAM.
- (2) Timing margins for this path are reported by the TimeQuest Timing Analyzer Report DDR function.
- (3) Altera recommends that you perform signal integrity simulations to verify I/O toggle rate.
- (4) For output clock specifications, refer to the *DC and Switching Characteristics* chapter of the *Cyclone III Device Handbook* and of the *Cyclone IV Device Handbook*

Figure 10-5. Cyclone III or Cyclone IV Input Data Path Registers and Circuit Types in SDRAM Interface

Timing Constraint and Report Files

The timing constraints differ for the ALTMEMPHY megafunction and the UniPHY IP.

ALTMEMPHY Megafunction

To ensure a successful external memory interface operation, the ALTMEMPHY MegaWizard™ Plug-In Manager generates the following files for timing constraints and reporting scripts:

- `<variation_name>phy_dds_timing.sdc`
- `<variation_name>phy_dds_timing.tcl` (except Cyclone III devices)
- `<variation_name>phy_report_timing.tcl`
- `<variation_name>phy_report_timing_core.tcl` (except Cyclone III devices)
- `<variation_name>phy_dds_pins.tcl`

<variation_name>_ddr_timing.sdc

The Synopsys Design Constraints File (**.sdc**) has the name **<controller_variation_name>_phy_ddr_timing.sdc** when you instantiate the ALTMEMPHY megafunction in the Altera® memory controller, and has the name **<phy_variation_name>_ddr_timing.sdc** when you instantiate the ALTMEMPHY megafunction as a stand-alone design.

To analyze the timing margins for all ALTMEMPHY megafunction timing paths, execute the Report DDR function in the TimeQuest Timing Analyzer; refer to the [“Timing Analysis Description” on page 10–13](#). No timing constraints are necessary (or specified in the **.sdc**) for Arria II GX devices read capture and write datapaths, because all DQ and DQS pins are predefined. The capture and output registers are built into the IOE, and the signals are using dedicated routing connections. Timing constraints have no impact on the read and write timing margins. However, the timing margins for these paths are analyzed using FPGA data sheet specifications and the user-specified memory data sheet parameters.

The ALTMEMPHY megafunction uses the following **.sdc** constraints for internal FPGA timing paths, address and command paths, and clock-to-strobe timing paths:

- Creating clocks on PLL inputs
- Creating generated clocks using `derive_pll_clocks`, which includes all full-rate and half-rate PLL outputs, PLL reconfiguration clock, and I/O scan clocks
- Calling `derive_clock_uncertainty`
- Cutting timing paths for DDR I/O, calibrated paths, and most reset paths
- Setting output delays on address and command outputs (versus CK/CK# outputs)
- Setting 2T or two clock-period multicycle setup for all half-rate address and command outputs, except nCS and on-die termination (ODT) (versus CK/CK# outputs)
- Setting output delays on DQS strobe outputs (versus CK/CK# outputs for DDR2 and DDR SDRAM)



The high-performance controller MegaWizard Plug-In Manager generates an extra **<variation_name>_example_top.sdc** for the example driver design. This file contains the timing constraints for the non-DDR specific parts of the project.

<variation_name>_ddr_timing.tcl

This script includes the memory interface and FPGA device timing parameters for your variation. It is included within **<variation_name>_report_timing.tcl** and **<variation_name>_ddr_timing.sdc** and runs automatically during compilation. This script is run for every instance of the same variation. Cyclone III devices do not have this **.tcl** file. All the parameters are in the **.sdc**.

<variation_name>_report_timing.tcl

This script reports the timing slacks for your variation. It runs automatically during compilation. You can also run this script with the Report DDR task in the TimeQuest Timing Analyzer window. This script is run for every instance of the same variation.

<variation_name>_report_timing_core.tcl

This script contains high-level procedures that *<variation_name>_report_timing.tcl* uses to compute the timing slacks for your variation. It runs automatically during compilation. Cyclone III devices do not have this .tcl file.

<variation_name>_ddr_pins.tcl

This script includes all the functions and procedures required by the *<variation_name>_report_timing.tcl* and *<variation_name>_ddr_timing.sdc* scripts. It is a library of useful functions to include at the top of an .sdc. It finds all the variation instances in the design and the associated clock, register, and pin names of each instance. The results are saved in the same directory as the .sdc and *<variation_name>_report_timing.tcl* as *<variation_name>_autodetectedpins.tcl*.



Because this .tcl file traverses the design for the project pin names, you do not need to keep the same port names on the top level of the design.

UniPHY IP

To ensure a successful external memory interface operation, the UniPHY IP generates two sets of files for timing constraints but in different folders and with slightly different filenames. One set of files are used for synthesis project, which is available under the *<variation_name>* folder located in the main project folder while the other set of files are the example designs, located in the *<variation_name>example design\example_project* folder.

The project folders contain the following files for timing constraints and reporting scripts:

- *<variation_name>.sdc*
- *<variation_name>_timing.tcl*
- *<variation_name>_report_timing.tcl*
- *<variation_name>_report_timing_core.tcl*
- *<variation_name>_pin_map.tcl*
- *<variation_name>_parameters.tcl*

<variation_name>.sdc

The *<variation_name>.sdc* is listed in the wizard-generated Quartus II IP File (.qip). Including this file in the project allows the Quartus II Synthesis and Fitter to use the timing driven compilation to optimize the timing margins.

To analyze the timing margins for all UniPHY timing paths, execute the Report DDR function in the TimeQuest Timing Analyzer.

The UniPHY IP uses the .sdc to constrain internal FPGA timing paths, address and command paths, and clock-to-strobe timing paths, and more specifically:

- Creating clocks on PLL inputs
- Creating generated clocks
- Calling `derive_clock_uncertainty`

- Cutting timing paths for specific reset paths
- Setting input and output delays on DQ inputs and outputs
- Setting output delays on address and command outputs (versus CK/CK# outputs)

<variation_name>_timing.tcl

This script includes the memory, FPGA, and board timing parameters for your variation. It is included within *<variation_name>_report_timing.tcl* and *<variation_name>.sdc*. In multiple interface designs with PLL and DLL sharing, you must change the master core name and instance name in this file for the slave controller.

<variation_name>_report_timing.tcl

This script reports the timing slack for your variation. It runs automatically during compilation (during static timing analysis). You can also run this script with the Report DDR task in the TimeQuest Timing Analyzer. This script is run for every instance of the same variation.

<variation_name>_report_timing_core.tcl

This script contains high-level procedures that the *<variation_name>_report_timing.tcl* script uses to compute the timing slack for your variation. This script runs automatically during compilation.

<variation_name>_pin_map.tcl

This script is a library of functions and procedures that the *<variation_name>_report_timing.tcl* and *<variation_name>.sdc* scripts use. The *<variation_name>_pin_assignments.tcl* script, which is not relevant to timing constraints, also uses this library.

<variation_name>_parameters.tcl

This script defines some of the parameters that describe the geometry of the core and the PLL configuration. Do not change this file, except when you modify the PLL through the MegaWizard Plug-In Manager. In this case, the changes to the PLL parameters do not automatically propagate to this file and you must manually apply those changes in this file.

Timing Analysis Description

The following sections describe the timing analysis using the respective FPGA data sheet specifications and the user-specified memory data sheet parameters.

For detailed timing analysis description, refer to the scripts listed in [“Timing Constraint and Report Files”](#) on page 10-10.

To account for the effects of calibration, the ALTMEMPHY and UniPHY IP include additional scripts that are part of the *<phy_variation_name>_report_timing.tcl* and *<phy_variation_name>_report_timing_core.tcl* files that determine the timing margin after calibration. These scripts use the setup and hold slacks of individual pins to emulate what is occurring during calibration to obtain timing margins that are

representative of calibrated PHYs. The effects considered as part of the calibrated timing analysis include improvements in margin because of calibration, and quantization error and calibration uncertainty because of voltage and temperature changes after calibration. The calibration effects do not apply to Stratix III and Cyclone III devices.

Address and Command

Address and command signals are single data rate signals latched by the memory device using the FPGA output clock. Some of the address and command signals are half-rate data signals, while others, such as the chip select, are full-rate signals. The TimeQuest Timing Analyzer analyzes the address and command timing paths using the `set_output_delay` (max and min) constraints.

PHY or Core

Timing analysis of the PHY or core path includes the path of soft registers in the device and the register in the I/O element. However, the analysis does not include the paths through the pin or the calibrated path. The PHY or core analyzes this path by calling the `report_timing` command in `<variation_name>_report_timing.tcl` and `<variation_name>_report_timing_core.tcl`.

PHY or Core Reset

The PHY or core reset is the internal timing of the asynchronous reset signals to the ALTMEMPHY or UniPHY IPs. The PHY or core analyzes this path by calling the `report_timing` command in `<variation_name>_report_timing.tcl` and `<variation_name>_report_timing_core.tcl`.

Read Capture and Write

Cyclone III and Stratix III memory interface designs perform read capture and write timing analysis using the TCCS and SW timing specification. Read capture and write timing analysis for Arria II, Cyclone IV, Stratix IV, and Stratix V memory interface designs are based on the timing slacks obtained from the TimeQuest Timing Analyzer and all the effects included with the Quartus II timing model such as die-to-die and within-die variations, aging, systematic skew, and operating condition variations. Because the PHY IP adjusts the timing slacks to account for the calibration effects, there are two sets of read capture and write timing analysis numbers—**Before Calibration** and **After Calibration**.

Cyclone III and Stratix III

This section details the timing margins, such as the read data and write data timing paths, which the TimeQuest Timing Analyzer callates for Cyclone III and Stratix III designs. Timing paths internal to the FPGA are either guaranteed by design and tested on silicon, or analyzed by the TimeQuest Timing Analyzer using corresponding timing constraints.

- For design guidelines about implementing and analyzing your external memory interface using the PHY in Cyclone III, Stratix III, and Stratix IV devices, refer to the design tutorials on the [List of designs using Altera External Memory IP](#) page of the Altera Wiki website.

Timing margins for chip-to-chip data transfers can be defined as:

$$\text{Margin} = \text{bit period} - \text{transmitter uncertainties} - \text{receiver requirements}$$

where:

- Sum of all transmitter uncertainties = transmitter channel-to-channel skew (TCCS).

The timing difference between the fastest and slowest output edges on data signals, including t_{CO} variation, clock skew, and jitter. The clock is included in the TCCS measurement and serves as the time reference.

- Sum of all receiver requirements = receiver sampling window (SW) requirement.

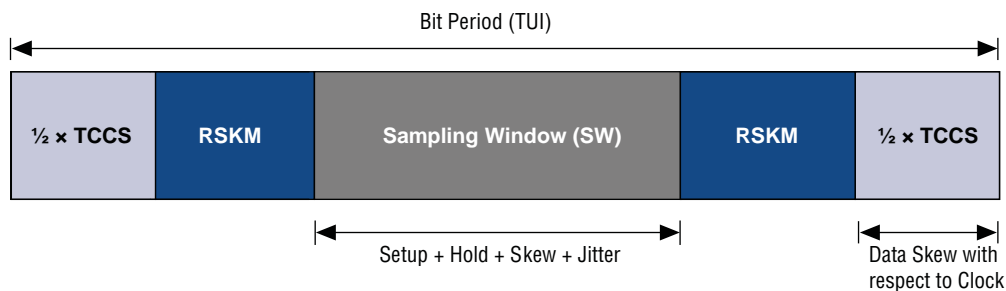
The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.

- Receiver skew margin (RSKM) = margin or slack at the receiver capture register.

- For TCCS and SW specifications, refer to the *DC and Switching Characteristics* chapter of the *Cyclone III Device Handbook* or *Stratix III Device Handbook*.

Figure 10-6 relates this terminology to a timing budget diagram.

Figure 10-6. Sample Timing Budget Diagram



The timing budget regions marked “ $\frac{1}{2} \times \text{TCCS}$ ” represent the latest data valid time and earliest data invalid times for the data transmitter. The region marked sampling window is the time required by the receiver during which data must stay stable. This sampling window comprises the following:

- Internal register setup and hold requirements
- Skew on the data and clock nets within the receiver device
- Jitter and uncertainty on the internal capture clock

- The sampling window is not the capture margin or slack, but instead the requirement from the receiver. The margin available is denoted as RSKM.

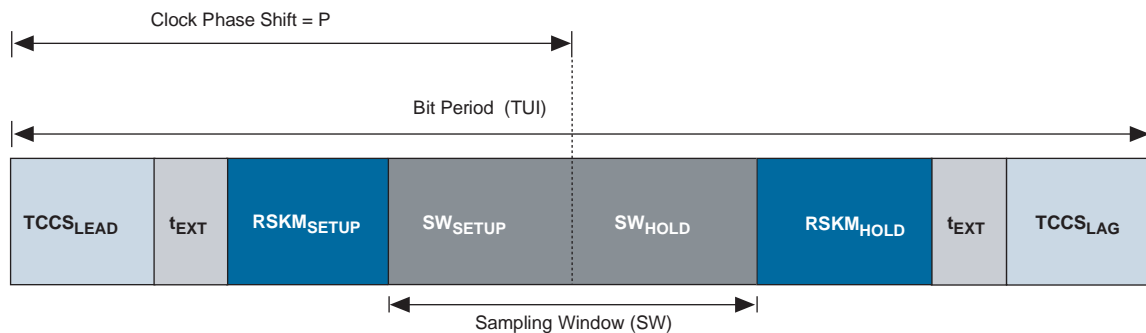
The simple example illustrated in Figure 10-6 does not consider any board level uncertainties, assumes a center-aligned capture clock at the middle of the receiver sampling window region, and assumes an evenly distributed TCCS with respect to the transmitter clock pin. In this example, the left end of the bit period corresponds to time $t = 0$, and the right end of the bit period corresponds to time $t = \text{TUI}$ (where TUI stands for time unit interval). Therefore, the center-aligned capture clock at the receiver is best placed at time $t = \text{TUI}/2$.

Therefore:

$$\text{the total margin} = 2 \times \text{RSKM} = \text{TUI} - \text{TCCS} - \text{SW}.$$

Consider the case where the clock is not center-aligned within the bit period (clock phase shift = P), and the transmitter uncertainties are unbalanced ($\text{TCCS}_{\text{LEAD}} \neq \text{TCCS}_{\text{LAG}}$). $\text{TCCS}_{\text{LEAD}}$ is defined as the skew between the clock signal and latest data valid signal. TCCS_{LAG} is defined as the skew between the clock signal and earliest data invalid signal. Also, the board level skew across data and clock traces are specified as t_{EXT} . For this condition, you should compute independent setup and hold margins at the receiver ($\text{RSKM}_{\text{SETUP}}$ and $\text{RSKM}_{\text{HOLD}}$). In this example, the sampling window requirement is split into a setup side requirement (SW_{SETUP}) and hold side (SW_{HOLD}) requirement. Figure 10-7 illustrates the timing budget for this condition. A timing budget similar to that shown in Figure 10-7 is used for Cyclone III and Stratix III FPGA read and write data timing paths.

Figure 10-7. Sample Timing Budget with Unbalanced (TCCS and SW) Timing Parameters



Therefore:

$$\text{Setup margin} = \text{RSKM}_{\text{SETUP}} = P - \text{TCCS}_{\text{LEAD}} - \text{SW}_{\text{SETUP}} - t_{\text{EXT}}$$

$$\text{Hold margin} = \text{RSKM}_{\text{HOLD}} = (\text{TUI} - P) - \text{TCCS}_{\text{LAG}} - \text{SW}_{\text{HOLD}} - t_{\text{EXT}}$$

The timing budget illustrated in Figure 10-6 with balanced timing parameters applies for calibrated paths where the clock is dynamically center-aligned within the data valid window. The timing budget illustrated in Figure 10-7 with unbalanced timing parameters applies for circuits that employ a static phase shift using a DLL or PLL to place the clock within the data valid window.

Read Capture

Memory devices provide edge-aligned DQ and DQS outputs to the FPGA during read operations. Stratix III FPGAs center-align the DQS strobe using static DLL-based delays, and the Cyclone III FPGAs use a calibrated PLL clock output to capture the read data in LE registers without using DQS. While Stratix III devices use a source synchronous circuit for data capture and Cyclone III devices use a calibrated circuit, the timing analysis methodology is quite similar, as shown in the following section.

When applying this methodology to read data timing, the memory device is the transmitter and the FPGA device is the receiver.

The transmitter channel-to-channel skew on outputs from the memory device is available from the corresponding device data sheet. Let us examine the TCCS parameters for a DDR2 SDRAM component.

For DQS-based capture:

- The time between DQS strobe and latest data valid is defined as t_{DQSQ}
- The time between earliest data invalid and next strobe is defined as t_{QHS}
- Based on earlier definitions, $TCCS_{LEAD} = t_{DQSQ}$ and $TCCS_{LAG} = t_{QHS}$

The sampling window at the receiver, the FPGA, includes several timing parameters:

- Capture register micro setup and micro hold time requirements
- DQS clock uncertainties because of DLL phase shift error and phase jitter
- Clock skew across the DQS bus feeding DQ capture registers
- Data skew on DQ paths from pin to input register including package skew


 For TCCS and SW specifications, refer to the *DC and Switching Characteristics* chapter of the *Cyclone III Device Handbook* or the *Stratix III Device Handbook*.

Figure 10-8 shows the timing budget for a read data timing path.

Figure 10-8. Timing Budget for Read Data Timing Path

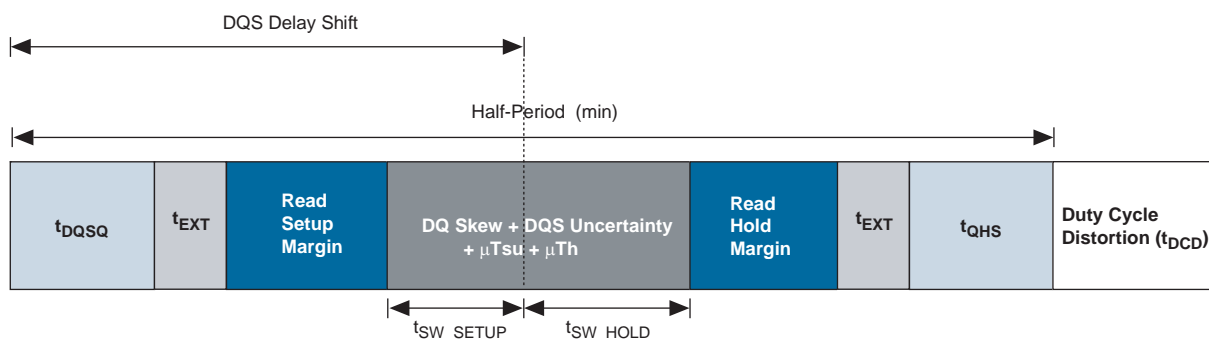


Table 10-5 lists a read data timing analysis for a Stratix III -2 speed-grade device interfacing with a 400-MHz DDR2 SDRAM component.

Table 10-5. Read Data Timing Analysis for Stratix III Device with a 400-MHz DDR2 SDRAM (1)

Parameter	Specifications	Value (ps)	Description
Memory Specifications (1)	t_{HP}	1250	Average half period as specified by the memory data sheet, $t_{HP} = 1/2 * t_{CK}$
	t_{DCD}	50	Duty cycle distortion = $2\% \times t_{CK} = 0.02 \times 2500$ ps
	t_{DQSQ}	200	Skew between DQS and DQ from memory
	t_{QHS}	300	Data hold skew factor as specified by memory
FPGA Specifications	t_{SW_SETUP}	181	FPGA sampling window specifications for a given configuration (DLL mode, width, location, and so on.)
	t_{SW_HOLD}	306	
Board Specifications	t_{EXT}	20	Maximum board trace variation allowed between any two signal traces (user specified parameter)
Timing Calculations	t_{DVW}	710	$t_{HP} - t_{DCD} - t_{DQSQ} - t_{QHS} - 2 \times t_{EXT}$
	$t_{DQS_PHASE_DELAY}$	500	Ideal phase shift delay on DQS capture strobe = (DLL phase resolution \times number of delay stages $\times t_{CK}$) / $360^\circ = (36^\circ \times 2$ stages $\times 2500$ ps) / $360^\circ = 500$ ps
Results	Setup margin	99	$RSKM_{SETUP} = t_{DQS_PHASE_DELAY} - t_{DQSQ} - t_{SW_SETUP} - t_{EXT}$
	Hold margin	74	$RSKM_{HOLD} = t_{HP} - t_{DCD} - t_{DQS_PHASE_DELAY} - t_{QHS} - t_{SW_HOLD} - t_{EXT}$

Notes to Table 10-5:

- (1) This sample calculation uses memory timing parameters from a 72-bit wide 256-MB micron MT9HTF3272AY-80E 400-MHz DDR2 SDRAM DIMM.

Table 10-6 lists a read data timing analysis for a DDR2 SDRAM component at 200 MHz using the SSTL-18 Class II/O standard and termination. A 267-MHz DDR2 SDRAM component is required to ensure positive timing margins for the 200-MHz memory interface clock frequency for the 200 MHz operation.

Table 10-6. Read Data Timing Analysis for a 200-MHz DDR2 SDRAM on a Cyclone III Device (1)

Parameter	Specifications	Value (ps)	Description
Memory Specifications (1)	t_{HP}	2500	Average half period as specified by the memory data sheet
	t_{DCD_TOTAL}	250	Duty cycle distortion = $2\% \times t_{CK} = 0.02 \times 5000$ ps
	t_{AC}	± 500	Data (DQ) output access time for a 267-MHz DDR2 SDRAM component
FPGA Specifications	t_{SW_SETUP}	580	FPGA sampling window specification for a given configuration (interface width, location, and so on).
	t_{SW_HOLD}	550	
Board Specifications (1)	t_{EXT}	20	Maximum board trace variation allowed between any two signal traces (user specified parameter)
Timing Calculations	t_{DVW}	1230	$t_{HP} - t_{DCD} - 2 \times t_{AC} - 2 \times t_{EXT}$
Results	Total margin	100	$t_{DVW} - t_{SW_SETUP} - t_{SW_HOLD}$

Notes to Table 10-6:

- (1) For this sample calculation, total duty cycle distortion and board skew are split over both setup and hold margin. For more information on Cyclone III -6 speed-grade device read capture and timing analysis, refer to "Cyclone III and Cyclone IV PHY Timing Paths" on page 10-9.

Write Capture

During write operations, the FPGA generates a DQS strobe and a center-aligned DQ data bus using multiple PLL-driven clock outputs. The memory device receives these signals and captures them internally. The Stratix III family contains dedicated DDIO (double data rate I/O) blocks inside the IOEs.

For write operations, the FPGA device is the transmitter and the memory device is the receiver. The memory device's data sheet specifies data setup and data hold time requirements based on the input slew rate on the DQ/DQS pins. These requirements make up the memory sampling window, and include all timing uncertainties internal to the memory.

Output skew across the DQ and DQS output pins on the FPGA make up the TCCS specification. TCCS includes contributions from numerous internal FPGA circuits, including:

- Location of the DQ and DQS output pins
- Width of the DQ group
- PLL clock uncertainties, including phase jitter between different output taps used to center-align DQS with respect to DQ
- Clock skew across the DQ output pins, and between DQ and DQS output pins
- Package skew on DQ and DQS output pins

Refer to the *DC and Switching Characteristics* chapter of the *Cyclone III Device Handbook* or the *Stratix III Device Handbook* for TCCS and SW specifications.

Figure 10-9 illustrates the timing budget for a write data timing path.

Figure 10-9. Timing Budget for Write Data Timing Path

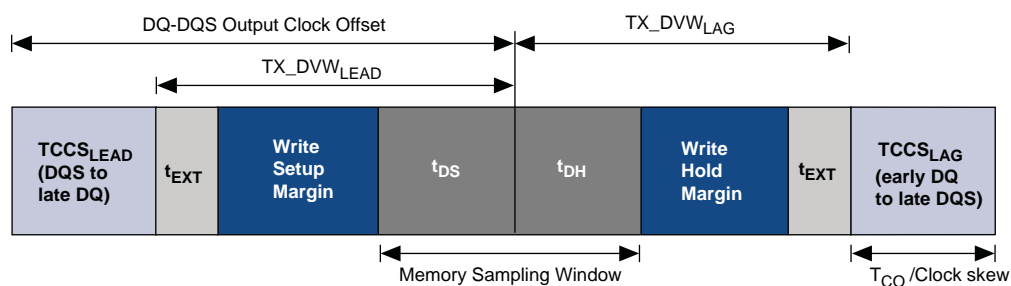


Table 10-7 lists a write data timing analysis for a Stratix III –2 speed-grade device interfacing with a DDR2 SDRAM component at 400 MHz. This timing analysis assumes the use of a differential DQS strobe with 2.0-V/ns edge rates on DQS, and 1.0-V/ns edge rate on DQ output pins. Consult your memory device’s data sheet for derated setup and hold requirements based on the DQ/DQS output edge rates from your FPGA.

Table 10-7. Write Data Timing Analysis for 400-MHz DDR2 SDRAM Stratix III Device ⁽¹⁾

Parameter	Specifications	Value (ps)	Description
Memory Specifications ⁽¹⁾	t_{HP}	1250	Average half period as specified by the memory data sheet
	t_{DSA}	250	Memory setup requirement (derated for DQ/DQS edge rates and V_{REF} reference voltage)
	t_{DHA}	250	Memory hold requirement (derated for DQ/DQS edge rates and V_{REF} reference voltage)
FPGA Specifications	$TCCS_{LEAD}$	229	FPGA transmitter channel-to-channel skew for a given configuration (PLL setting, location, and width).
	$TCCS_{LAG}$	246	
Board Specifications	t_{EXT}	20	Maximum board trace variation allowed between any two signal traces (user specified parameter)
Timing Calculations	$t_{OUTPUT_CLOCK_OFFSET}$	625	Output clock phase offset between DQ & DQS output clocks = 90° . $t_{OUTPUT_CLOCK_OFFSET} = (\text{output clock phase DQ and DQS offset} \times t_{CK})/360^\circ = (90^\circ \times 2500)/360^\circ = 625$
	TX_DVW_{LEAD}	396	Transmitter data valid window = $t_{OUTPUT_CLOCK_OFFSET} - TCCS_{LEAD}$
	TX_DVW_{LAG}	379	Transmitter data valid window = $t_{HP} - t_{OUTPUT_CLOCK_OFFSET} - TCCS_{LAG}$
Results	Setup margin	126	$TX_DVW_{LEAD} - t_{EXT} - t_{DSA}$
	Hold margin	109	$TX_DVW_{LAG} - t_{EXT} - t_{DHA}$

Notes to Table 10-7:

- (1) This sample calculation uses memory timing parameters from a 72-bit wide 256-MB micron MT9HTF3272AY-80E 400-MHz DDR2 SDRAM DIMM

Table 10-8 lists a write timing analysis for a Cyclone III –6 speed-grade device interfacing with a DDR2 SDRAM component at 200 MHz. A 267-MHz DDR2 SDRAM component is used for this analysis.

Table 10-8. Write Data Timing Analysis for a 200-MHz DDR2 SDRAM Interface on a Cyclone III Device ⁽¹⁾ (Part 1 of 2)

Parameter	Specifications	Value (ps)	Description
Memory Specifications	t_{HP}	2500	Average half period as specified by the memory data sheet
	t_{DCD_TOTAL}	250	Total duty cycle distortion = $5\% \times t_{CK} = 0.05 \times 5000$
	t_{DS} (derated)	395	Memory setup requirement from a 267-MHz DDR2 SDRAM component (derated for single-ended DQS and 1 V/ns slew rate)
	t_{DH} (derated)	335	Memory hold from DDR2 267-MHz component (derated for single-ended DQS and 1 V/ns slew rate)
FPGA Specifications	$TCCS_{LEAD}$	790	FPGA TCCS for a given configuration (PLL setting, location, width)
	$TCCS_{LAG}$	380	
Board Specifications	t_{EXT}	20	Maximum board trace variation allowed between any two signal traces (user specified parameter)

Table 10–8. Write Data Timing Analysis for a 200-MHz DDR2 SDRAM Interface on a Cyclone III Device ⁽¹⁾ (Part 2 of 2)

Parameter	Specifications	Value (ps)	Description
Timing Calculations	TX_DVW _{LEAD}	460	Transmitter data valid window = $t_{\text{OUTPUT_CLOCK_OFFSET}} - \text{TCCS}_{\text{LEAD}}$
	TX_DVW _{LAG}	870	Transmitter data valid window = $t_{\text{HP}} - t_{\text{OUTPUT_CLOCK_OFFSET}} - \text{TCCS}_{\text{LAG}}$
	$t_{\text{OUTPUT_CLOCK_OFFSET}}$	1250	Output clock phase offset between DQ/DQS output clocks = 90° $t_{\text{OUTPUT_CLOCK_OFFSET}} = (\text{output clock phase DQ \& DQS offset} \times t_{\text{CK}}) / 360^\circ = (90^\circ \times 5000) / 360^\circ = 1250$
Results	Setup margin	45	$\text{TX_DVW}_{\text{LEAD}} - t_{\text{EXT}} - t_{\text{DS}}$
	Hold margin	265	$\text{TX_DVW}_{\text{LAG}} - t_{\text{EXT}} - t_{\text{DH}} - t_{\text{DCD_TOTAL}}$

Note to Table 10–8:

(1) For more information on Cyclone III –6 speed-grade device read capture and timing analysis, refer to “Read Capture” on page 10–17.

Arria II, Arria V, Cyclone IV, Cyclone V, Stratix IV and Stratix V

Read Capture

Read capture timing analysis indicates the amount of slack on the DDR DQ signals that are latched by the FPGA using the DQS strobe output of the memory device. The read capture timing paths are analyzed by a combination of the TimeQuest Timing Analyzer using the `set_input_delay` (max and min), `set_max_delay`, and `set_min_delay` constraints, and further steps to account for calibration that occurs at runtime. The ALTMEMPHY and UniPHY IP include timing constraints in the `<phy_variation_name>_ddr_timing.sdc` (ALTMEMPHY) or `<phy_variation_name>.sdc` (UniPHY), and further slack analysis in `<phy_variation_name>_report_timing.tcl` and `<phy_variation_name>_report_timing_core.tcl` files.

The PHY IP captures the Cyclone IV devices read data using a PLL phase that is calibrated and tracked with the sequencer. The equations in `<phy_variation_name>_report_timing_core.tcl` ensures optimum read capture timing margin.

In Arria II, Cyclone IV, and Stratix IV devices, the margin is reported based on a combination of the TimeQuest Timing Analyzer calculation results and further processing steps that account for the calibration that occurs at runtime. First, the TimeQuest analyzer returns the base setup and hold slacks, and further processing steps adjust the slacks to account for effects which the TimeQuest analyzer cannot model.

Write

Write timing analysis indicates the amount of slack on the DDR DQ signals that are latched by the memory device using the DQS strobe output from the FPGA device. The write timing paths are analyzed by a combination of the TimeQuest Timing Analyzer using the `set_output_delay` (max and min) and further steps to account for calibration that occurs at runtime. The ALTMEMPHY and UniPHY IP include timing constraints in the `<phy_variation_name>_ddr_timing.sdc` (ALTMEMPHY) or `<phy_variation_name>.sdc` (UniPHY), and further slack analysis in `<phy_variation_name>_report_timing.tcl` and `<phy_variation_name>_report_timing_core.tcl` files.

Read Resynchronization

In the DDR3, DDR2, and DDR SDRAM interfaces with Arria II GX FPGAs, the resynchronization timing analysis concerns transferring read data that is captured with a DQS strobe to a clock domain under the control of the ALTMEMPHY. After calibration by a sequencer, a dedicated PLL phase tracks any movements in the data valid window of the captured data. The exact length of the DQS and CK traces does not affect the timing analysis. The calibration process centers the resynchronization clock phase in the middle of the captured data valid window to maximize the resynchronization setup and hold the margin, and removes any static offset from other timing paths. With the static offset removed, any remaining uncertainties are voltage and temperature variation, jitter and skew.

In a UniPHY interface, a FIFO buffer synchronizes the data transfer from the data capture to the core. The calibration process sets the depth of the FIFO buffer and no dedicated synchronization clock is required. Refer to `<phy_variation_name>_report_timing_core.tcl` for more information about the resynchronization timing margin equation.

Mimic Path

The mimic path mimics the FPGA portion of the elements of the round-trip delay, which enables the calibration sequencer to track delay variations because of voltage and temperature changes during the memory read and write transactions without interrupting the operation of the ALTMEMPHY megafunction.

As the timing path register is integrated in the IOE, there is no timing constraint required for the Arria II GX device families.

For Cyclone III and Cyclone IV devices, the mimic register is a register in the core and it is placed closer to the IOE by the fitter.

 The UniPHY IP does not use any mimic path.

DQS versus CK—Arria II GX, Cyclone III, and Cyclone IV Devices

The DQS versus CK timing path indicates the skew requirement for the arrival time of the DQS strobe at the memory with respect to the arrival time of CK/CK# at the memory. Arria II GX, Cyclone III, and Cyclone IV devices require the DQS strobes and CK clocks to arrive edge aligned.

There are two timing constraints for DQS versus CK timing path to account for duty cycle distortion. The DQS/DQS# rising edge to CK/CK# rising edge (t_{DQSS}) requires the rising edge of DQS to align with the rising edge of CK to within 25% of a clock cycle, while the DQS/DQS# falling edge setup/hold time from CK/CK# rising edge (t_{DSS}/t_{DSH}) requires the falling edge of DQS to be more than 20% of a clock cycle away from the rising edge of CK.

The TimeQuest Timing Analyzer analyzes the DQS vs CK timing paths using the `set_output_delay` (max and min) constraints. For more information, refer to `<phy_variation_name>_phy_ddr_timing.sdc`.

Write Leveling t_{DQSS}

In DDR2 SDRAM (with UniPHY) and DDR3 SDRAM (with ALTMEMPHY and UniPHY) interfaces, write leveling t_{DQSS} timing is a calibrated path that details skew margin for the arrival time of the DQS strobe with respect to the arrival time of CK/CK# at the memory side. For proper write leveling configuration, DLL delay chain must be equal to 8. The PHY IP reports the margin through an equation. For more information, refer to `<phy_variation_name>_report_timing_core.sdc`.

Write Leveling t_{DSH}/t_{DSS}

In DDR2 SDRAM (with UniPHY) and DDR3 SDRAM (with ALTMEMPHY and UniPHY) interfaces, write leveling t_{DSH}/t_{DSS} timing details the setup and hold margin for the DQS falling edge with respect to the CK clock at the memory. The PHY IP reports the margin through an equation. For more information, refer to `<phy_variation_name>_report_timing_core.sdc`.

DK versus CK (RLDRAM II with UniPHY)

In RLDRAM II with UniPHY designs using the Nios-based sequencer, DK versus CK timing is a calibrated path that details skew margin for the arrival time of the DK clock versus the arrival time of CK/CK# on the memory side. The PHY IP reports the margin through an equation. For more information, refer to `<phy_variation_name>_report_timing_core.sdc`.

Bus Turnaround Time

In DDR2 and DDR3 SDRAM, and RLDRAM II (CIO) with UniPHY designs that use bidirectional data bus, you may have potential encounter with data bus contention failure when a write command follows a read command. The bus-turnaround time analysis determines how much margin there is on the switchover time and prevents bus contention. If the timing is violated, you can either increase the controller's bus turnaround time, which may reduce efficiency or board traces delay. Refer to `<variation>_report_timing_core.tcl` for the equation. You can find this analysis in the timing report. This analysis is only available for DDR2/3 SDRAM and RLDRAM II UniPHY IPs in Arria II GZ, Arria V, Cyclone V, Stratix IV, and Stratix V devices.

The RTL simulation for ALTMEMPHY IP is unable to detect timing violations because ALTMEMPHY IP is not enhanced with the bus turnaround analysis feature. Therefore, Altera recommends that you verify the design on board by manually changing the default values of `MEM_IF_WR_TO_RD_TURNAROUND_OCT` and `MEM_IF_RD_TO_WR_TURNAROUND_OCT` parameters in the controller wrapper file.

To determine whether the bus turnaround time issue is the cause of your design failure and to overcome this timing violation, follow these steps:

1. When the design fails, change the default values of `MEM_IF_WR_TO_RD_TURNAROUND_OCT` and `MEM_IF_RD_TO_WR_TURNAROUND_OCT` parameters in the controller wrapper file to a maximum value of 5. If the design passes after the change, it is a bus turnaround issue.

2. To solve the bus turnaround time issue, reduce the values of the MEM_IF_WR_TO_RD_TURNAROUND_OCT and MEM_IF_RD_TO_WR_TURNAROUND_OCT parameters gradually until you reach the minimum value needed for the design to pass on board.

Timing Report DDR

The **Report DDR** task in the TimeQuest Timing Analyzer generates custom timing margin reports for all ALTMEMPHY and UniPHY instances in your design. The TimeQuest Timing Analyzer generates this custom report by sourcing the wizard-generated `<variation>_report_timing.tcl` script.

This `<variation>_report_timing.tcl` script reports the following timing slacks on specific paths of the DDR SDRAM:

- Read capture
- Read resynchronization
- Mimic, address and command
- Core
- Core reset and removal
- Half-rate address and command
- DQS versus CK
- Write
- Write leveling (t_{DQSS})
- Write leveling (t_{DSS}/t_{DSH})

In Stratix III and Cyclone III designs, the `<variation_name>_report_timing.tcl` script checks the design rules and assumptions as listed in “[Timing Model Assumptions and Design Rules](#)” on page 10-29. If you do not adhere to these assumptions and rules, you receive critical warnings when the TimeQuest Timing Analyzer runs during compilation or when you run the **Report DDR** task.

To generate a timing margin report, follow these steps:

1. Compile your design in the Quartus II software.
2. Launch the TimeQuest Timing Analyzer.
3. Double-click **Report DDR** from the **Tasks** pane. This action automatically executes the **Create Timing Netlist**, **Read SDC File**, and **Update Timing Netlist** tasks for your project.

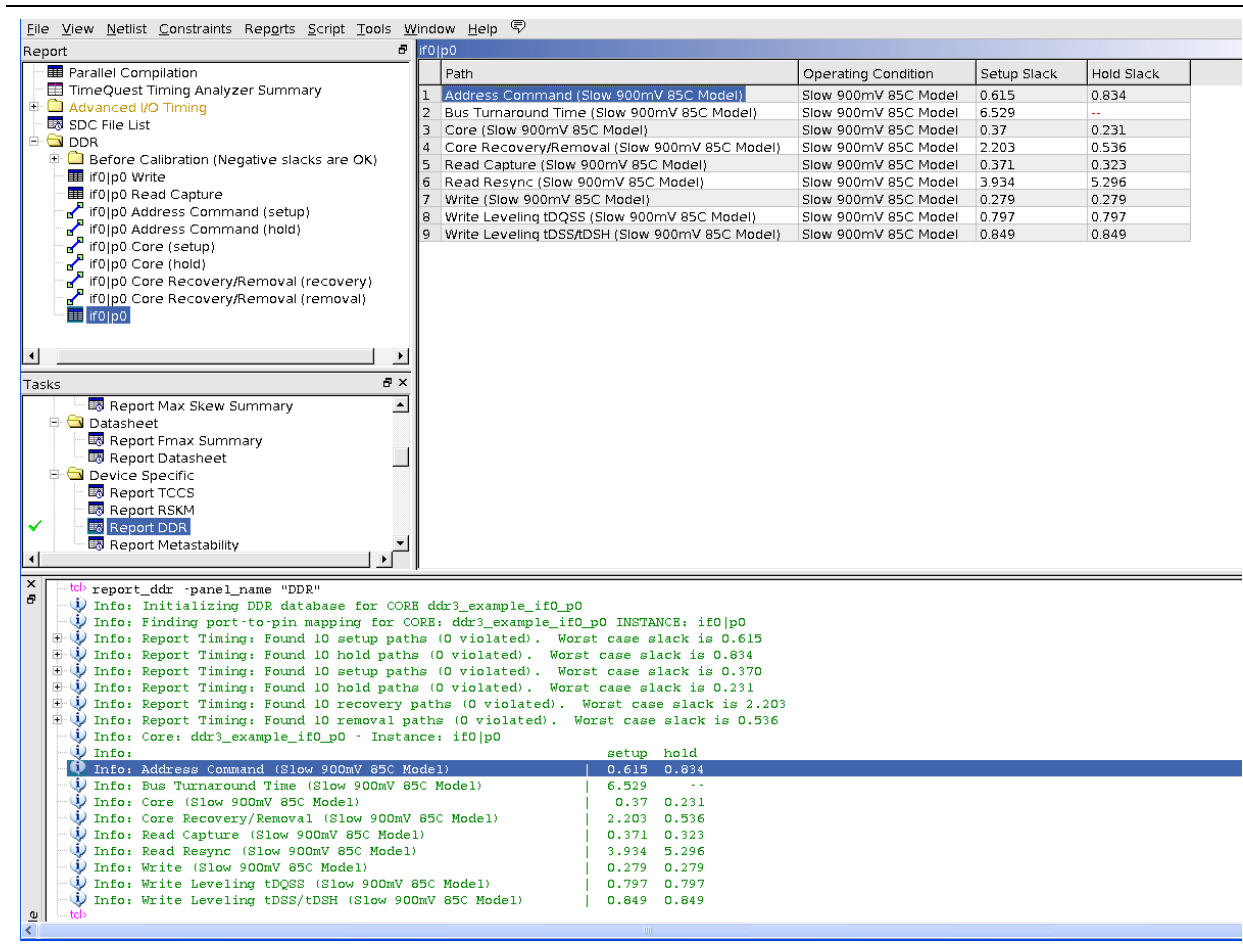


The `.sdc` may not be applied correctly if the variation top-level file is the top-level file of the project. You must have the top-level file of the project instantiate the variation top-level file.

The **Report DDR** feature creates a new DDR folder in the TimeQuest Timing Analyzer **Report** pane.

Expanding the DDR folder reveals the detailed timing information for each PHY timing path, in addition to an overall timing margin summary for the ALTMEMPHY or UniPHY instance, as shown in Figure 10-10.

Figure 10-10. Timing Margin Summary Window Generated by Report DDR Task




 Bus turnaround time shown in Figure 10-10 is available in all UniPHY IPs and devices except in QDR II and QDR II+ SRAM memory protocols and Stratix III devices.

Figure 10-11 shows the timing analysis results calculated using FPGA timing model before adjustment in the **Before Calibration** panel.

Figure 10-11. Read and Write Before Calibration

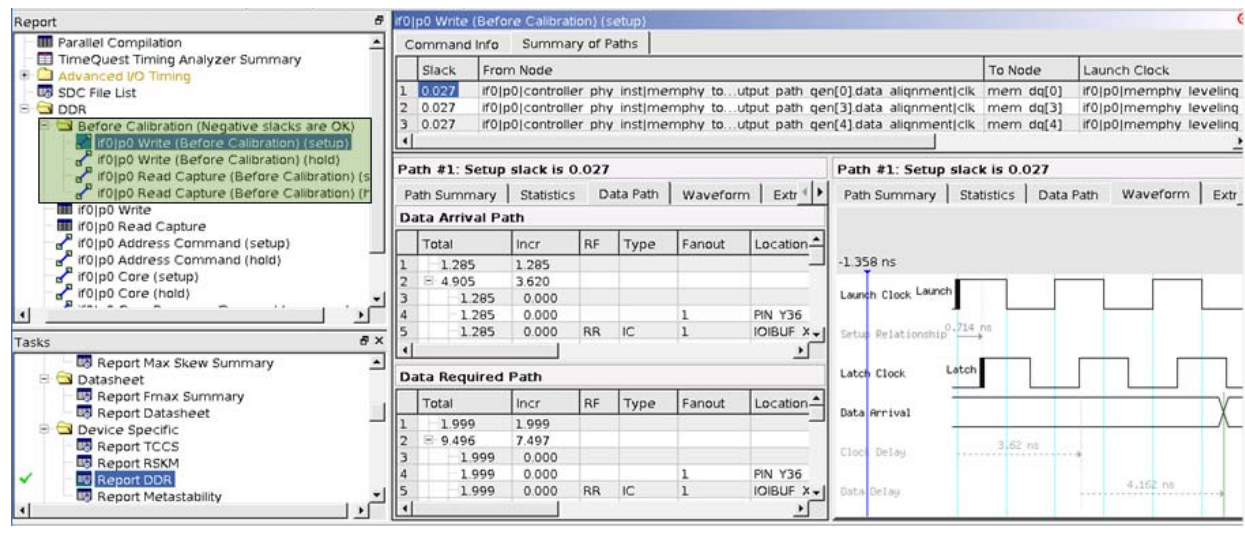


Figure 10-12 and Figure 10-13 show the read capture and write margin summary window generated by the Report DDR Task for a DDR3 core. It first shows the timing results calculated using the FPGA timing model. The `<variation_name>_report_timing_core.tcl` then adjusts these numbers to account for effects that are not modeled by either the timing model or by TimeQuest Timing Analyzer. The read and write timing margin analysis for Stratix III and Cyclone III devices do not need any adjustments.

Figure 10-12. Read Capture Margin Summary Window

if0 p0 Read Capture			
	Operation	Setup Slack	Hold Slack
1	After Calibration Read Capture	0.371	0.323
2	Before Calibration Read Capture	0.280	0.273
3	Memory Calibration	0.078	0.150
4	Deskew Read	0.157	0.044
5	Quantization error	-0.050	-0.050
6	Calibration uncertainty	-0.093	-0.093

Figure 10-13. Write Capture Margin Summary Window

if0 p0 Write			
	Operation	Setup Slack	Hold Slack
1	After Calibration Write	0.279	0.279
2	Before Calibration Write	0.027	0.026
3	Memory Calibration	0.135	0.113
4	Deskew Write and/or more clock pessimism removal	0.216	0.240
5	Quantization error	-0.050	-0.050
6	Calibration uncertainty	-0.050	-0.050

Report SDC

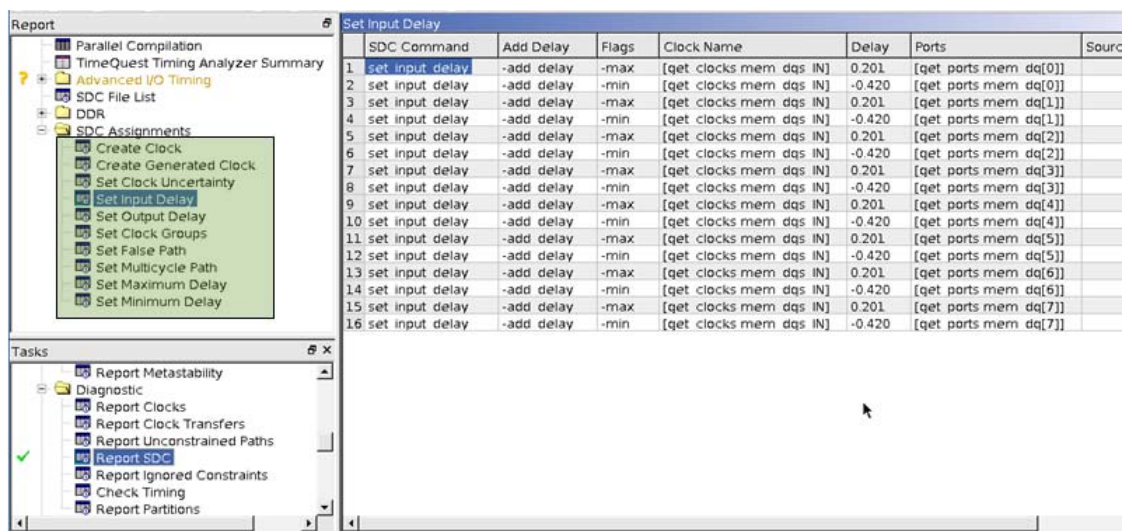
The **Report SDC** task in the TimeQuest Timing Analyzer generates the SDC assignment reports for your design. The TimeQuest Timing Analyzer generates this constraint report by sourcing the `.sdc`. The SDC assignment reports show the constraint applied in the design.

For example, the reports may include the following constraints:

- Create Clock
- Create Generated Clock
- Set Clock Uncertainty
- Set Input Delay
- Set Output Delay
- Set False Path
- Set Multicycle Path
- Set Maximum Delay
- Set Minimum Delay

Figure 10-14 shows the SDC assignments generated by the **Report SDC** task for a DDR3 SDRAM core design. The timing analyzer uses these constraint numbers in analysis to calculate the timing margin. Refer to the `.sdc` files of each constraints number.

Figure 10-14. SDC Assignments Report Window



Calibration Effect in Timing Analysis

Timing analysis for Arria II, Cyclone IV, Stratix IV, and Stratix V devices take into account the calibration effects to improve the timing margin. This section discusses ways to include the calibration effects in timing analysis.

Calibration Emulation for Calibrated Path

In conventional static timing analysis, calibration paths do not include calibration effects. To account for the calibration effects, the timing analyzer emulates the calibration process and integrates it into the timing analysis. Normally the calibration process involves adding or subtracting delays to a path. The analyzer uses the delay obtained through static timing analysis in the emulation algorithm to estimate the extra delay added during calibration. With these estimated delays, the timing analysis emulates hardware calibration and obtains a better estimate timing margin.



Refer to `<phy_variation_name>_report_timing.tcl` and `<phy_variation_name>_report_timing_core.tcl` for the files that determine the timing margin after calibration.

Calibration Error or Quantization Error

Hardware devices use calibration algorithms when delay information is unknown or incomplete. If the delay information is unknown, the timing analysis of the calibrated paths has to work with incomplete data. This unknown information may cause the timing analysis calibration operations to pick topologies that are different than what would actually occur in hardware. The differences between what can occur in hardware and what occurs in the timing analysis are quantified and included in the timing analysis of the calibrated paths as quantization error or calibration error.

Calibration Uncertainties

Calibration results may change or reduce due to one or more of the following uncertainties:

- Jitter and DCD effects
- Voltage and temperature variations
- Board trace delays changing due to noise on terminated supply voltages

These calibration uncertainties are accounted for in the timing analysis.

Memory Calibration

All the timing paths reported include one or more memory parameters, such as t_{DQSS} and t_{DQSQ} . These specifications indicate the amount of variation that occurs in various timing paths in the memory and abstracts them into singular values so that they can be used by others when interfacing with the memory device.

JEDEC defines these parameters in their specification for memory standards, and every memory vendor must meet this specification or improve it. However, there is no proportion of each specification due to different types of variations. Variations that are of interest are typically grouped into three different types: process variations (P), voltage variations (V), and temperature variations (T). These together compose PVT

variations that typically define the JEDEC specification. You can determine the maximum P variation by comparing different dies, and you can determine the maximum V and T variations by operating a design at the endpoints of the range of voltage and temperature. P variations do not change once the chip has been fabricated, while V and T variations change over time.

The timing analysis for Stratix V FPGAs at 667 MHz of various paths (if the analysis is comprehensive and includes all the sources of noise) indicate that there is no timing margin available. However, the designs do actually work in practice with a reasonable amount of margin. The reason for this behavior is that the memory devices typically have specifications that easily beat the JEDEC specification and that our calibration algorithms calibrate out the process portion of the JEDEC specification, leaving only the V and T portions of the variations.

The memory calibration figure determination includes noting what percentage of the JEDEC specification of various memory parameters is caused by process variations for which Altera IPs' (ALTMEMPHY and UniPHY) calibration algorithms can calibrate out, and to apply that to the full JEDEC specification. The remaining portion of the variation is caused by voltage and temperature variations which cannot be calibrated out.

You can find the percentage of the JEDEC specification that is due to process variation is set in `<variation>_report_timing.tcl`.

Timing Model Assumptions and Design Rules

External memory interfaces using Altera IP are optimized for highest performance, and use a high-performance timing model to analyze calibrated and source-synchronous, double-data rate I/O timing paths. This timing model applies to designs that adhere to a set of predefined assumptions. These timing model assumptions include memory interface pin-placement requirements, PLL and clock network usage, I/O assignments (including I/O standard, termination, and slew rate), and many others.

For example, the read and write datapath timing analysis is based on the FPGA pin-level t_{TCCS} and t_{SW} specifications, respectively. While calculating the read and write timing margins, the Quartus II software analyzes the design to ensure that all read and write timing model assumptions are valid for your variation instance.



Timing model assumptions only apply to Stratix III and Cyclone III devices.

When the Report DDR task or `report_timing.tcl` script is executed, the timing analysis assumptions checker is invoked with specific variation configuration information. If a particular design rule is not met, the Quartus II software reports the failing assumption as a Critical Warning message. Figure 10-15 shows a sample set of messages generated when the memory interface DQ, DQS, and CK/CK# pins are not placed in the same edge of the device.

Figure 10-15. Read and Write Timing Analysis Assumption Verification

```

477 tcl> report_ddr -panel_name "DDR"
478 Critical Warning: Pin mem_clk[0], mem_dq[0], mem_dq[10], mem_dq[11], mem_dq[12], mem_dq[13], mem_dq[14], mem_dq[15], mem
479 Critical Warning: mem_clk[0] was placed on the left edge of the device
480 Critical Warning: mem_dq[0] was placed on the bottom edge of the device
481 Critical Warning: mem_dq[10] was placed on the bottom edge of the device
482 Critical Warning: mem_dq[11] was placed on the bottom edge of the device
483 Critical Warning: mem_dq[12] was placed on the bottom edge of the device
484 Critical Warning: mem_dq[13] was placed on the bottom edge of the device
485 Critical Warning: mem_dq[14] was placed on the bottom edge of the device
486 Critical Warning: mem_dq[15] was placed on the bottom edge of the device
487 Critical Warning: mem_dq[16] was placed on the bottom edge of the device
488 Critical Warning: mem_dq[17] was placed on the bottom edge of the device
489 Critical Warning: mem_dq[18] was placed on the bottom edge of the device
551 Critical Warning: mem_dq[9] was placed on the bottom edge of the device
552 Critical Warning: mem_dqs[0] was placed on the bottom edge of the device
553 Critical Warning: mem_dqs[1] was placed on the bottom edge of the device
554 Critical Warning: mem_dqs[2] was placed on the bottom edge of the device
555 Critical Warning: mem_dqs[3] was placed on the bottom edge of the device
556 Critical Warning: mem_dqs[4] was placed on the bottom edge of the device
557 Critical Warning: mem_dqs[5] was placed on the bottom edge of the device
558 Critical Warning: mem_dqs[6] was placed on the bottom edge of the device
559 Critical Warning: mem_dqs[7] was placed on the bottom edge of the device
560 Critical Warning: mem_dqs[8] was placed on the bottom edge of the device
561 Critical Warning: Memory clock pin mem_clk[0], mem_clk[1], mem_clk[2] must be placed on the same edge of the device
562 Critical Warning: mem_clk[0] was placed on the left edge of the device
563 Critical Warning: mem_clk[1] was placed on the top edge of the device
564 Critical Warning: mem_clk[2] was placed on the bottom edge of the device
565 Critical Warning: Read Capture and write timing analyses may not be valid due to violated timing model assumptions
566 Info: Report Timing: Found 24 setup paths (0 violated). Worst case slack is 1.155

```

Memory Clock Output Assumptions

To verify the quality of the FPGA clock output to the memory device (CK/CK# or K/K#), which affects FPGA performance and quality of the read clock/strobe used to read data from the memory device, the following assumptions are necessary:

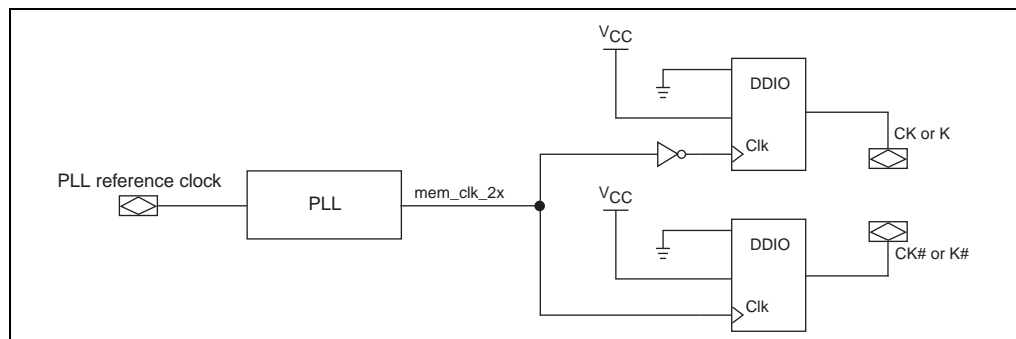
- The slew rate setting must be **Fast** or an on-chip termination (OCT) setting must be used.
- The output delay chains must all be **0** (the default value applied by the Quartus II software). These delay chains include the Cyclone III output register to pin delay chain and the Stratix III D5 and D6 output delay chains.
- The output open-drain parameter on the memory clock pin `IO_OBUF` atom must be **Off**. The **Output Open Drain** logic option must not be enabled.
- The weak pull-up on the CK and CK# pads must be **Off**. The **Weak Pull-Up Resistor** logic option must not be enabled.
- The bus hold on the CK and CK# pads must be **Off**. The **Enable Bus-Hold Circuitry** logic option must not be enabled.
- All CK and CK# pins must be declared as output-only pins or bidirectional pins with the output enable set to V_{CC} .

Cyclone III Devices


For Cyclone III devices the following additional memory clock assumptions are necessary:

- The memory clock output pins must be fed by DDIO output registers and placed on DIFFIO_{p-} and n- pin pairs.
- The memory output clock signals must be generated using the DDIO configuration shown in Figure 10–16. In this configuration, the high register connects to V_{CC} and the low register connects to GND.

Figure 10–16. DDIO Configuration



- CK and CK# pins must be fed by a DDIO_OUT WYSIWYG with datainhi connected to GND and datainlo connected to V_{CC}.
- CK or K pins must be fed by a DDIO_OUT with its clock input from the PLL inverted.
- CK# or K# pins must be fed by a DDIO_OUT with its clock input from the PLL uninverted.
- The I/O standard and current strength settings on the memory clock output pins must be as follows:
 - SSTL-2 Class I and 12 mA, or SSTL-2 Class II and 16 mA for DDR SDRAM interfaces
 - SSTL-18 Class I and 12 mA, or SSTL-18 Class II and 16 mA for DDR2 SDRAM interfaces

 For more information about placing memory clock output pins, refer to “Additional Placement Rules for Cyclone III and Cyclone IV Devices” in the *Planning Pin and Resource* chapter in volume 2 of the *External Memory Interface Handbook*.

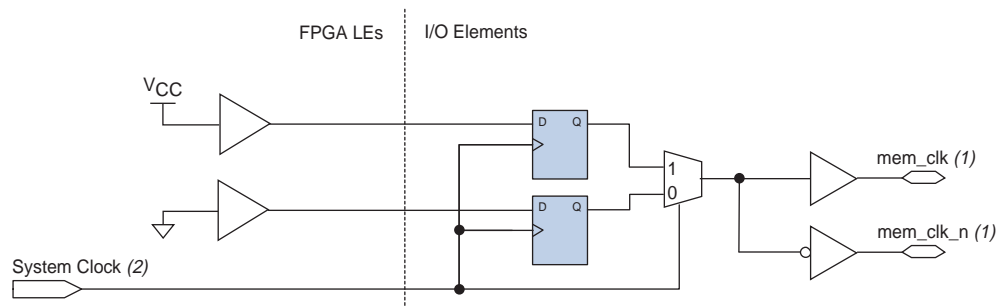
Stratix III Devices

For Stratix III devices the following additional memory clock assumptions are necessary:

- All memory clock output pins must be placed on DIFFOUT pin pairs on the same edge of the device.

- For DDR3 SDRAM interfaces:
 - The CK pins must be placed on FPGA output pins marked DQ, DQS, or DQSn.
 - The CK pin must be fed by an OUTPUT_PHASE_ALIGNMENT WYSIWYG with a 0° phase shift.
 - The PLL clock driving CK pins must be the same as the clock driving the DQS pins.
 - The T4 (DDIO_MUX) delay chains setting for the memory clock pins must be the same as the settings for the DQS pins.
- For non-DDR3 interfaces, the T4 (DDIO_MUX) delay chains setting for the memory clock pins must be greater than 0.
- The programmable rise and fall delay chain settings for all memory clock pins must be set to 0.
- The memory output clock signals must be generated with the DDIO configuration shown in Figure 10-17, with a signal splitter to generate the n- pin pair and a regional clock network-to-clock to output DDIO block.

Figure 10-17. DIDO Configuration with Signal Splitter



Notes to Figure 10-17:

- (1) The `mem_clk[0]` and `mem_clk_n[0]` pins for DDR3, DDR2, and DDR SDRAM interfaces use the I/O input buffer for feedback, therefore bidirectional I/O buffers are used for these pins. For memory interfaces using a differential DQS input, the input feedback buffer is configured as differential input; for memory interfaces using a single-ended DQS input, the input buffer is configured as a single-ended input. Using a single-ended input feedback buffer requires that the I/O standard's VREF voltage is provided to that I/O bank's VREF pins.
- (2) Regional QCLK (quadrant) networks are required for memory output clock generation to minimize jitter.

Write Data Assumptions

To verify the memory interface using the FPGA TCCS output timing specifications, the following assumptions are necessary:

- For QDRII, QDRII+, and RLDRAM II SIO memory interfaces, the write clock output pins (such as K/K# or DK/DK#) must be placed in DQS/DQSn pin pairs.
- The PLL clock used to generate the write-clock signals and the PLL clock used to generate the write-data signals must come from the same PLL.
- The slew rate for all write clocks and write data pins must be set to **Fast** or **OCT** must be used.

- When auto deskew is not enabled (or not supported by the ALTMEMPHY configuration), the output delay chains and output enable delay chains must all be set to the default values applied by Quartus II. These delay chains include the Cyclone III output register and output enable register-to-pin delay chains, and the Stratix III D5 and D6 delay chains.
- The output open drain for all write clocks and write data pins' IO_OBUF atom must be set to **Off**. The **Output Open Drain** logic option must not be enabled.
- The weak pull-up for all write clocks and write data pins must be set to **Off**. The **Weak Pull-Up Resistor** logic option must not be enabled.
- The Bus Hold for all write clocks and write data pins must be set to **Off**. The **Enable Bus-Hold Circuitry** logic option must not be enabled.

Cyclone III Devices

For Cyclone III devices the following additional write data assumptions are necessary:

- Write data pins (including the DM pins) must be placed on DQ pins related to the selected DQS pins.
- All write clock pins (DQS/DQS#) must be fed by DDIO output registers.
- All write data pins must be fed by DDIO output registers, V_{CC} , or GND.
- The phase shift of the PLL clock used to generate the write clocks must be 72° to 108° more than the PLL clock used to generate the write data (nominally 90° offset).
- The I/O standard and current strength settings on the write data- and clock-output pins must be as follows:
 - SSTL-2 Class I and 12 mA, or SSTL-2 Class II and 16 mA for DDR SDRAM interfaces
 - SSTL-18 Class I and 8/12 mA, or SSTL-18 Class II and 16 mA for DDR2 SDRAM interfaces

Stratix III Devices

For Stratix III devices the following additional write data assumptions are necessary:

- Differential write clock signals (DQS/DQS_n) must be generated using the signal splitter.
- The write data pins (including the DM pins) must be placed in related DQ pins associated with the chosen DQS pin. The only exception to this rule is for QDRII and QDRII+ $\times 36$ interfaces emulated using two $\times 18$ DQ groups. For such interfaces, all of the write data pins must be placed on the same edge of the device (left, right, top, or bottom). Also, the write clock K/K# pin pair should be placed on one of the DQS/DQS_n pin pairs on the same edge.

- All write clock pins must have similar circuit structure.
 - For DDR2 SDRAM interfaces and DDR3 SDRAM with leveling interfaces, all DQS/DQS# write strobes must be fed by DDIO output registers clocked by the write-leveling delay chain in the OUTPUT_PHASE_ALIGNMENT block.
 - For DDR and DDR2 SDRAM interfaces, all write clock pins must be fed by DDIO output registers clocked by a global or regional clock network.
- All write data pins must have similar circuit structure.
 - For DDR3 SDRAM interfaces, all write data pins must be fed by either DDIO output registers clocked by the OUTPUT_PHASE_ALIGNMENT block, V_{CC} , or GND.
 - For DDR and DDR2 SDRAM interfaces, all write data pins must be fed by either DDIO output registers clocked by a global or regional clock network, V_{CC} , or GND.
- The write clock output must be 72°, 90°, or 108° more than the write data output.
 - For DDR2 SDRAM and DDR3 SDRAM with leveling interfaces, the write-leveling delay chain in the OUTPUT_PHASE_ALIGNMENT block must implement a phase shift of 72°, 90°, or 108° to center-align write clock with write data.
 - For DDR and DDR2 SDRAM interfaces, the phase shift of the PLL clock used to clock the write clocks must be 72 to 108° more than the PLL clock used to clock the write data clocks to generated center-aligned clock and data.
- The T4 (DDIO_MUX) delay chains must all be set to 3. When differential DQS (using splitter) is used, T4 must be set to 2.
- The programmable rise and fall delay chain settings for all memory clock pins must be set to 0.

Table 10-9 lists I/O standards supported for the write clock and write data signals for each memory type and pin location.

Table 10-9. I/O standards (Part 1 of 2)

Memory Type	Placement	Legal I/O Standards for DQS	Legal I/O Standards for DQ
DDR3 SDRAM	Row I/O	Differential 1.5-V SSTL Class I	1.5-V SSTL Class I
DDR3 SDRAM	Column I/O	Differential 1.5-V SSTL Class I Differential 1.5-V SSTL Class II	1.5-V SSTL Class I 1.5-V SSTL Class II
DDR2 SDRAM	Any	SSTL-18 Class I SSTL-18 Class II Differential 1.8V SSTL Class I Differential 1.8V SSTL Class II	SSTL-18 Class I SSTL-18 Class II
DDR SDRAM	Any	SSTL-2 Class I SSTL-2 Class II	SSTL-2 Class I SSTL-2 Class II

Table 10–9. I/O standards (Part 2 of 2)

Memory Type	Placement	Legal I/O Standards for DQS	Legal I/O Standards for DQ
QDR II and QDR II + SRAM	Any	HSTL-1.5 Class I HSTL-1.8 Class I	HSTL-1.5 Class I HSTL-1.8 Class I
RLDRAM II	Any	HSTL-1.5 Class I HSTL-1.8 Class I	HSTL-1.5 Class I HSTL-1.8 Class I

Read Data Assumptions

To verify that the external memory interface can use the FPGA Sampling Window (SW) input timing specifications, the following assumptions are necessary:

- The read clocks input pins must be placed on DQS pins. DQS/DQS# inputs must be placed on differential DQS/DQSn pins on the FPGA.
- Read data pins (DQ) must be placed on the DQ pins related to the selected DQS pins.
- For QDR II and QDR II+ SRAM interfaces, the complementary read clocks must have a single-ended I/O standard setting of HSTL-18 Class I or HSTL-15 Class I.
- For RLDRAM II interfaces, the differential read clocks must have a single ended I/O standard setting of HSTL 18 Class I or HSTL 15 Class I.

Cyclone III Devices

For Cyclone III devices the following additional read data and mimic pin assumptions are necessary:

- The I/O standard setting on read data and clock input pins must be as follows:
 - SSTL-2 Class I and Class II for DDR SDRAM interface
 - SSTL-18 Class I and Class II for DDR2 SDRAM interfaces
- The read data and mimic input registers (flip-flops fed by the read data pin's input buffers) must be placed in the LAB adjacent to the read data pin. A read data pin can have 0 input registers.
- Specific routing lines from the IOE to core read data/mimic registers must be used. The Quartus II Fitter ensures proper routing unless user-defined placement constraints or LogicLock™ assignments force non-optimal routing. User assignments that prevent input registers from being placed in the LAB adjacent to the IOE must be removed.
- The read data and mimic input pin input pad to core/register delay chain must be set to 0.
- If all read data pins are on row I/Os or column I/Os, the mimic pin must be placed in the same type of I/O (row I/O for read-data row I/Os, column I/O for read-data column I/Os). For wraparound cases, the mimic pin can be placed anywhere.

Stratix III Devices

For Stratix III devices the following additional read data and mimic pin assumptions are necessary:

- For DDR3, DDR2, and DDR SDRAM interfaces, the read clock pin can only drive a DQS bus clocking a $\times 4$ or $\times 9$ DQ group.
- For QDR II, QDR II+ SRAM, and RLDRAM II interfaces, the read clock pin can only drive a DQS bus clocking a $\times 9$, $\times 18$, or $\times 36$ DQ group.
- For non-wraparound DDR, DDR2, and DDR3 interfaces, the mimic pin, all read clock, and all read data pins must be placed on the same edge of the device (top, bottom, left, or right). For wraparound interfaces, these pins can be placed on adjacent row I/O and column I/O edges and operate at reduced frequencies.
- All read data pins and the mimic pin must feed DDIO_IN registers and their input delay chains D1, D2, and D3 set to the Quartus II default.
- DQS phase-shift setting must be either 72° or 90° (supports only one phase shift for each operating band and memory standard).
- All read clock pins must have the `dqs_ctrl_latches_enable` parameter of its `DQS_DELAY_CHAIN` WYSIWYG set to false.
- The read clocks pins must have their D4 delay chain set to the Quartus II default value of 0.
- The read data pins must have their T8 delay chain set to the Quartus II default value of 0.
- When differential DQS strobes are used (DDR3 and DDR2 SDRAM), the mimic pin must feed a true differential input buffer. Placing the memory clock pin on a `DIFFIO_RX` pin pair allows the mimic path to track timing variations on the DQS input path.
- When single ended DQS strobes are used, the mimic pin must feed a single ended input buffer.

Mimic Path Assumptions

To verify that the ALTMEMPHY-based DDR, DDR2, or DDR3 SDRAM interface's mimic path is configured correctly, the mimic path input must be placed on the `mem_clk[0]` pin.

DLL Assumptions

The following DLL assumptions are necessary:



These assumptions do not apply to Cyclone III devices.

- The DLL must directly feed its `delayctrlout[]` outputs to all DQS pins without intervening logic or inversions.
- The DLL must be in a valid frequency band of operation as defined in the corresponding device data sheet.
- The DLL must have jitter reduction mode and dual-phase comparators enabled.

PLL and Clock Network Assumptions

The PLL and clock network assumptions vary for each device family.

Stratix III Devices

- The PLL that generates the memory output clock signals and write data and clock signals must be set to **No compensation** mode to minimize output clock jitter.
- The reference input clock signal to the PLL must be driven by the dedicated clock input pin located adjacent to the PLL, or from the clock output signal from the adjacent PLL. To minimize output clock jitter, the reference input clock pin to the ALTMEMPHY PLL must not be routed through the core using global or regional clock networks. If the reference clock cascades from another PLL, that upstream PLL must be in **No compensation** mode and **Low bandwidth** mode.
- For DDR3 and DDR2 SDRAM interfaces, use only regional or dual regional clock networks to route PLL outputs that generate the write data, write clock, and memory output clock signals. This requirement ensures that the memory output clocks (CK/CK#) meet the memory device input clock jitter specifications, and that output timing variations or skews are minimized.
- For other memory types, the same clock tree type (global, regional, or dual regional) is recommended for PLL clocks generating the write clock, write data, and memory clock signals to minimize timing variations or skew between these outputs.

Cyclone III Devices

To verify that the memory interface's PLL is configured correctly, the following assumptions are necessary:

- The PLL that generates the memory output clock signals and write data/clock signals must be set to **Normal** compensation mode in Cyclone III devices.
- PLL cascading is not supported.
- The reference input clock signal to the PLL must be driven by the dedicated clock input pin located adjacent to the PLL. The reference input clock pin must not be routed through the core using global or regional clock networks to minimize output clock jitter.

Timing Closure

This section describes common issues and how to optimize timing.

Common Issues

This topic describes potential timing closure issues that can occur when using the ALTMEMPHY or UniPHY IP. For possible timing closure issues with ALTMEMPHY or UniPHY variations, refer to the *Quartus II Software Release Notes* for the software version that you are using. You can solve some timing issues by moving registers or changing the project fitting setting to **Standard** (from **Auto**).



The *Quartus II Software Release Notes* list common timing issues that can be encountered in a particular version of the Quartus II software.

Missing Timing Margin Report

The ALTMEMPHY and UniPHY timing margin reports may not be generated during compilation if the `.sdc` does not appear in the Quartus II project settings.

Timing margin reports are not generated if you specify the ALTMEMPHY or UniPHY variation as the top-level project entity. Instantiate the ALTMEMPHY or UniPHY variation as a lower level module in your user design or memory controller.

Incomplete Timing Margin Report


The timing report may not include margin information for certain timing paths if certain memory interface pins are optimized away during synthesis. Verify that all memory interface pins appear in the `<variation>_autodetectedpins.tcl` (ALTMEMPHY) or `<variation>_all_pins.txt` (UniPHY) file generated during compilation, and ensure that they connect to the I/O pins of the top-level FPGA design.

Read Capture Timing

In Stratix III and Stratix IV devices, read capture timing may fail if the DQS phase shift selected is not optimal or if the board skew specified is large.

- You can adjust the effective DQS phase shift implemented by the DLL to balance setup and hold margins on the read timing path. The DQS phase shift can be adjusted in coarse PVT-compensated steps of 22.5°, 30°, 36°, or 45° by changing the number of delay buffers (range 1 to 4), or in fine steps using the DQS phase offset feature that supports uncompensated delay addition and subtraction in approximately 12 ps steps.
- To adjust the coarse phase shift selection, determine the supported DLL modes for your chosen memory interface frequency by referencing the DLL and DQS Logic Block Specifications tables in the *Switching Characteristics* section of the device data sheet. For example, a 400 MHz DDR2 interface on a -2 speed grade device can use DLL mode 5 (resolution 36°, range 290 – 450 MHz) to implement a 72° phase shift, or DLL mode 6 (resolution 45°, range 360–560 MHz) to implement a 90° phase shift.

In Cyclone III devices, the read capture is implemented using a calibrated clock, and therefore no clock phase-shift adjustment is possible. Additionally, the capture registers are routed to specific LE registers in the logic array blocks (LABs) adjacent to the IOE using predefined routing. Therefore, no timing optimization is possible for this path. Ensure that you select the correct memory device speed grade for the FPGA speed grade and interface frequency.

 Ensure that you specify the appropriate board-skew parameter when you parameterize the controllers in the parameter editor. The default board trace length mismatch used is 20 ps.

Write Timing

Negative timing margins may be reported for write timing paths if the PLL phase shift used to generate the write data signals is not optimal. Adjust the PLL phase shift selection on the write clock PLL output using the PLL MegaWizard Plug-In Manager.

 Regenerating the ALTMEMPHY- or UniPHY-based controller overwrites changes made using the PLL MegaWizard Plug-In Manager.

Address and Command Timing

You can optimize the timing margins on the address and command timing path by changing the PLL phase shift used to generate these signals. Modify the **Dedicated Clock Phase** parameter in the **PHY Settings** page of the ALTMEMPHY parameter editor. In the DDR2 or DDR3 SDRAM Controllers with UniPHY IP cores, modify the **Additional CK/CK# phase** and **Additional Address and Command clock phase** parameters.

The DDR2 and DDR3 SDRAM memory controllers use 1T memory timing even in half-rate mode, which may affect the address command margins for DDR2 or DDR3 SDRAM designs that use memory DIMMs. DDR2 SDRAM designs have a greater impact because the address command bus fans out to all the memory devices on a DIMM increasing the loading effect on the bus. Make sure your board designs are robust enough to have the memory clock rising edge within the 1T address command window. You can also use the **Additional Address and Command clock phase** parameter to adjust the phase of the address and command if needed.

The far-end load value and board trace delay differences between address and command and memory clock pins can result in timing failures if they are not accounted for during timing analysis.

The Quartus II Fitter may not optimally set output delay chains on the address and command pins. To ensure that any PLL phase-shift adjustments are not negated by delay chain adjustments, create logic assignments using the Assignment Editor to set all address and command output pin D5 delay chains to 0.

For HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices, some corner cases of device family and memory frequency may require an increase to the address and command clock phase to meet core timing. You can identify this situation, if the DDR timing report shows a `PHY setup` violation with the `phy_clk` launch clock, and the address and command latch clock—clock 0 (half-rate `phy_clk`) or 2 (full-rate `phy_clk`), and 6, respectively.

If you see this timing violation, you may fix it by advancing the address and command clock phase as required. For example, a 200-ps violation for a 400-MHz interface represents 8% of the clock period, or 28.8°. Therefore, advance the address and command phase from 270° to 300°. However, this action reduces the setup and hold margin at the DDR device.

PHY Reset Recovery and Removal

A common cause for reset timing violations in ALTMEMPHY or UniPHY designs is the selection of a global or regional clock network for a reset signal. The ALTMEMPHY or UniPHY IP does not require any dedicated clock networks for reset signals. Only ALTMEMPHY or UniPHY PLL outputs require clock networks, and any other PHY signal using clock networks may result in timing violations.

You can correct such timing violations by:

- Setting the Global Signal logic assignment to **Off** for the problem path (using the Assignment Editor), or
- Adjusting the logic placement (using the Assignment Editor or Chip Planner)

Clock-to-Strobe (for DDR and DDR2 SDRAM Only)

Memory output clock signals and DQS strobes are generated using the same PLL output clock. Therefore, no timing optimization is possible for this path and positive timing margins are expected for interfaces running at or below the FPGA data sheet specifications.

For DDR3 interfaces, the timing margin for this path is reported as **Write Leveling**.

Read Resynchronization and Write Leveling Timing (for SDRAM Only)

These timing paths apply only to Arria II GX, Stratix III, and Stratix IV devices, and are implemented using calibrated clock signals driving dedicated IOE registers. Therefore, no timing optimization is possible for these paths, and positive timing margin is expected for interfaces running at or below the FPGA data sheet specifications.

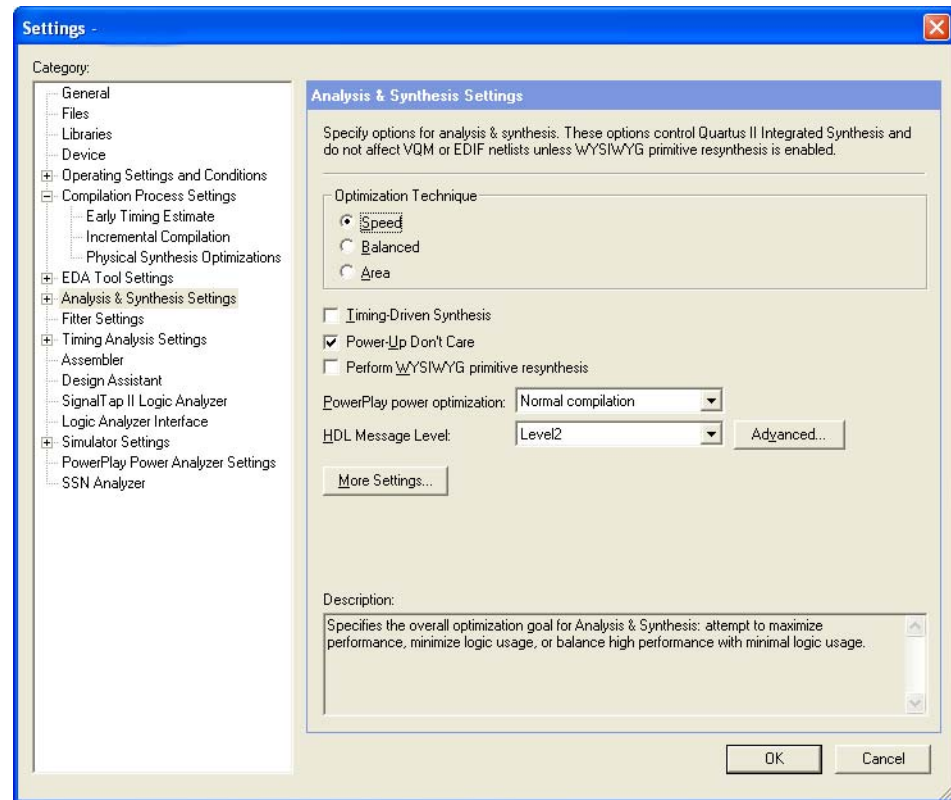
Ensure that you specify the correct memory device timing parameters (t_{DQSCK} , t_{DSS} , t_{DSH}) and board skew (t_{EXT}) in the ALTMEMPHY, DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY, or DDR2 and DDR3 SDRAM Controllers with UniPHY parameter editor.

Optimizing Timing

For full-rate designs you may need to use some of the Quartus II advanced features, to meet core timing, by following these steps:

1. On the Assignments menu click **Settings**. In the **Category** list, click **Analysis & Synthesis Settings**. For **Optimization Technique** select **Speed** (see Figure 10-18).

Figure 10-18. Optimization Technique



2. In the **Category** list, click **Physical Synthesis Optimizations**. Specify the following options:

- Turn on **Perform physical synthesis for combinational logic**.

For more information about physical synthesis, refer to the *Netlist and Optimizations and Physical Synthesis* chapter in the *Quartus II Software Handbook*.

- Turn on **Perform register retiming**
- Turn on **Perform automatic asynchronous signal pipelining**
- Turn on **Perform register duplication**


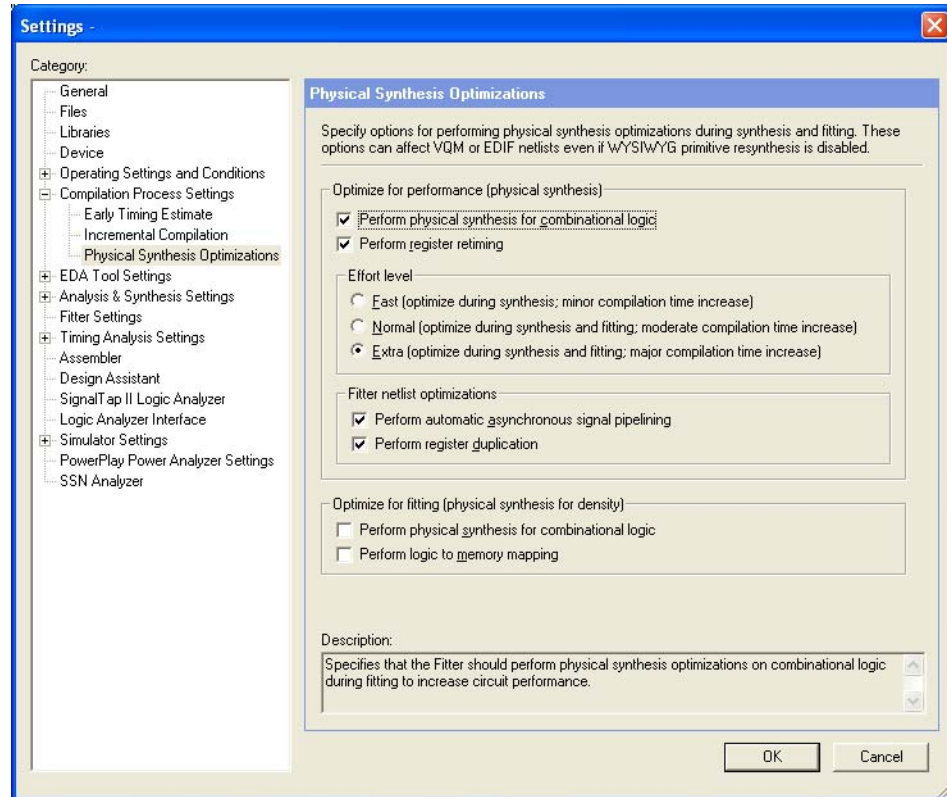
 You can initially select **Normal** for **Effort level**, then if the core timing is still not met, select **Extra** (see [Figure 10-19](#)).

Figure 10-19. Physical Synthesis Optimizations



Timing Deration Methodology for Multiple Chip Select DDR2 and DDR3 SDRAM Designs


In a multiple chip select system, each individual rank has its own chip select signal. Consequently, you must change the **Total Memory chip selects**, **Number of chip select** (for discrete components) or **Number of chip select per slot** (DIMMs) in the **Preset Editor** of the ALTMEMPHY- or UniPHY-based parameter editors.

In the **Preset Editor**, you must leave the baseline non-derated 'DS, 'DH, 'IS, 'IH values, because the settings on the **Board Settings** page account for multiple chip select slew rate deration.


This section explains the following two timing deration methodologies for multiple chip-select DDR2 and DDR3 SDRAM designs:

- [Timing Deration using the Board Settings](#)
- [Timing Deration Using the Excel-Based Calculator](#)

For Arria II GX, Arria II GZ, Stratix IV, and Stratix V devices, the ALTMEMPHY, and ALTMEMPHY- and UniPHY-based controller parameter editors have an option to select multiple chip-select deration.

 To perform multiple chip-select timing deration for other Altera devices (for example Cyclone III and Stratix III devices), Altera provides an Excel-based calculator available from the [Altera website](#).

Timing deration in this section applies to either discrete components or DIMMs.

 You can derate DDR SDRAM multiple chip select designs by using the DDR2 SDRAM section of the Excel-based calculator, but Altera does not guarantee the results.

This section assumes you know how to obtain data on PCB simulations for timing deration from HyperLynx or any other PCB simulator.

Multiple Chip Select Configuration Effects

A DIMM contains one or several RAM chips on a small PCB with pins that connect it to another system such as a motherboard or router.

Nonregistered (unbuffered) DIMMs (or UDIMMs) connect address and control buses directly from the module interface to the DRAM on the module.

Registered DIMMs (RDIMMs) improve signal integrity (and hence potentially clock rates and overall memory size) by electrically buffering the signals with a register, at a cost of an extra clock of increased latency. In addition, most RDIMMs come with error correction coding (ECC) as standard.

Multiple chip select configurations allow for one set of data pins (and address pins for UDIMMs) to be connected to two or more memory ranks. Multiple chip select configurations have a number of effects on the timing analysis including the intersymbol interference (ISI) effects, board effects, and calibration effects.

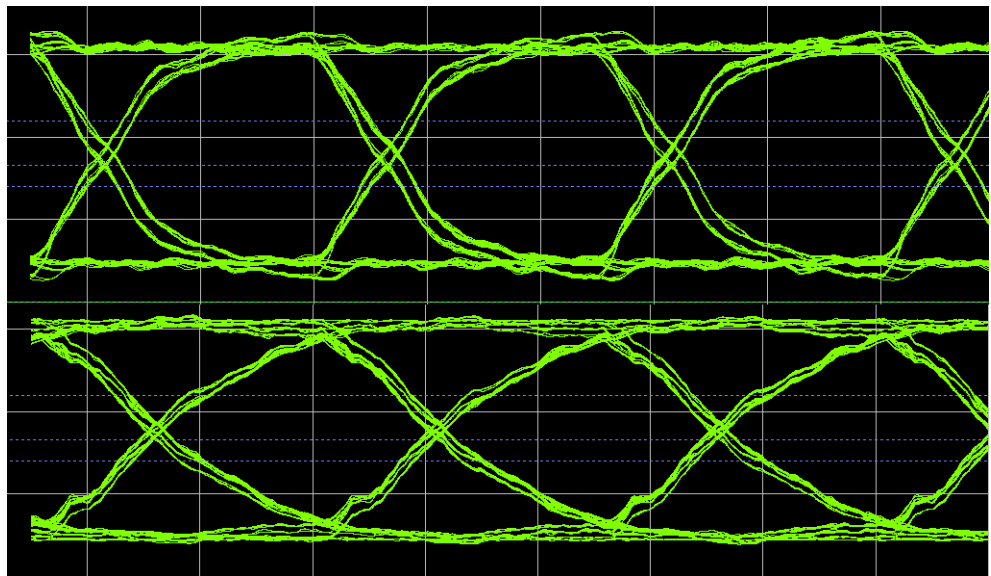
ISI Effects

With multiple chip selects and possible slots loading the far end of the pin, there may be ISI effects on a signal causing the eye openings for DQ, DQS, and address and command signals to be smaller than for single-rank designs (Figure 10-20).

Figure 10-20 shows the eye shrinkage for DQ signal of a single rank system (top) and multiple chip select system (bottom). The ISI eye reductions reduce the timing window available for both the write path and the address and command path analysis. You must specify them as output delay constraints in the .sdc.

Extra loading from the additional ranks causes the slew rate of signals from the FPGA to be reduced. This reduction in slew rate affects some of the memory parameters including data, address, command and control setup and hold times (t_{DS} , t_{DH} , t_{IS} , and t_{IH}).

Figure 10-20. Eye Shrinkage for DQ Signal




Calibration Effects

In addition to the SI effects, multiple chip select topologies change the way that the FPGA calibrates to the memories. In single-rank situations with leveling, the calibration algorithms set delay chains in the FPGA such that specific DQ and DQS pin delays from the memory are equalized (only for ALTMEMPHY-based designs at 401 MHz and above) so that the write-leveling and resynchronization timing requirements are met. In single rank without leveling situations, the calibration algorithm centers the resynchronization or capture phase such that it is optimum for the single rank. When there are two or more ranks in a system, the calibration algorithms must calibrate to the average point of the ranks.

Board Effects

Unequal length PCB traces result in delays reducing timing margins. Furthermore, skews between different memory ranks can further reduce the timing margins in multiple chip select topologies. Board skews can also affect the extent to which the FPGA can calibrate to the different ranks. If the skew between various signals for different ranks is large enough, the timing margin on the fully calibrated paths such as write leveling and resynchronization changes.

To account for all these board effects for Arria II GX, Arria II GZ, Arria V, Cyclone V, Stratix IV, and Stratix V devices, refer to the **Board Settings** page in the ALTMEMPHY- or UniPHY-based controller parameter editors.

 To perform multiple chip select timing deration for other Altera devices (for example Cyclone III and Stratix III devices), use the Excel-based calculator available from the [Altera website](#).


Timing Deration using the Board Settings

When you target Arria II GX, Arria II GZ, Arria V, Cyclone V, Stratix IV, or Stratix V devices, the ALTMEMPHY- or UniPHY-based parameter editors include the **Board Settings** page, to automatically account for the timing deration caused by the multiple chip selects in your design.

When you target Cyclone III or Stratix III devices, you can derate single chip-select designs using the parameter editors to account for the skews, ISI, and slew rates in the **Board Settings** page.

If you are targeting Cyclone III or Stratix III devices you see the following warning:

```
"Warning: Calibration performed on all chip selects, timing analysis only performed on first chip select. Manual timing derating is required"
```

 You must perform manual timing deration using the Excel-based calculator.

The **Board Settings** page allows you to enter the parameters related to the board design including skews, signal integrity, and slew rates. The **Board Settings** page also includes the board skew setting parameter, **Addr/Command to CK skew**, (previously on the **PHY Settings** tab).

Slew Rates

You can obtain the slew rates in one of the following ways:

- Altera performs PCB simulations on internal Altera boards to compute the output slew rate and ISI effects of various multiple chip select configurations. These simulation numbers are prepopulated in the **Slew Rates** based on the number of ranks selected. The address and command setup and hold times (tDS, tDH, tIS, tIH) are then computed from the slew rate values and the baseline nonderated tDS, tDH, tIS, tIH numbers entered in the **Preset Editor**. The parameter editor shows the computed values in **Slew Rates**. If you do not have access to a simulator to obtain accurate slew rates for your specific system, Altera recommends that you use these prepopulated numbers for an approximate estimate of your actual board parameters.

- Alternatively, you can update these default values, if dedicated board simulation results are available for the slew rates. Custom slew rates cause the t_{DS} , t_{DH} , t_{IS} , t_{IH} values to be updated. Altera recommends performing board level simulations to calculate the slew rate numbers that accounts for accurate board-level effects for your board.
- You can modify the auto-calculated t_{DS} , t_{DH} , t_{IS} , t_{IH} values with more accurate dedicated results direct from the vendor data sheets, if available.

Slew Rate Setup, Hold, and Derating Calculation

Slew rate is calculated based on the nominal slew rate for setup and hold times. The total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the Micron data sheet t_{IS} (base) and t_{IH} (base) values to the delta t_{IS} and delta t_{IH} derating values, respectively.

For more information about slew rate calculation, setup, hold, and derating values, download the data sheet specifications from the following vendor websites:

- Micron (www.micron.com)
For example, refer to *Command and Address Setup, Hold, and Derating* section in the [Micron DDR3 data sheet](#).
- JEDEC (www.jedec.org)
For example, refer to the [DDR2 SDRAM Standard data sheet](#).

The following section describes the timing derating algorithms and shows you where to obtain the setup, hold, and derating values in the Micron datasheet.

The slew rate derating process uses the following timing derating algorithms, which is similar to the JEDEC specification:

$$t_{DS} = t_{DS}(\text{base}) + \text{delta } t_{DS} + (V_{IHAC} - V_{REF}) / (\text{DQ slew rate})$$

$$t_{DH} = t_{DH}(\text{base}) + \text{delta } t_{DH} + (V_{IHDC} - V_{REF}) / (\text{DQ slew rate})$$

$$t_{IS} = t_{IS}(\text{base}) + \text{delta } t_{IS} + (V_{IHAC} - V_{REF}) / (\text{Address/Command slew rate})$$

$$t_{IH} = t_{IH}(\text{base}) + \text{delta } t_{IH} + (V_{IHDC} - V_{REF}) / (\text{Address/Command slew rate})$$

where:

- a. The setup and hold values for $t_{DS}(\text{base})$, $t_{DH}(\text{base})$, $t_{IS}(\text{base})$, and $t_{IH}(\text{base})$ are obtained from the Micron datasheet.

Figure 10-21 shows a screenshot example of the values from the Micron datasheet.

Figure 10-21. Setup and Hold Values from Micron Datasheet

Parameter	Symbol	DDR3-800		DDR3-1066		
		Min	Max	Min	Max	
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification)	t_{DS}	75	–	25	–
	$V_{REF} @ 1 \text{ V/ns}$	AC175	250	–	200	–
Data setup time to DQS, DQS#	Base (specification)	t_{DS}	125	–	75	–
	$V_{REF} @ 1 \text{ V/ns}$	AC150	275	–	250	–
Data setup time to DQS, DQS#	Base (specification)	t_{DS}	–	–	–	–
	$V_{REF} @ 1 \text{ V/ns}$	AC135	–	–	–	–
Data hold time from DQS, DQS#	Base (specification)	t_{DH}	150	–	100	–
	$V_{REF} @ 1 \text{ V/ns}$	DC100	250	–	200	–
Minimum data pulse width	t_{DIPW}		600	–	490	–
Command and Address Timing						
DLL locking time	t_{DLLK}		512	–	512	–
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	t_{IS}	200	–	125	–
	$V_{REF} @ 1 \text{ V/ns}$	AC175	375	–	300	–
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	t_{IS}	350	–	275	–
	$V_{REF} @ 1 \text{ V/ns}$	AC150	500	–	425	–
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	t_{IH}	275	–	200	–
	$V_{REF} @ 1 \text{ V/ns}$	DC100	375	–	300	–
Minimum CTRL, CMD, ADDR pulse width	t_{IPW}		900	–	780	–

- b. The JEDEC defined logic trip points for DDR3 SDRAM memory standard are as follow:

- $V_{IHAC} = V_{REF} + 0.175 \text{ V}$
- $V_{IHDC} = V_{REF} + 0.1 \text{ V}$
- $V_{ILAC} = V_{REF} - 0.175 \text{ V}$
- $V_{ILDC} = V_{REF} - 0.1 \text{ V}$

- c. The derating values for Δt_{IS} , t_{IH} , t_{DH} , and t_{DS} are obtained from the Micron data sheet.
Figure 10-22 shows the screenshot of the derating values from the Micron data sheet.

Figure 10-22. Derating Values from Micron Datasheet

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based AC175 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 175mV$, $V_{IL(AC)} = V_{REF(DC)} - 175mV$												
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate											
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	88	50	88	50	88	50	96	58	104	66	112	74
1.5	59	34	59	34	59	34	67	42	75	50	83	58
1.0	0	0	0	0	0	0	8	8	16	16	24	24
0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20
0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14
0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8
0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2
0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16
0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36


Shaded cells indicate slew rate combinations not supported

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based												
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate											
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	88	50	88	50	88	50						
1.5	59	34	59	34	59	34	67	42				
1.0	0	0	0	0	0	0	8	8	16	16		
0.9			-2	-4	-2	-4	6	4	14	12	22	20
0.8					-6	-10	2	-2	10	6	18	14
0.7							-3	-8	5	0	13	8
0.6									-1	-10	7	-2
0.5											-11	-16
0.4												

Intersymbol Interference

ISI parameters are similarly auto-populated based on the number of ranks you select with Altera's PCB simulations. You can update these autopopulated typical values, if more accurate dedicated simulation results are available.

Altera recommends performing board-level simulations to calculate the slew rate and ISI deltas that account for accurate board level effects for your board. You can use HyperLynx or similar simulators to obtain these simulation numbers. The default values have been computed using HyperLynx simulations for Altera boards with multiple DDR2 and DDR3 SDRAM slots.

 For DQ and DQS ISI there is one textbox for the total ISI, which assumes symmetric setup and hold. For address and command, there are two textboxes: one for ISI on the leading edge, and one for the lagging edge, to allow for asymmetric ISI.

The wizard writes these parameters for the slew rates and the ISI into the `.sdc` and they are used during timing analysis.

Board Skews

Table 10-10 lists the types of board skew.

Table 10-10. Board Skews

Board Skew		Description
ALTMEMPHY	UniPHY	
Minimum CK/DQS skew to DIMM	—	The largest negative skew that exists between the CK signal and any DQS signal when arriving at any rank. This value affects the write leveling margin for DDR3 SDRAM DIMM interfaces in multiple chip select configurations only.
Maximum CK/DQS skew to DIMM	—	The maximum skew (or largest positive skew) between the CK signal and any DQS signal when arriving at any rank. This value affects the write leveling margin for DDR3 SDRAM DIMM interfaces in multiple chip select configurations.
Maximum skew between DIMMs	Maximum delay difference between DIMMs/devices	The largest skew or propagation delay between ranks (especially for different ranks in different slots). This value affects the resynchronization margin for DDR2 and DDR3 SDRAM interfaces in multiple chip select configurations.
Maximum skew within DQS group	Maximum skew within DQS group	The largest skew between DQ pins in a DQS group. This value affects the read capture and write margins for DDR2 and DDR3 SDRAM interfaces.
Maximum skew between DQS groups	Maximum skew between DQS groups	The largest skew between DQS signals in different DQS groups. This value affects the resynchronization margin in non-leveled memory interfaces such as DDR2 and DDR3 SDRAM.
Address and command to CK skew	Maximum delay difference between Address/Command and CK	The skew (or propagation delay) between the CK signal and the address and command signals. Positive values represent address and command signals that are longer than CK signals; negative values represent address and command signals that are shorter than CK signals. The Quartus II software uses this skew to optimize the delay of the address and command signals to have appropriate setup and hold margins for DDR2 and DDR3 SDRAM interfaces.
—	Maximum skew within Address/Command bus	The largest skew between the Address/Command signals.

Measuring Eye Reduction for Address/Command, DQ, and DQS Setup and Hold Time

This section describes how to measure eye reduction for address/command, DQ, and DQS. This section describes how to measure eye reduction for address/command, DQ, and DQS.

Address/Command

The setup and hold times for address/command eye reduction is measured by comparing both the multirank and single rank address/command timing window as shown in Figure 10-24. Relative to the single rank address/command timing window, the reduction of the eye opening on the left side of the window denotes the setup time, while the reduction of the eye opening on the right side denotes the hold time.

To obtain the address/command eye reduction (setup time), measure the $V_{IL(AC)}$ or $V_{IH(AC)}$ difference between the single rank and multirank timing window, denoted by A in Figure 10-23 and Figure 10-24.

To obtain the address/command eye reduction (hold time), measure the $V_{IL(DC)}$ or $V_{IH(DC)}$ difference between the single rank and multirank timing window, denoted by B in Figure 10-23 and Figure 10-24.

Figure 10-23. Difference between Single Rank and Multirank Timing Window for Address/Command Eye Reduction (Setup)

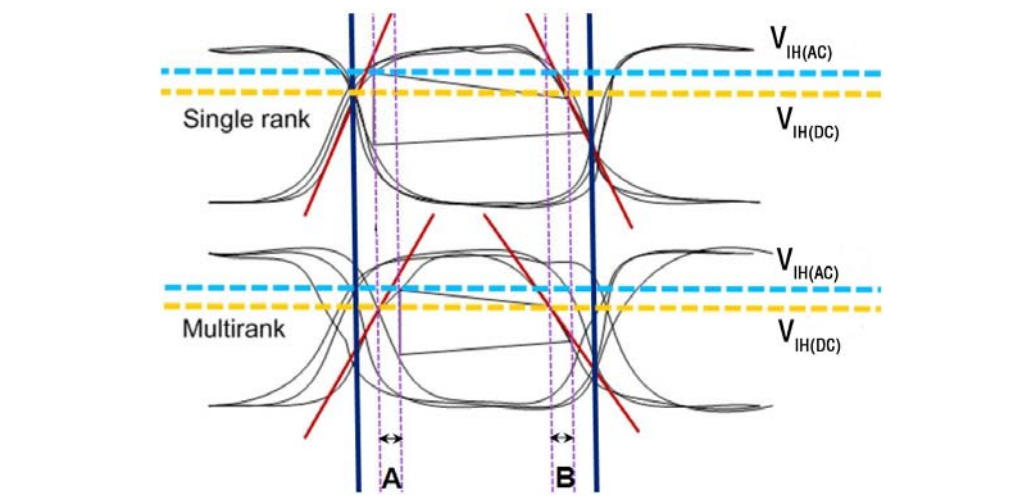
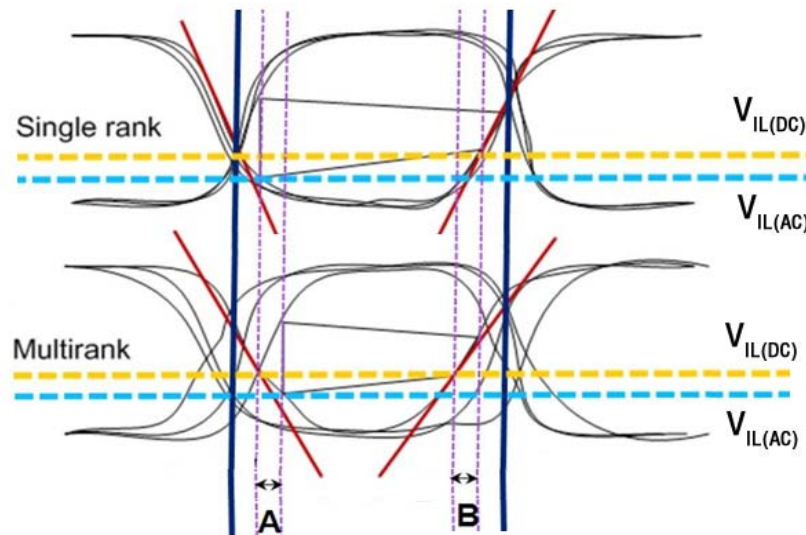


Figure 10-24. Difference between Single Rank and Multirank Timing Window for Address/Command Eye Reduction (Hold)



For signals with multiple loads, look at the measurements for all the target locations and pick the worst case eye width in all cases. For example, if pin A7 is the worst case eye width from pins A0 to A14, then the A7 measurement is used for the address signal. In general, look for eye reduction for the worst-pin in single-rank as compared to the worst-pin in multirank regardless of whether the pin is the same pin or a different pin.

DQ

The method to measure the DQ eye reduction is similar to the method you use to measure the command/address eye reduction. To measure the DQ eye reduction hold time, compare $V_{IH(DC)}$ or $V_{IL(DC)}$ between the single rank and multirank timing window. To measure the DQ eye reduction setup time, compare $V_{IH(AC)}$ or $V_{IL(AC)}$ between the single rank and multirank timing window.

DQS

DQS arrival time is the jitter before and after the single-rank timing window that you must enter in the GUI. The DQS arrival time is indicated by the DQS signal eye reduction between the signal rank system and multiple chip selects. Therefore, the method to measure the DQS arrival time is similar to the method you use to measure the command/address and DQ eye reduction.

ISI and Board Skew

Skews are systematic effects that are not time-varying, while ISI values are time- and pattern-dependent varying margin reduction.

In the `.sdc`, the address/command eye reduction is applied as an output delay constraint on the setup side and on the hold side, respectively.

For the write analysis, the eye reduction in DQ is applied as an output delay constraint, with half on the setup side and half on the output side. Similarly, the extra variation in the DQS is also applied as an output delay constraint with half

removed from the setup side and half removed from the hold side.

The board skews are included in the timing margin on the fully calibrated path such as write-leveling and resynchronization. Both the ISI and board skews values are entered to ensure that the interfaces are not over constraint.

Timing Deration Using the Excel-Based Calculator

To perform multiple chip select timing deration for other Altera devices (for example Stratix III and Cyclone III devices), use the Excel-based calculator, which is available from the [Altera web site](#). You can also derate single chip-select cases using the Excel based calculator for devices that do not have the board settings panel provided you have the board simulation data to account for the ISI, skew and slew rate information.

The Excel-based calculator requires data like the slew rate, eye reduction, and the board skews of your multiple chip select system as inputs and outputs the final result based on built-in formula.

The calculator requires the Quartus II timing results (report DDR section) from the single rank version of your system. Two simulations are also required for the slew rate and ISI information required by the calculator: a baseline single rank version of your system and your multiple chip select system. The calculator uses the timing deltas of these simulation results for the signals of interest (DQ, DQS, CK/CK#, address and command, and CS). You must enter board skews for your specific board. The calculator outputs the final derated timing margins, which provides a full analysis of your multiple chip select system's performance.

The main assumption for this flow is that you have board trace models available for the single rank version of your system. If you have these board trace models, the Quartus II software automatically derates the effects for the single rank case correctly. Hence the Excel-based calculator provides the deration of the supported single-rank timing analysis, assuming that the single rank version has provided an accurate baseline.

You must ensure that the single rank board trace models are included in your Quartus II project so that the baseline timing analysis is accurate. If you do not have board trace models, follow the process described at the end of this section.

Before You Use the Excel-based Calculator for Timing Deration

Ensure you have the following items before you use the Excel-based calculator for timing deration:

1. A Quartus II project with your instantiated memory IP. Always use the latest version of the Quartus II software, for the most accurate timing models.
2. The board trace models for the single rank version of your system.



If you do not have board trace models, refer to “[Using the Excel-based Calculator for Timing Deration \(Without Board Trace Models\)](#)” on page 10-55.

Using the Excel-Based Calculator

To obtain derated timing margins for multiple chip select designs using the Excel-based calculator, follow these steps:

1. Create a memory interface design in the Quartus II software.
2. Ensure board trace models are specified for your single rank system. Extract Quartus II reported timing margins into the Excel-based calculator.
3. Use the slow 85C model timing results (Figure 10-25).


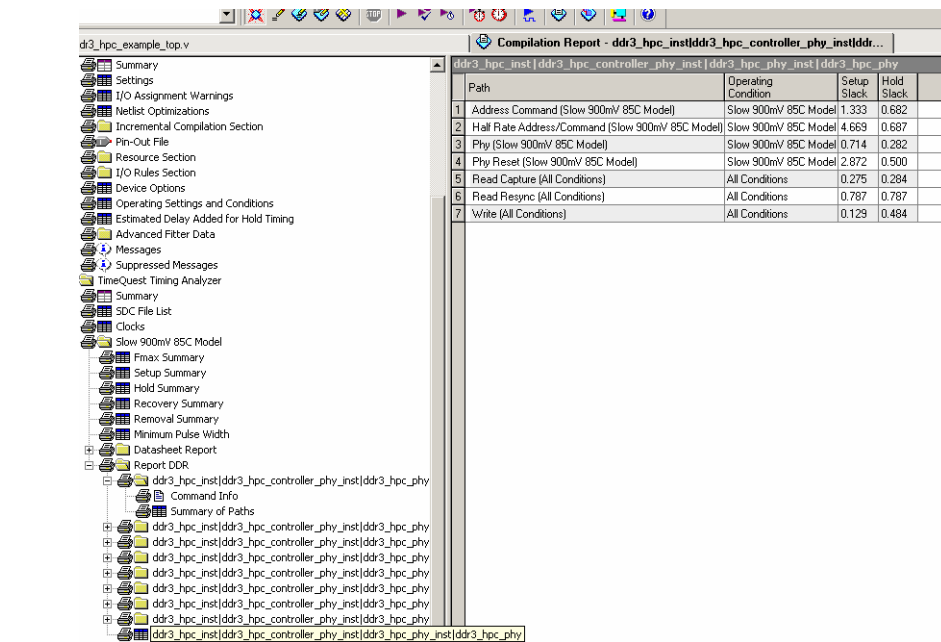
 Use the worst-case values from all corners, which means that some values may come from different corners. For example, a setup value may come from the slow 85C model, while the hold value for the same metric may come from the fast 0C model. In most cases, using the slow 85C model should be accurate enough.

Figure 10-25. Quartus II Report DDR Section Timing Results for the Slow 85C Model



Path	Operating Condition	Setup Slack	Hold Slack
1 Address Command (Slow 900mV 85C Model)	Slow 900mV 85C Model	1.333	0.682
2 Half Rate Address/Command (Slow 900mV 85C Model)	Slow 900mV 85C Model	4.669	0.687
3 PhY (Slow 900mV 85C Model)	Slow 900mV 85C Model	0.714	0.282
4 PhY Reset (Slow 900mV 85C Model)	Slow 900mV 85C Model	2.872	0.500
5 Read Capture (All Conditions)	All Conditions	0.275	0.284
6 Read Resync (All Conditions)	All Conditions	0.787	0.787
7 Write (All Conditions)	All Conditions	0.129	0.484

4. Enter the Report DDR results from Quartus II timing analysis into the Excel-based calculator (Figure 10-26).

Figure 10-26. Calculator

Multi-Chip Select Calculator for DDR3		
1. Results obtained from Quartus		
Path	Setup Slack	Hold Slack
Address Command	0.374	0.197
Half Rate Address/Command	2.234	0.193
Phy	0.136	0.025
Phy Reset	0.176	0.291
Read Capture	0.019	0.03
Read Resync	0.169	0.169
Write	0.016	0.007
Write Leveling tDQSS	0.149	0.099
Write Leveling tDSS/tDSH	0.005	0.135

5. Perform PCB SI simulations to get the following values:
 - Single rank eye width and topology eye width for data, strobe, and address and command signals.
 - Multiple chip select topology slew rates for clock, address and command, and data and strobe signals.

Table 10-11 lists the data rates and recommended stimulus patterns for various signals and memory interface types.


 Use a simulation tool (for example, HyperLynx), if you have access to the relevant input files that the tool requires, or use prelayout line simulations if the more accurate layout information is not available.

Table 10-11. Data Rates and Stimulus Patterns

Memory Interface	CLK and DQS Toggling Pattern (MHz)	DQ PRBS Pattern (MHz)	Address and Command PRBS Pattern (MHz)
DDR2 SDRAM (with a half-rate controller)	400	400	100
DDR2 SDRAM (with a full-rate controller)	300	300	150
DDR3 SDRAM (with a half-rate controller)	533	533	133

6. Calculate the deltas to enter into the Excel-based calculator. For example, if DQ for the single rank case is 853.682 ps and DQ for the dual rank case is 805.137 ps, enter 48 ps into the calculator (Figure 10-27).


 For signals with multiple loads, look at the measurements at all the target locations and pick the worst case eye width in all cases. For example, for the address bus, if A7 is the worst case eye width from pins A0 to A14, use that measurement for the address signal.

Figure 10-27. ISI and Slew Rate Values

Intersymbol Interference	
Path	Time (in ns)
Address Command eye reduction on the setup	0.013
Address Command eye reduction on the hold	0.013
DQ eye reduction	0.048
Variation in DQS arrival time	0.003
Slew Rates Deration	
Path	V/ns
DQ	1
DQS (differential)	2
Address/Command	1
CK (differential)	2
extra tDS	0
extra tDH	0
extra tIS	0
extra tIH	0

7. Enter the topology slew rates into the slew rate deration section. The calculator calculates the extra tDS, tDH, tIS, tIH values.

- Obtain the board skew numbers for your PCB from either your board simulation or from your PCB vendor and enter them into the calculator (Figure 10-28).

Figure 10-28. Board Skew Values

Board Skews	
Path	Time (in ns)
Maximum skew between DIMMs	0.05
Minimum CK/DQS to one DIMM	0.01
Maximum CK/DQS to one DIMM	0.03

The Excel-based calculator then outputs the final derated numbers for your multiple chip select design.

Figure 10-29. Derated Setup and Hold Values

Final Multi Chip Select Results		
Path	Setup Slack	Hold Slack
Address Command	0.361	0.184
Half Rate Address/Command	2.228	0.187
Phy	0.136	0.025
Phy Reset	0.176	0.291
Read Capture	0.019	0.030
Read Resync	0.119	0.119
Write	-0.010	-0.019
Write Leveling tDQSS	0.126	0.076
Write Leveling tDSS/DSH	-0.018	0.112

These values are an accurate calculation of your multiple chip select design timing, assuming the simulation data you provided is correct. In this example, there is negative slack on some of the paths, so this design does not pass timing. You have the following four options available:

- Try to optimize margins and see if it improves timing (for example modify address and command phase setting)
- Lower the frequency of your design
- Lower the loading (change the topology of your interface to lower the loading and skew)
- Use a faster DIMM

Using the Excel-based Calculator for Timing Deration (Without Board Trace Models)

If board trace models are not available for any of the signals of the single rank system, follow these steps:

- Create a new Quartus II Project with the Stratix III or Cyclone III device that you are targeting and instantiate a High-Performance SDRAM Controller for your memory interface.
- Do not enter the board trace models (assumes a 0-pf load) and compile the Quartus II design.
- Enter the Report DDR setup and hold slack numbers into the Excel-based calculator.

4. Perform a prelayout line simulation of a 0-pf load simulation and obtain eye width and slew rate numbers. Perform multiple chip select simulations of your topology and use the Excel-based calculator.

Performing I/O Timing Analysis

For accurate I/O timing analysis, the Quartus II software must be made aware of the board trace and loading information. This information must be derived and refined during your PCB development process of pre-layout (line) and post-layout (board) simulations.

For external memory interfaces that use memory modules (DIMMs), the board trace and loading information must include the trace and loading information of the module in addition to the main and host platform, which you can obtain from your memory vendor.

You can use the following I/O timing analysis methods for your memory interface:

- [Perform I/O Timing Analysis with 3rd Party Simulation Tools](#)
- [Perform Advanced I/O Timing Analysis with Board Trace Delay Model](#)

Perform I/O Timing Analysis with 3rd Party Simulation Tools

Altera recommends that you perform I/O timing analysis using the 3rd party simulation tool flow because this flow involves post layout simulation that can capture more accurate I/O timing. This method is also easier because it only requires you to enter the slew rates, board skews, and ISI values in the ALTMEMPHY or UniPHY IP parameter editor.

To perform I/O timing analysis using 3rd party simulation tools, follow these steps:

1. Use a 3rd party simulation tool such as HyperLynx to simulate the full path for DQ, DQS, CK, Address, and Command signals.
2. Under the **Board Settings** tab of the ALTMEMPHY or UniPHY parameter editor, enter the slowest slew rate, ISI, and board skew values.

Perform Advanced I/O Timing Analysis with Board Trace Delay Model

You should use this method only if you are unable to perform post-layout simulation on the memory interface signals to obtain the slew rate parameters, and/or when no simulation tool is available.

To perform I/O timing analysis using board trace delay model, follow these steps:

1. After the instantiation is complete, analyze and synthesize your design.
2. Add pin and DQ group assignment by running the `<variation_name>_p0_pin_assignments.tcl` script.



The naming of the pin assignment file may vary depending on the Quartus II software version that you are using.

3. Enter the pin location assignments.
4. Assign the virtual pins, if necessary.

5. Enter the board trace model information. To enter board trace model information, follow these steps:
 - a. In the Pin Planner, select the pin or group of pins for which you want to enter board trace parameters.
 - b. Right-click and select **Board Trace Model**.
6. Compile your design. To compile the design, on the Processing menu, click **Start Compilation**.
7. After successfully compiling the design, perform timing analysis in the TimeQuest timing analyzer. To perform timing analysis, follow these steps:
 - a. In the Quartus II software, on the Tools menu, click **TimeQuest Timing Analyzer**.
 - b. On the **Tasks** pane, click **Report DDR**.
 - c. On the **Report** pane, select **Advanced I/O Timing>Signal Integrity Metrics**.
 - d. In the **Signal Integrity Metrics** window, right-click and select **Regenerate** to regenerate the signal integrity metrics.
 - e. In the **Signal Integrity Metrics** window, note the 10–90% rise time (or fall time if fall time is worse) at the far end for CK/CK#, address, and command, DQS/DQS#, and DQ signals.
 - f. In the DDR3 SDRAM controller parameter editor, in the **Board Settings** tab, type the values you obtained from the signal integrity metrics.
 - g. For the board skew parameters, set the maximum skew within DQS groups of your design. Set the other board parameters to 0 ns.
 - h. Compile your design.

Document Revision History

Table 10–12 lists the revision history for this document.

Table 10–12. Document Revision History

Date	Version	Changes
November 2011	4.0	<ul style="list-style-type: none"> ■ Added Arria V and Cyclone V information. ■ Added Performing I/O Timing Analysis section. ■ Added Measuring Eye Reduction for Address/Command, DQ, and DQS Setup and Hold Time section.
June 2011	3.0	Updated for 11.0 release.
December 2010	2.1	Added Arria II GZ and Stratix V, updated board skews table.
July 2010	2.0	Added information about UniPHY-based IP and controllers.
January 2010	1.2	Corrected minor typos.
December 2009	1.1	Added <i>Timing Deration</i> section.
November 2009	1.0	First published.