

Latency is defined using the local (user) side frequency and absolute time (ns). There are two types of latencies that exist while designing with memory controllers—read and write latencies, which have the following definitions:

- Read latency—the amount of time it takes for the read data to appear at the local interface after initiating the read request.
- Write latency—the amount of time it takes for the write data to appear at the memory interface after initiating the write request.



For a half-rate controller, the local side frequency is half of the memory interface frequency. For a full-rate controller, the local side frequency is equal to the memory interface frequency.

Altera defines read and write latencies in terms of the local interface clock frequency and by the absolute time for the memory controllers. These latencies apply to supported device families with half-rate and full-rate HPC II memory controllers.

The latency defined in this section uses the following assumptions:

- The row is already open, there is no extra bank management needed.
- The controller is idle, there is no queued transaction pending, indicated by the `local_ready` signal asserted high.
- No refresh cycles occur before the transaction.

Latency Stages

The latency for the high-performance controller II comprises many different stages of the memory interface. Figure 14-1 shows a typical memory interface read latency path showing read latency from the time a `local_read_req` signal assertion is detected by the controller up to data available to be read from the dual-port RAM (DPRAM) module.

Figure 14-1. Typical Latency Path

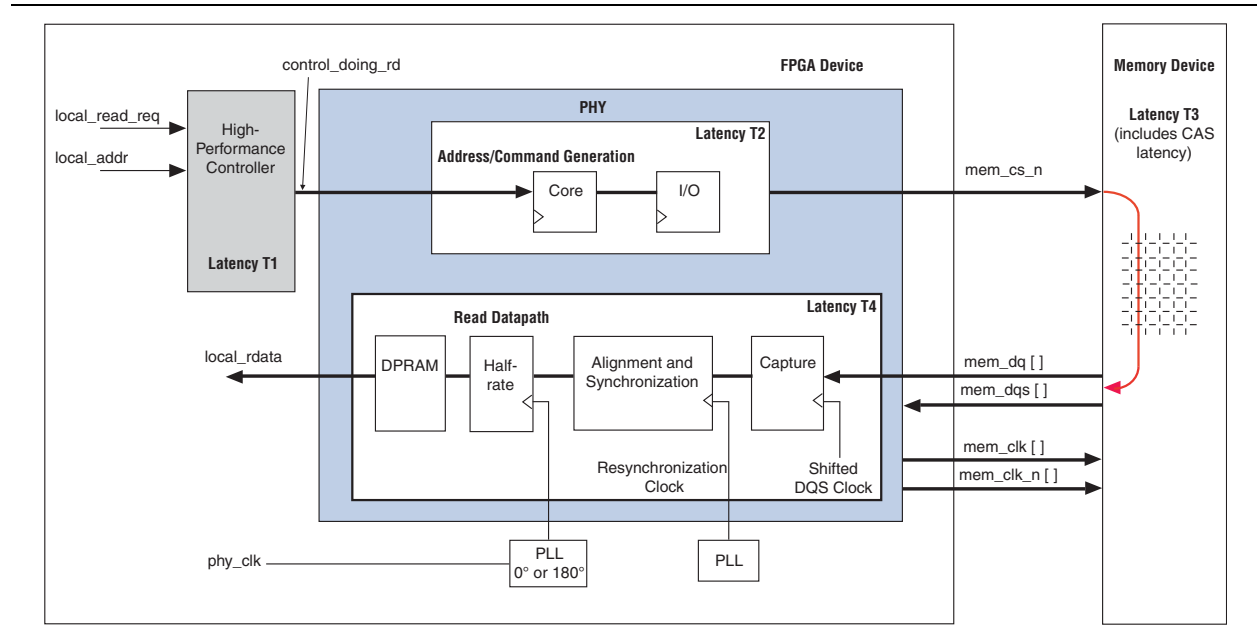


Table 14-1 shows the different stages that make up the whole read and write latency that Figure 14-1 shows.

Table 14-1. High-Performance Controller Latency Stages and Descriptions

Latency Number	Latency Stage	Description
T1	Controller	<code>local_read_req</code> or <code>local_write_req</code> signal assertion to <code>ddr_cs_n</code> signal assertion.
T2	Command Output	<code>ddr_cs_n</code> signal assertion to <code>mem_cs_n</code> signal assertion.
T3	CAS or WL	Read command to DQ data from the memory or write command to DQ data to the memory.
T4	ALTMEMPHY read data input	Read data appearing on the local interface.
T2 + T3	Write data latency	Write data appearing on the memory interface.

From Figure 14-1, the read latency in the high-performance controllers is made up of four components:

$$\text{read latency} = \text{controller latency (T1)} + \text{command output latency (T2)} + \text{CAS latency (T3)} + \text{PHY read data input latency (T4)}$$

Similarly, the write latency in the high-performance controller II is made up of three components:

$$\text{write latency} = \text{controller latency (T1)} + \text{write data latency (T2+T3)}$$

You can separate the controller and ALTMEMPHY read data input latency into latency that occurred in the I/O element (IOE) and latency that occurred in the FPGA fabric.

Table 14-2 shows the minimum and maximum supported CAS latency for the DDR and DDR2 SDRAM high-performance controller II.

Table 14-2. Supported CAS Latency ⁽¹⁾

Device Family	Minimum Supported CAS Latency		Maximum Supported CAS Latency	
	DDR	DDR2	DDR	DDR2
Arria GX	3.0	3.0	3.0	6.0
Arria II GX	3.0	3.0	3.0	6.0
Cyclone III	2.0	3.0	3.0	6.0
Cyclone IV	2.0	3.0	3.0	6.0
HardCopy III	3.0	3.0	3.0	6.0
HardCopy IV	3.0	3.0	3.0	6.0
Stratix II	3.0	3.0	3.0	6.0
Stratix III	3.0	3.0	3.0	6.0
Stratix IV	3.0	3.0	3.0	6.0

Note to Table 14-2:

- (1) The registered DIMMs, where supported, effectively introduce one extra cycle of CAS latency. For the registered DIMMs, you need to subtract 1.0 from the CAS figures to determine the minimum supported CAS latency, and add 1.0 to the CAS figures to determine the maximum supported CAS latency.

Table 14-3 and Table 14-4 show a typical latency that can be achieved in Arria GX, Arria II GX, Cyclone III, Cyclone IV, Stratix IV, Stratix III, Stratix II, and Stratix II GX devices. The exact latency for your memory controller depends on your precise configuration. You can obtain precise latency from simulation, but this figure can vary slightly in hardware because of the automatic calibration process.

The actual memory CAS and write latencies shown are halved in half-rate designs as the latency calculation is based on the local clock.

The read latency also depends on your board trace delay. The latency found in simulation can be different from that found in board testing as functional simulation does not take into account the board trace delays. For a given design on a given board, the latency may change by one clock cycle (for full-rate designs) or two clock cycles (for half-rate designs) upon resetting the board. Different boards could also show different latencies even with the same design.

The CAS and write latencies are different between DDR and DDR2 SDRAM interfaces. To calculate latencies for DDR SDRAM interfaces, use the numbers from DDR2 SDRAM listed below and replace the CAS and write latency with the DDR SDRAM values.

Table 14-3. Typical Read Latency in HPC II ⁽¹⁾, ⁽²⁾

Device	Frequency (MHz)	Interface	Controller Latency ⁽³⁾	Address and Command Latency		CAS Latency ⁽⁴⁾	Read Data Latency		Total Read Latency ⁽⁵⁾	
				FPGA	I/O		FPGA	I/O	Local Clock Cycles	Time (ns)
Arria GX	233	Half-rate	5	3	1	2	4.5	1	18	154
	167	Full-rate	5	2	1	4	5	1	19	114
Arria II GX	233	Half-rate	5	3	1	2.5	5.5	1	18	154
	167	Full-rate	5	2	1	4	6	1	20	120
Cyclone III and Cyclone IV	200	Half-rate	5	3	1	2	4.5	1	18	180
	167	Full-rate	5	2	1	4	5	1	19	114
Stratix II and Stratix II GX	333	Half-rate	5	3	1	2	4.5	1	18	108
	267	Half-rate	5	3	1	2	4.5	1	18	135
	200	Full-rate	5	2	1	4	5	1	19	95
Stratix III and Stratix IV	400	Half-rate	5	3	1	2.5	7.125	1.5	20	100
	267	Full-rate	4	2	1.5	4	7	1	20	75

Notes to Table 14-3:

- (1) These are typical latency values using the assumptions listed in the beginning of the section. Your actual latency may be different than shown. Perform your own simulation for your actual latency.
- (2) Numbers shown may have been rounded up to the nearest higher integer.
- (3) The controller latency value is from the Altera high-performance controller.
- (4) CAS latency is per memory device specification and is programmable in the MegaWizard Plug-In Manager.
- (5) Total read latency is the sum of controller, address and command, CAS, and read data latencies.

Table 14-4. Typical Write Latency in HPC II ⁽¹⁾, ⁽²⁾ (Part 1 of 2)


Device	Frequency (MHz)	Interface	Controller Latency ⁽³⁾	Address and Command Latency		Memory Write Latency ⁽⁴⁾	Total Write Latency ⁽⁵⁾	
				FPGA	I/O		Local Clock Cycles	Time (ns)
Arria GX	233	Half-rate	5	3	1	1.5	12	103
	167	Full-rate	5	2	1	3	12	72
Arria II GX	233	Half-rate	5	3	1	2.5	12	103
	167	Full-rate	5	2	1	4	12	72
Cyclone III and Cyclone IV	200	Half-rate	5	3	1	1.5	12	120
	167	Full-rate	5	2	1	3	12	72

Table 14–4. Typical Write Latency in HPC II ⁽¹⁾, ⁽²⁾ (Part 2 of 2)

Device	Frequency (MHz)	Interface	Controller Latency ⁽³⁾	Address and Command Latency		Memory Write Latency ⁽⁴⁾	Total Write Latency ⁽⁵⁾	
				FPGA	I/O		Local Clock Cycles	Time (ns)
Stratix II and Stratix II GX	333	Half-rate	5	3	1	1.5	12	72
	267	Half-rate	5	3	1	1.5	12	90
	200	Full-rate	5	2	1	3	12	60
Stratix III and Stratix IV	400	Half-rate	5	3	1	2	12	60
	267	Full-rate	5	2	1.5	3	13	49

Notes to Table 14–4:

- (1) These are typical latency values using the assumptions listed in the beginning of the section. Your actual latency may be different than shown. Perform your own simulation for your actual latency.
- (2) Numbers shown may have been rounded up to the nearest higher integer.
- (3) The controller latency value is from the Altera high-performance controller.
- (4) Memory write latency is per memory device specification. The latency from when you provide the command to write to when you need to provide data at the memory device.
- (5) Total write latency is the sum of controller, address and command, and memory write latencies.

 To see the latency incurred in the IOE for both read and write paths for ALTMEMPHY variations in Stratix IV and Stratix III devices refer to the IOE figures in the *External Memory Interfaces in Stratix III Devices* chapter of the *Stratix III Device Handbook* and the *External Memory Interfaces in Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

Document Revision History

Table 14–5 lists the revision history for this document.

Table 14–5. Document Revision History

Date	Version	Changes
November 2011	1.0	Consolidated latency information from 11.0 DDR and DDR2 SDRAM Controller with ALTMEMPHY IP User Guide , and DDR3 SDRAM Controller with ALTMEMPHY IP User Guide .

