

Built on the 28-nm low-power process technology, Arria® V devices offer the lowest power and lowest system cost for mainstream applications. Arria V devices include unique innovations such as the lowest static power in its class, the lowest power transceivers of any midrange family, support for serial data rates up to 10.3125 gigabits per second (Gbps), a powerful collection of integrated hard intellectual property (IP), and a power-optimized core architecture, making Arria V devices ideal for the following applications:

- Power sensitive wireless infrastructure equipment
- 20G/40G bridging, switching, and packet processing applications
- High-definition video processing and image manipulation
- Intensive digital signal processing (DSP) applications

Arria V devices are available in the following variants:

- Arria V GX—FPGA with integrated 6-Gbps transceivers, this variant provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications.
- Arria V GT—FPGA with integrated 10-Gbps transceivers, this variant provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications.
- Arria V SX—system-on-a-chip (SoC) FPGA with integrated Arria V FPGA and ARM®-based hard processor system (HPS).
- Arria V ST—SoC FPGA with integrated Arria V FPGA, ARM-based HPS, and 10-Gbps transceivers.

The Arria V SoC FPGA variants feature an FPGA integrated with an HPS that consists of a dual-core ARM Cortex™-A9 MPCore™ processor, a rich set of peripherals, and a shared multiport SDRAM memory controller.

The unique feature set in Arria V devices was chosen to optimize power, cost, and performance. These features include a redesigned adaptive logic module (ALM), distributed memory, new 10-Kbit (M10K) internal memory blocks, variable-precision DSP blocks, and fractional clock synthesis phase-locked loops (PLLs) with a highly flexible clocking network, all interconnected by a power-optimized MultiTrack routing architecture.

Arria V devices provide interface support flexibility with up to 10-Gbps transceivers, 1.25-Gbps LVDS, 1.333-Gbps memory interfaces with low latency, and support for all mainstream single-ended and differential I/O standards, including 3.3 V. Arria V devices also offer the lowest system cost by requiring only three power supplies to operate the devices and a thermal composite flip chip ball-grid array (BGA) packaging option. Arria V devices also support innovative features, such as configuration via protocol (CvP), partial reconfiguration, and design security.

Arria V devices provide the power, features, and cost you require to succeed with your designs. With these innovations, Arria V devices deliver ideal performance and capability for a wide range of applications.

## Arria V Feature Summary

Table 1-1 lists the Arria V device features.

**Table 1-1. Feature Summary for Arria V Devices (Part 1 of 3)**

Feature	Details
Technology	<ul style="list-style-type: none"> <li>■ 28-nm TSMC low-power process technology</li> <li>■ Lowest static power in its class (less than 800 mW for 500 K logic elements (LEs) at 85°C junction under typical conditions)</li> <li>■ 1.1-V core nominal voltage</li> </ul>
Lowest-power serial transceivers of any midrange FPGA	<ul style="list-style-type: none"> <li>■ 611-Mbps to 10.3125-Gbps integrated transceivers</li> <li>■ Transmit pre-emphasis and receiver equalization</li> <li>■ Dynamic reconfiguration of individual channels</li> </ul>
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>■ 1.25-Gbps LVDS</li> <li>■ 667-MHz/1.333-Gbps external memory interface</li> <li>■ On-chip termination (OCT)</li> <li>■ 3.3-V support</li> </ul>
Embedded transceiver hard IP	<ul style="list-style-type: none"> <li>■ Custom implementation up to 10.3125 Gbps</li> <li>■ PCI Express® (PCIe®) Gen1 and Gen2</li> <li>■ Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS)</li> <li>■ Common Public Radio Interface (CPRI) PCS</li> <li>■ Gigabit-capable passive optical network (GPON) PCS</li> </ul>

**Table 1–1. Feature Summary for Arria V Devices (Part 2 of 3)**

Feature	Details
HPS (Arria V SX and ST devices only)	<ul style="list-style-type: none"> <li>■ Dual-core ARM Cortex-A9 MPCore processor. Up to 800 MHz maximum frequency that supports symmetric and asymmetric multiprocessing</li> <li>■ Interface peripherals—10/100/1000 Ethernet media access control (MAC), USB 2.0 On-The-Go (OTG) controller, Quad SPI flash controller, NAND flash controller, and SD/MMC/SDIO controller, UART, serial peripheral interface (SPI), I2C interfaces, and up to 86 GPIO interfaces</li> <li>■ System peripherals—general-purpose and watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li> <li>■ On-chip RAM and boot ROM</li> <li>■ HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to master transactions to slaves in the HPS, and vice versa</li> <li>■ FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end of the HPS SDRAM controller</li> <li>■ ARM CoreSight™ JTAG debug, trace port, and on-chip trace storage</li> <li>■ Three fractional PLLs</li> </ul>
Physical medium attachment (PMA) with soft PCS	<ul style="list-style-type: none"> <li>■ 10GBASE-R</li> <li>■ 9.8304-Gbps CPRI</li> </ul>
High-performance core fabric	<ul style="list-style-type: none"> <li>■ Enhanced ALM with four registers</li> <li>■ Improved routing architecture to reduce congestion and improve compilation time</li> </ul>
Variable-precision DSP blocks	<ul style="list-style-type: none"> <li>■ Natively supports three-signal processing precision ranging from 9 x 9, 18 x 19, or 27 x 27 in the same DSP block</li> <li>■ 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li> <li>■ Embedded internal coefficient memory</li> <li>■ Pre-adder/subtractor improves efficiency</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>■ M10K, 10 Kbit with soft error correction code (ECC)</li> <li>■ Memory logic array block (MLAB), 640-bit distributed LUTRAM—you can use up to 25% of the LEs as MLAB memory</li> <li>■ Hardened double data rate3 (DDR3) and DDR2 memory controllers</li> </ul>
High-resolution Fractional PLLs	<ul style="list-style-type: none"> <li>■ Integer mode and fractional mode</li> <li>■ Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li> </ul>
Clock networks	<ul style="list-style-type: none"> <li>■ 625-MHz global clock network</li> <li>■ Global, quadrant, and peripheral clock networks</li> <li>■ Unused clock networks can be powered down to reduce dynamic power</li> </ul>

**Table 1–1. Feature Summary for Arria V Devices (Part 3 of 3)**

Feature	Details
Configuration	<ul style="list-style-type: none"> <li>■ Partial and dynamic reconfigurations</li> <li>■ CvP</li> <li>■ Configuration via HPS</li> <li>■ Serial and parallel flash interface</li> <li>■ Enhanced advanced encryption standard (AES) design security features</li> <li>■ Tamper protection</li> <li>■ Remote system upgrade</li> </ul>
Packaging	<ul style="list-style-type: none"> <li>■ Thermal composite flip chip BGA packaging</li> <li>■ Multiple device densities with identical package footprints for seamless migration between different device densities</li> <li>■ Lead, lead-free (Pb-free), and RoHS-compliant options</li> </ul>

## Arria V Family Plan

Arria V devices offer various thermal composite flip chip BGA packaging options with differing price and performance points. [Table 1–2](#) and [Table 1–3](#) list the Arria V devices features.

**Table 1–2. Maximum Resource Counts for Arria V GX Devices — Preliminary**

Feature	Arria V GX Device							
	5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7
ALMs	28,302	56,100	71,698	91,680	113,208	136,880	158,491	190,240
LE (K)	75	148	190	242	300	362	420	504
M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414
MLAB memory (Kbit)	463	873	1,173	1,448	1,852	2,098	2,532	2,906
Block memory (Kbit)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,139
18 x 19 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,278
Fractional PLLs <sup>(1)</sup>	10	10	12	12	12	12	16	16
GPIO	480	480	544	544	704	704	704	704
LVDS transmitter (TX) <sup>(2)</sup>	68	68	120	120	160	160	156	160
LVDS receiver (RX) <sup>(2)</sup>	80	80	136	136	176	176	172	176
PCIe hard IP blocks	1	1	2	2	2	2	2	2
Hard memory controllers	2	2	4	4	4	4	4	4

**Notes to Table 1–2:**

- (1) The total number of available fractional PLLs is a combination of general-purpose and transceiver PLLs. Transceiver fractional PLLs that are not used by the transceiver I/O can be used as general-purpose fractional PLLs.
- (2) For the LVDS channels count for each package, refer to the [High-Speed Differential I/O Interfaces with DPA in Arria V Devices](#) chapter.

**Table 1-3. Maximum Resource Counts for Arria V GT, SX, and ST Devices—Preliminary**

Feature	Arria V GT Device		Arria V SX Device		Arria V ST Device	
	5AGTD3	5AGTD7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
ALMs	136,880	190,240	132,075	174,340	132,075	174,340
LE (K)	362	504	350	462	350	462
M10K memory blocks	1,726	2,414	1,729	2,282	1,729	2,282
MLAB memory (Kb)	2,098	2,906	2,014	2,658	2,014	2,658
Block memory (Kb)	17,260	24,140	17,288	22,820	17,288	22,820
Variable-precision DSP blocks	1,045	1,156	809	1,068	809	1,068
18 x 19 multipliers	2,090	2,312	1,618	2,186	1,618	2,186
FPGA Fractional PLLs <sup>(1)</sup>	12	16	TBD	TBD	TBD	TBD
HPS PLLs <sup>(1)</sup>	—	—	TBD	TBD	TBD	TBD
FPGA GPIO	704	704	528	528	528	528
HPS I/O	—	—	216	216	216	216
LVDS TX <sup>(2)</sup>	160	160	120	120	120	120
LVDS RX <sup>(2)</sup>	176	176	120	120	120	120
PCIe hard IP blocks	2	2	2	2	2	2
Hard memory controllers	4	4	3	3	3	3
HPS memory controllers	—	—	1	1	1	1
ARM Cortex-A9 MPCore processor	—	—	Dual-core	Dual-core	Dual-core	Dual-core

**Notes to Table 1-3:**

- (1) The total number of available fractional PLLs is a combination of general-purpose and transceiver PLLs. Transceiver fractional PLLs, when not used by the transceiver I/O, can be used as a general-purpose fractional PLL.
- (2) For the LVDS channels count for each package, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria V Devices* chapter.

Table 1-4 lists the Arria V package plan. The package plan shows the GPIO counts, the maximum number of 6-Gbps transceivers available, and the maximum number of 10-Gbps transceivers available per density and package. Various combinations of 6-Gbps and 10-Gbps transceiver counts are available.

**Table 1-4. Package Plan for Arria V Devices — Preliminary<sup>(1)</sup>**

Variants	Devices	F672 (27 mm) Flip Chip		F896 (31 mm) Flip Chip			F1152 (35 mm) Flip Chip			F1517 (40 mm) Flip Chip		
		GPIO	XCVR	GPIO (2)	HPS I/O	XCVR	GPIO	HPS I/O	XCVR	GPIO	HPS I/O	XCVR
Arria V GX (3)	5AGXA1	▲ 336	9	▲ 480	—	12	—	—	—	—	—	—
	5AGXA3	▼ 336	9	▼ 480	—	12	—	—	—	—	—	—
	5AGXA5	▲ 336	9	▲ 384	—	18	▲ 544	—	24	—	—	—
	5AGXA7	▼ 336	9	▲ 384	—	18	▲ 544	—	24	—	—	—
	5AGXB1	—	—	▲ 384	—	18	▲ 544	—	24	▲ 704	—	24
	5AGXB3	—	—	▲ 384	—	18	▲ 544	—	24	▲ 704	—	24
	5AGXB5	—	—	—	—	—	▲ 544	—	24	▲ 704	—	36
Arria V GT (4), (5)	5AGTD3	—	—	▼ 384	—	12, 2	▲ 544	—	12, 4	▲ 704	—	12, 4
	5AGTD7	—	—	—	—	—	▼ 544	—	12, 4	▼ 704	—	12, 8
Arria V SX (3)	5ASXB3	—	—	▲ 178	216	12	▲ 350	216	18	▲ 528	216	30
	5ASXB5	—	—	▼ 178	216	12	▼ 350	216	18	▼ 528	216	30
Arria V ST (4), (5)	5ASTD3	—	—	▲ 178	216	6, 2	▲ 350	216	12, 2	▲ 528	216	12, 6
	5ASTD5	—	—	▼ 178	216	6, 2	▼ 350	216	12, 2	▼ 528	216	12, 6

**Notes to Table 1-4:**

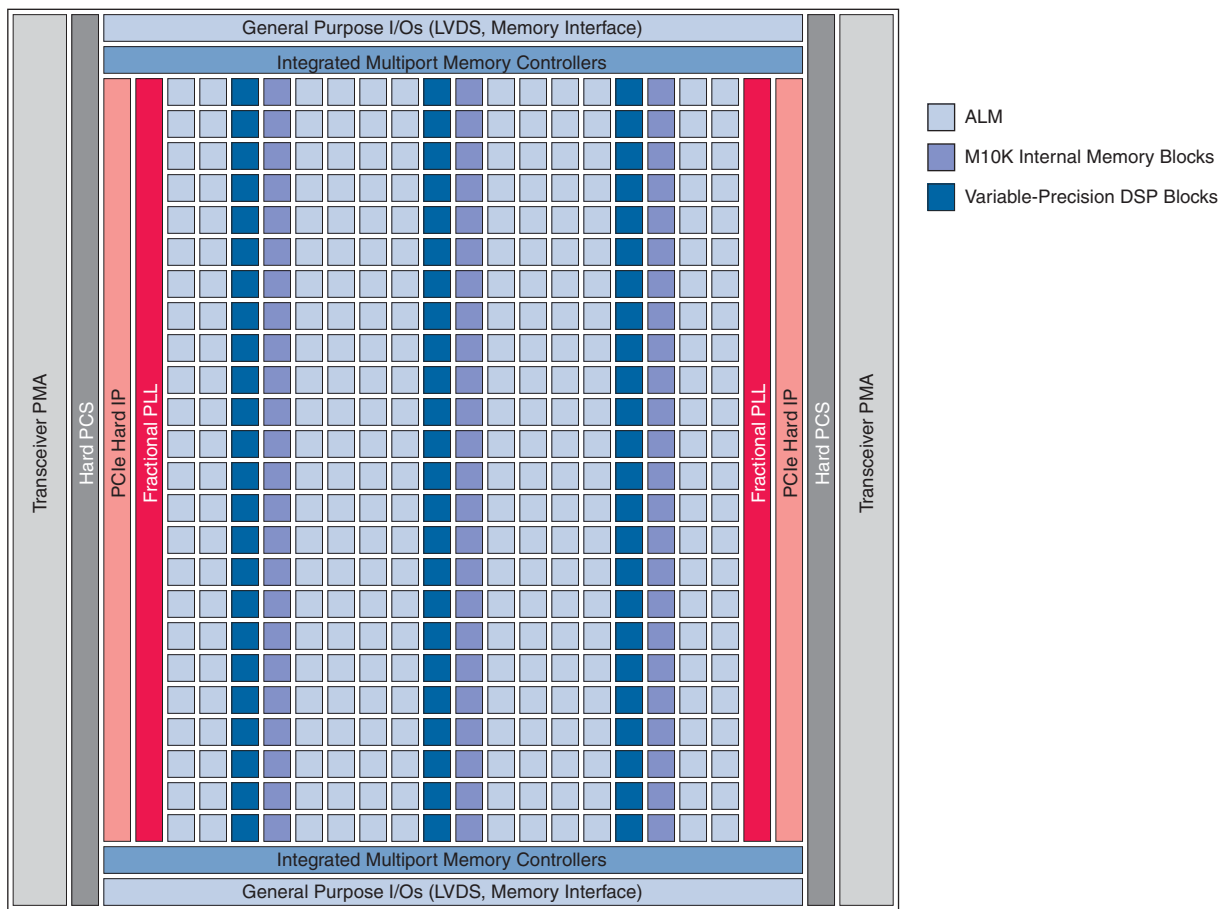
- (1) The arrows indicate the package vertical migration capability. Vertical migration allows you to migrate across device densities for devices having the same dedicated pins, configuration pins, and power pins for a given package.
- (2) In the F896 package, the PCIe hard IP block on the right side of the 5AGXA5, 5AGXA7, 5AGXB1, 5AGXB3, and 5AGTD3 devices supports x1 for Gen1 and Gen2 data rates.
- (3) The transceiver counts listed are for 6-Gbps transceivers.
- (4) The transceiver counts listed are for 6-Gbps and 10-Gbps transceivers, respectively.
- (5) You can alternatively configure any pair of 10-Gbps channels as six 6-Gbps channels. For instance, you can alternatively configure the 5AGTD7 device in the F1517 package as eighteen 6-Gbps and six 10-Gbps, twenty-four 6-Gbps and four 10-Gbps, or thirty 6-Gbps and two 10-Gbps channels.

## Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power 10-Gbps transceivers at less than 140 mW and 6-Gbps transceivers at less than 100 mW power consumption per channel. Arria V transceivers are designed to be standard compliant for a wide range of protocols and data rates.

The transceivers are positioned on the left and right outer edges of the device, as shown in Figure 1-1.

Figure 1-1. Device Chip Overview for Arria V Devices (1), (2)



**Notes to Figure 1-1:**

- (1) This figure represents an Arria V device with transceivers. Other Arria V devices may have a different floor plan than the one shown here.
- (2) This figure is a graphical representation of a top view of the silicon die, which corresponds to a reverse view for flip chip packages.

## PMA Support

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip, ensuring optimal signal integrity. The transceiver channels consist of the PMA, PCS, and clock networks. You can also use the unused receiver PMA channels as additional transmit PLLs.

Table 1-5 lists the transceiver PMA features.

**Table 1-5. Transceiver PMA Features for Arria V Devices**

Features	Capability
Backplane support	Up to 16" FR4 PCB fabric drive capability at up to 6.5536 Gbps
Chip-to-chip support	Up to 10.3125 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	Up to 6 dB of pre-emphasis and 4 dB of equalization
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows reconfiguration of single channels without affecting operation of other channels

## PCS Support

The Arria V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, or 40-bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1 and Gen2, XAUI, GbE, Serial RapidIO® (SRIO), and CPRI protocols. All other standard and proprietary protocols from 611 Mbps to 6.5536 Gbps are supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) transceiver PCS hard IP. A dedicated 80-bit interface to the core logic connects directly from the PMA, bypassing the PCS hard IP, to support all protocols beyond 6.5536 Gbps up to 10.3125 Gbps.

Table 1-6 lists the transceiver PCS features.

**Table 1-6. Transceiver PCS Features for Arria V Devices (Part 1 of 2)**

PCS Support <sup>(1)</sup>	Data Rates (Gbps)	Transmitter Data Path	Receiver Data Path
Custom single- and double-width modes	0.61 to ~6.5536	Phase compensation FIFO, byte serializer, and 8B/10B encoder	Word aligner, 8B/10B decoder, byte deserializer, and phase compensation FIFO
PCIe Gen1: x1, x2, x4, x8 PCIe Gen2: x1, x2, x4 <sup>(2)</sup>	2.5 and 5.0	The same as custom single- and double-width modes, plus PIPE 2.0 interface to the core logic	The same as custom single- and double-width modes, plus rate match FIFO and PIPE 2.0 interface to the core logic
GbE	1.25	The same as custom single- and double-width modes	The same as custom single- and double-width modes, plus rate match FIFO

**Table 1-6. Transceiver PCS Features for Arria V Devices (Part 2 of 2)**

PCS Support <sup>(1)</sup>	Data Rates (Gbps)	Transmitter Data Path	Receiver Data Path
XAUI	3.125	The same as custom single- and double-width modes, plus the XAUI state machine for bonding four channels	The same as custom single- and double-width modes, plus the XAUI state machine for realigning four channels, and deskew FIFO circuitry
SRIO	1.25 to 6.25	The same as custom single- and double-width modes	The same as custom single- and double-width modes
SDI	0.27 <sup>(3)</sup> , 1.485, 2.97	Phase compensation FIFO, byte serializer	Byte deserializer and phase compensation FIFO
Serial ATA	1.5, 3.0, 6.0	Phase compensation FIFO, byte serializer, 8B/10B encoder	Phase compensation FIFO, byte deserializer, word aligner, and 8B/10B decoder
CPRI <sup>(4)</sup>	0.6144 to 6.144	The same as custom single- and double-width modes, plus the TX deterministic latency	The same as custom single- and double-width modes, plus the RX deterministic latency
GPON <sup>(5)</sup>	1.25 and 2.5	Phase compensation FIFO and byte serializer	Phase compensation FIFO and byte deserializer

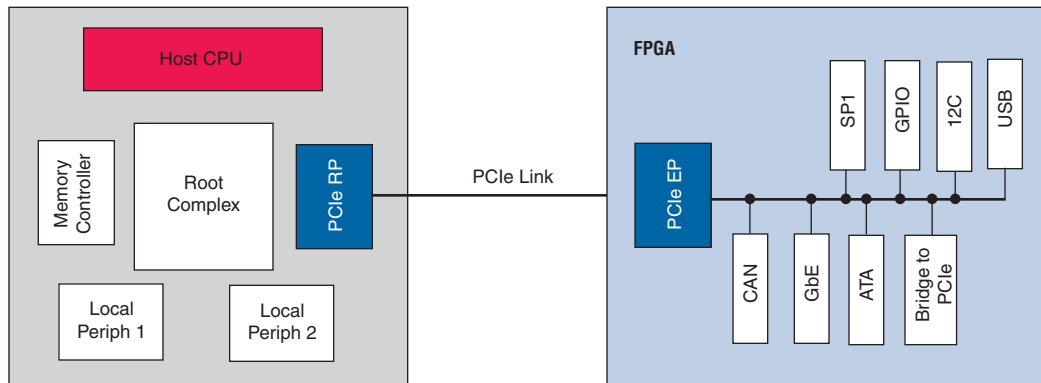
**Notes to Table 1-6:**

- (1) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through soft PCS.
- (2) PCIe Gen2 is supported with the PCIe hard IP only.
- (3) The 0.27-Gbps data rate is supported using oversampling user logics that you must implement in the FPGA fabric.
- (4) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through soft PCS.
- (5) The GPON standard does not support burst mode.

## PCIe Gen1 and Gen2 Hard IP

Arria V devices contain PCIe hard IP designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the PHY MAC, data link, and transaction layers. The PCIe hard IP supports PCIe Gen2 end point and root port for up to x4 lane configurations, and PCIe Gen1 end point and root port for up to x8 lane configurations. PCIe endpoint support includes multifunction support for up to eight functions, as shown in [Figure 1-2](#).

**Figure 1-2. PCIe Multifunction for Arria V Devices**



The Arria V PCIe hard IP operates independently from the core logic, which allows the PCIe link to wake up and complete link training in less than 100 ms, while the Arria V device completes loading the programming file for the rest of the device. In addition, the Arria V PCIe hard IP has improved end-to-end data path protection using ECC.

## FPGA GPIOs

Arria V devices offer highly configurable GPIOs. The following list describes the many features of the GPIOs:

- Programmable bus hold and weak pull-up.
- LVDS output buffer with programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis.
- Dynamic on-chip parallel termination ( $R_T$  OCT) for all I/O banks with OCT calibration to limit the termination impedance variation.
- On-chip dynamic termination to swap between serial and parallel termination, depending on whether there is reading or writing on a common bus for signal integrity.
- Configurable unused voltage reference ( $V_{REF}$ ) pins as user I/Os.
- Easy timing closure support using the hardened read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture.

## External Memory

Arria V devices support up to four hardened memory controllers for DDR3 and DDR2 SDRAM. Each controller supports 8- to 32-bit components up to 4 gigabits (Gb) in density with two-chip select and optional ECC. Arria V devices do not support DDR3 SDRAM leveling.

Arria V devices also support soft memory controllers for DDR3, DDR2, LPDDR2, and LPDDR SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM for maximum flexibility.

Table 1-7 lists the external memory interface block performance.

**Table 1-7. External Memory Interface Performance for Arria V Devices**

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDR3 SDRAM	1.5	533	667
	1.35	533	667
	1.25	400	400
DDR2 SDRAM	1.8	400	400
	1.5	400	400
RLDRAM II	1.8	(1)	400
QDR II+ SRAM	1.8	(1)	400
	1.5	(1)	400
QDR II SRAM	1.8	(1)	400
	1.5	(1)	400
DDR II+ SRAM (2)	1.8	(1)	400
	1.5	(1)	400
LPDDR SDRAM (2)	1.8	(1)	200
LPDDR2 SDRAM (2)	1.2	(1)	400

**Notes to Table 1-7:**

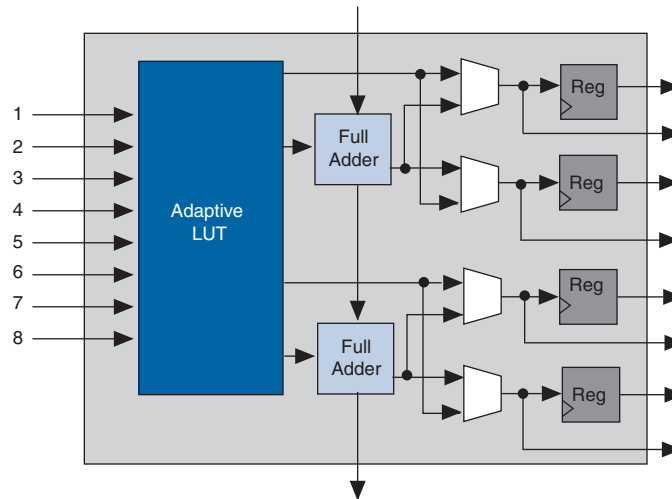
- (1) These memory interfaces are not supported in the hard memory controller.
- (2) These memory interfaces are not available as Altera® IP.

## ALM

Arria V devices use a 28-nm ALM as the basic building block of the device fabric. The ALM shown in Figure 1-3 uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

You can configure up to 25% of the ALMs in Arria V devices as distributed MLABs. For more information, refer to “Embedded Memory” on page 1-14.

**Figure 1-3. ALM for Arria V Devices**



## Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that you can configure to support signal processing with precision ranging from 9 x 9, 18 x 19, and 27 x 27 bits natively.

You can independently configure each DSP block during compilation as a triple 9 x 9, a dual 18 x 19 multiply, or a single 27 x 27. With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

The variable precision DSP block also supports these features:

- 64-bit accumulator that is the largest in the industry,
- Double accumulator
- Hard pre-adder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic FIR filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single floating point arithmetic
- Inferability of all modes by the Altera Complete Design Suite

Table 1-8 lists the accommodation of different configurations in a DSP block.

**Table 1-8. Variable-Precision DSP Block Configurations for Arria V Devices**

Multiplier Size (Bit)	DSP Block Resources	Expected Usage
Three 9 x 9	1 variable-precision DSP block	Low precision fixed point for video applications
Two 18 x 19	1 of variable-precision DSP block	Medium precision fixed point in FIR filters
Two 18 x 19 with accumulate	1 variable-precision DSP block	FIR filters
One 27 x 27	1 variable-precision DSP block	Single precision floating point

Table 1-9 lists the number of multipliers in Arria V devices.

**Table 1-9. Number of Multipliers in Arria V Devices**

Variants	Devices	Variable Precision DSP Blocks	Independent Input and Output Multiplications Operator			18 x 19 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36-bit Input
			9 x 9 Multipliers	18 x 19 Multipliers	27 x 27 Multipliers		
Arria V GX	5AGXA1	240	720	480	240	240	240
	5AGXA3	396	1,188	792	396	396	396
	5AGXA5	600	1,800	1,200	600	600	600
	5AGXA7	800	2,400	1,600	800	800	800
	5AGXB1	920	2,760	1,840	920	920	920
	5AGXB3	1,045	3,135	2,090	1,045	1,045	1,045
	5AGXB5	1,092	3,276	2,184	1,092	1,092	1,092
Arria V GT	5AGXB7	1,139	3,417	2,278	1,139	1,139	1,139
	5AGTD3	1,045	3,135	2,090	1,045	1,045	1,045
Arria V SX	5AGTD7	1,139	3,417	2,278	1,139	1,139	1,139
	5ASXB3	809	2,427	1,618	809	809	809
Arria V ST	5ASXB5	1,068	3,204	2,136	1,068	1,068	1,068
	5ASTD3	809	2,427	1,618	809	809	809
	5ASTD5	1,068	3,204	2,136	1,068	1,068	1,068

## Embedded Memory

The Arria V memory blocks are flexible and designed to provide an optimal amount of small- and large-sized memory arrays. Arria V devices contain two types of embedded memory blocks:

- 640-bit MLAB blocks—for wide and shallow memories. You can use up to 25% of the device LABs as MLAB. The MLAB operates at up to 500 MHz.
- 10-Kb M10K blocks—for larger memory configurations. The M10K embedded memory operates at up to 400 MHz.

Table 1–10 lists the supported memory configurations for Arria V devices.

**Table 1–10. Embedded Memory Block Configuration for Arria V Devices**

Memory Block	Depth (bits)	Programmable Widths
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

## Dynamic and Partial Reconfiguration

Dynamic reconfiguration enables transceiver data rates or encoding schemes to be changed dynamically while maintaining data transfer on adjacent transceiver channels in Arria V devices. Dynamic reconfiguration is ideal for applications requiring on-the-fly multi-protocol or multi-rate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Partial reconfiguration allows you to reconfigure part of the device while other sections remain running. Partial reconfiguration is required in systems where the uptime is critical because it allows you to make updates or adjust functionality without disrupting other services. While lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place the device functions that do not operate simultaneously. Instead, you can store these functions in external memory and load them as required. This reduces the size of the required device by allowing multiple applications on a single device, which saves board space and reduces power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building the partial reconfiguration capability on top of the proven incremental compile and design flow in the Quartus® II software. With this Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable partial reconfiguration of both the core and transceiver simultaneously.

## Clock Networks and PLL Clock Sources

The Arria V clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dedicated clock input pins and fractional PLLs. Arria V devices have 16 global clock networks capable of up to 625 MHz operation. The Quartus II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Arria V devices have up to 16 PLLs with 18 output counters per PLL. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use fractional PLLs to reduce the number of oscillators required on your board, as well as reduce the clock pins used in the device by synthesizing multiple clock frequencies from a single reference clock source. You can use the PLLs for frequency synthesis, on-chip clock deskew, jitter attenuation, dynamic phase-shift, zero delay buffers, counters reconfiguration, bandwidth reconfiguration, programmable output clock duty cycles, PLL cascading, and reference clock switchover.

Arria V devices use a fractional PLL architecture in addition to the historical integer PLL. When you use fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for an off-chip reference clock. Transceiver fractional PLLs, when not used by the Transceiver I/O, can be used as general-purpose fractional PLLs by the FPGA fabric.

## Enhanced Configuration and Configuration via Protocol

Arria V devices support 3.3-V programming voltage and the following configuration modes:

- active serial (AS)
- passive serial (PS)
- fast passive parallel (FPP)
- CvP
- Configuration via HPS
- configuration through JTAG

You can configure Arria V devices through PCIe using CvP instead of an external flash or ROM. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100-ms power-up-to-active time requirement.

 For more information regarding CvP, refer to the [Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#).

Table 1-11 lists the configuration modes that Arria V devices support.

**Table 1-11. Configuration Modes and Features for Arria V Devices**

Mode	Data Width (Bit)	Maximum Clock Rate (MHz)	Maximum Data Rate (Mbps)	Decompression	Design Security	Remote System Update	Partial Reconfiguration
AS	1, 4	100	—	✓	✓	✓	—
PS	1	125	125	✓	✓	—	—
FPP	8, 16	125	—	✓	✓	Parallel flash loader	16-bit only
CvP	x1, x2, x4, x8 <sup>(1)</sup>	—	—	✓	✓	✓	✓
HPS	32	125	—	✓	✓	Parallel flash loader	✓
JTAG	1	33	33	—	—	—	—

**Note to Table 1-11:**

(1) Number of lanes instead of bits.

## Power Management

Arria V devices leverage FPGA architectural features and process technology advancements to reduce the total device core power consumption by as much as 50% when compared with Stratix IV devices at the same performance level.

Additionally, Arria V devices have a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings when compared with soft implementations. The list includes PCIe Gen1 and Gen2, XAUI, GbE, SRIO, GPON and CPRI protocols. The hard IP blocks consume up to 25% less power than equivalent soft implementations.

Arria V transceivers are also designed for power efficiency. As a result, the transceiver channels consume 50% less power than the previous generation of Arria devices.

## SoC FPGA with HPS

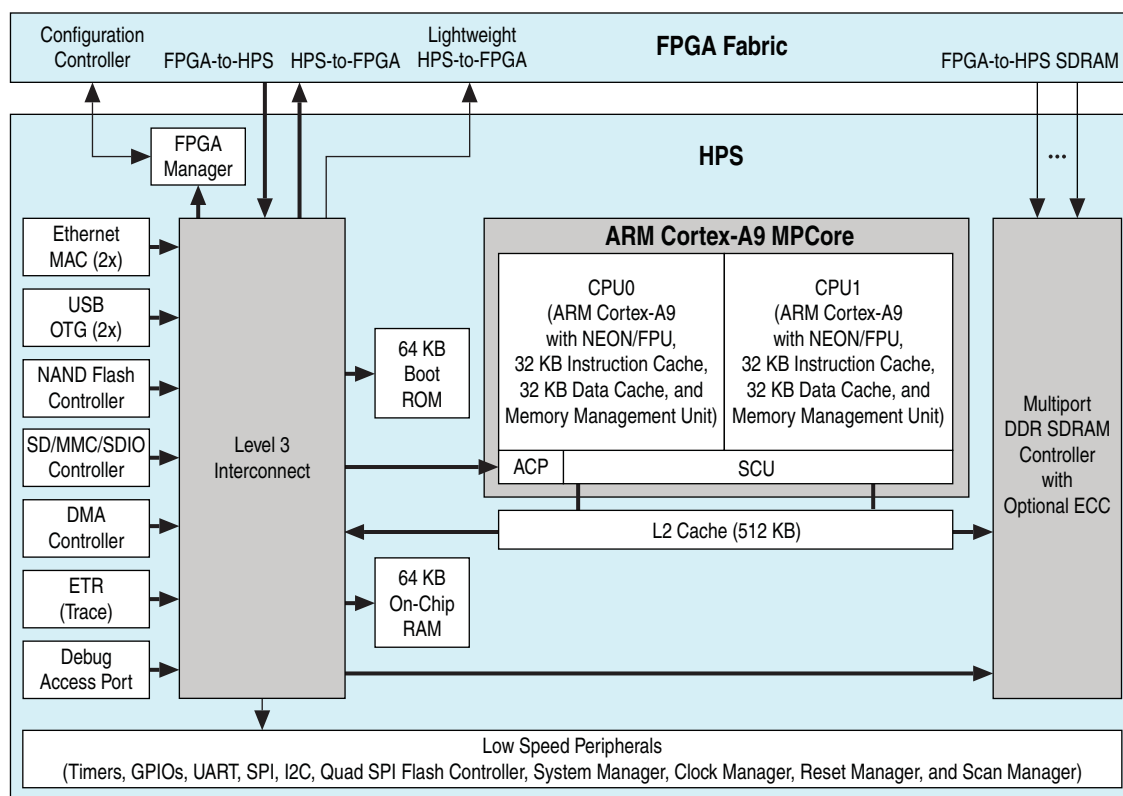
Each SoC FPGA device combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in the following ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both the hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## Features of the HPS

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in Figure 1-4..

Figure 1-4. HPS with Dual-Core ARM Cortex-A9 MPCore Processor



## System Peripherals

The Ethernet MAC, USB OTG controller, NAND flash controller and SD/MMC/SDIO controller modules have an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels for high-bandwidth data transfers. The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA<sup>®</sup>) Advanced eXtensible Interface (AXI<sup>™</sup>) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the FPGA fabric to master transactions to the slaves in the HPS
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the HPS to master transactions to the slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower performance 32-bit width bus that allows the HPS to master transactions to the slaves in the FPGA fabric.

The HPS-FPGA AXI bridges also allow the FPGA fabric to access the memory shared by one or both microprocessors, and provide asynchronous clock crossing with the clock from the FPGA fabric.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that is shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon<sup>®</sup> Memory-Mapped (Avalon-MM) interface standards, and provides up to four ports with separate read and write directions.

To maximize memory performance, the HPS SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The HPS SDRAM controller subsystem supports DDR2, DDR3, LPDDR, or LPDDR2 devices up to 4 Gb and runs up to 533 MHz (1066 Mbps data rate).

For easy migration, the FPGA-to-HPS SDRAM interface is compatible with the interface of the soft SDRAM memory controller IPs and hard SDRAM memory controllers in the FPGA fabric.

## FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC FPGA are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS before you power up and configure the FPGA fabric. After the system is running, the HPS reconfigures the FPGA fabric at any time under program control or through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then upload the boot code to the HPS from the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus II software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoC FPGAs follows the same steps as those for other SoC devices. Altera also provides support for the Linux and VxWorks® operating systems.

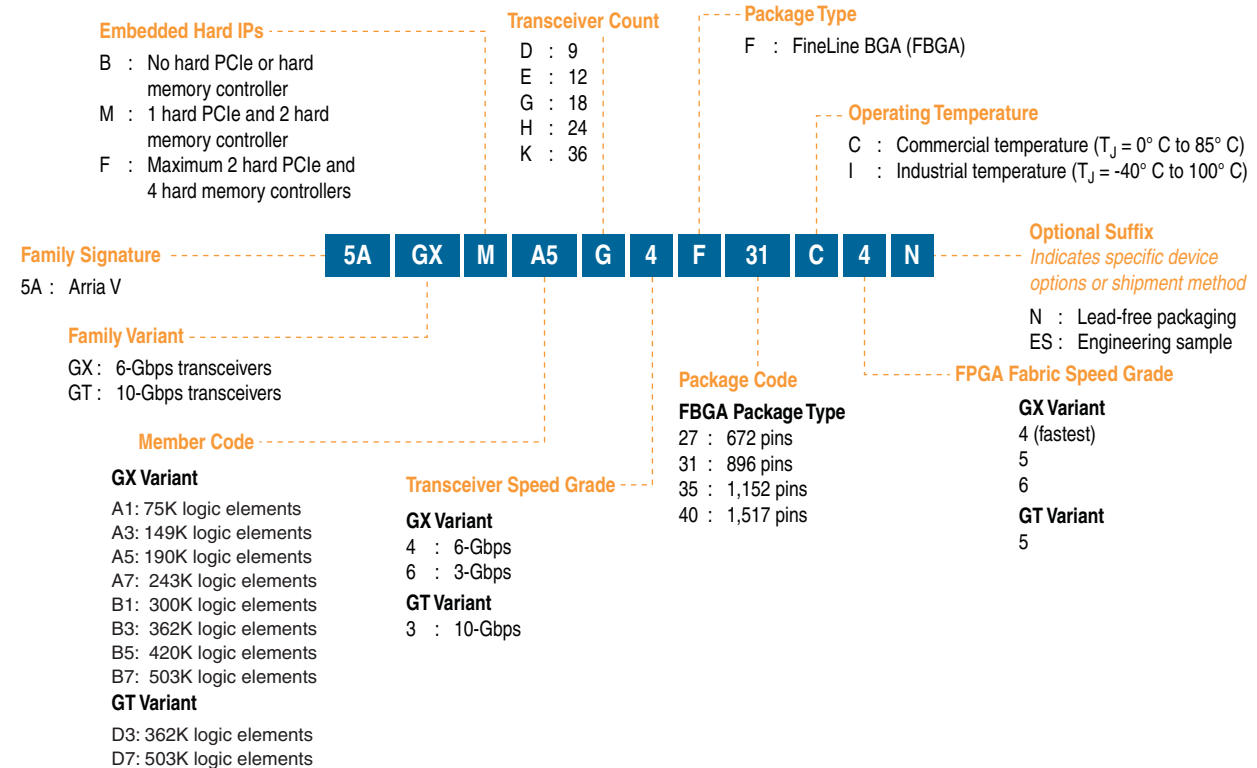
You can begin device-specific firmware and software development on the Altera SoC FPGA Virtual Target. The Virtual Target is a PC-based fast-functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Ordering Information

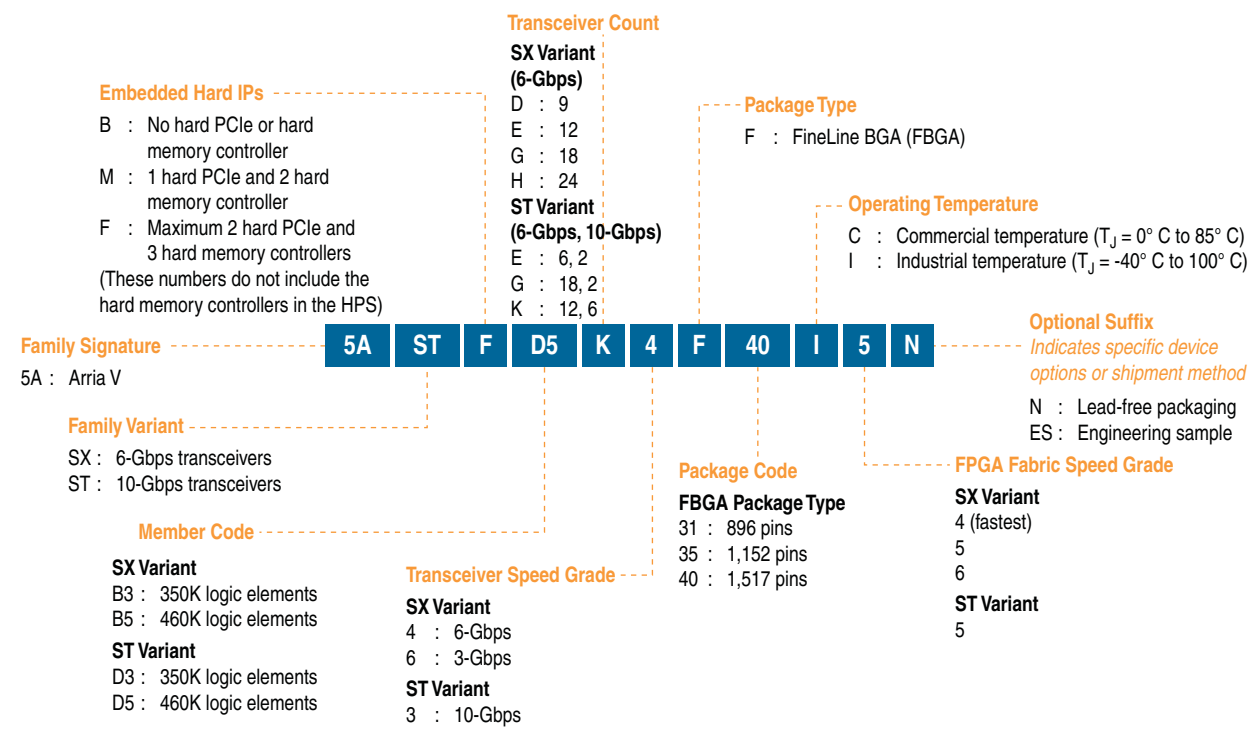
This section describes the ordering information for Arria V devices.

Figure 1-5 and Figure 1-6 show the ordering codes for Arria V devices.

**Figure 1-5. Ordering Information for Arria V GX and GT Devices**



**Figure 1-6. Ordering Information for Arria V SX and ST Devices**



## Document Revision History

Table 1-12 lists the revision history for this chapter.

**Table 1-12. Document Revision History**

Date	Version	Changes
February 2012	1.3	<ul style="list-style-type: none"> <li>Updated Table 1-2 and Table 1-3.</li> <li>Updated Figure 1-5 and Figure 1-6.</li> <li>Minor text edits.</li> </ul>
December 2011	1.2	<ul style="list-style-type: none"> <li>Minor text edits.</li> </ul>
November 2011	1.1	<ul style="list-style-type: none"> <li>Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-6, Table 1-7, Table 1-9, and Table 1-10.</li> <li>Added “SoC FPGA with HPS” section.</li> <li>Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections.</li> <li>Updated Figure 1-5.</li> <li>Added Figure 1-6.</li> <li>Minor text edits.</li> </ul>
August 2011	1.0	Initial release.

