8. Selectable I/O Standards in Arria GX Devices

AGX52008-1.2

Introduction

This chapter provides guidelines for using industry I/O standards in Arria™ GX devices, including:

- I/O features
- I/O standards
- External memory interfaces
- I/O banks
- Design considerations

This chapter contains the following sections:

Arria GX I/O Features

Arria GX devices contain an abundance of adaptive logic modules (ALMs), embedded memory, high-bandwidth digital signal processing (DSP) blocks, and extensive routing resources, all of which can operate at very high core speed.

The Arria GX device's I/O structure is designed to ensure that these internal capabilities are fully utilized. There are numerous I/O features to assist in high-speed data transfer into and out of the device including:

- Single-ended, non-voltage-referenced and voltage-referenced I/O standards
- High-speed differential I/O standards featuring serializer/deserializer (SERDES), dynamic phase alignment (DPA), capable of 840 megabit per second (Mbps) performance for low-voltage differential signaling (LVDS), Hypertransport technology, high-speed transceiver logic (HSTL), stub-series terminated logic (SSTL), and LVPECL

HSTL, SSTL, and LVPECL I/O standards are used only for PLL clock inputs and outputs in differential mode.

- Double data rate (DDR) I/O pins
- Programmable output drive strength for voltage-referenced and non-voltage-referenced single-ended I/O standards
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination
- On-chip differential termination
- Peripheral component interconnect (PCI) clamping diode
- Hot socketing

For a detailed description of each I/O feature, refer to the *Arria GX Architecture* chapter in volume 1 of the *Arria GX Device Handbook*.

Arria GX I/O Standards Support

Arria GX devices support a wide range of industry I/O standards. Table 8–1 shows which I/O standards Arria GX devices support as well as typical applications.

Table 8–1. Arria GX I/O Standard Applications (Part 1 of 2)

I/O Standard	Application
LVTTL	General purpose
LVCMOS	General purpose
2.5 V	General purpose
1.8 V	General purpose
1.5 V	General purpose
3.3-V PCI	PC and embedded system
3.3-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
1.8-V HSTL Class I	SRAM interfaces
1.8-V HSTL Class II	SRAM interfaces
1.5-V HSTL Class I	SRAM interfaces
1.5-V HSTL Class II	SRAM interfaces
1.2-V HSTL	General purpose
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM

Table 8–1. Arria GX I/O Standard Applications (Part 2 of 2)

I/O Standard	Application
Differential SSTL-18 Class II	DDR2 SDRAM
1.8-V differential HSTL Class I	Clock interfaces
1.8-V differential HSTL Class II	Clock interfaces
1.5-V differential HSTL Class I	Clock interfaces
1.5-V differential HSTL Class II	Clock interfaces
LVDS	High-speed communications
HyperTransport technology	PCB interfaces
Differential LVPECL	Video graphics and clock distribution

Single-Ended I/O Standards

In non-voltage-referenced single-ended I/O standards, the voltage at the input must be above a set voltage to be considered "on" (high, or logic value 1) or below another voltage to be considered "off" (low, or logic value 0). Voltages between the limits are undefined logically, and may fall into either a logic value 0 or 1. The non-voltage-referenced single-ended I/O standards supported by Arria GX devices are:

- Low-voltage transistor-transistor logic (LVTTL)
- Low-voltage complementary metal-oxide semiconductor (LVCMOS)
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X

Voltage-referenced, single-ended I/O standards provide faster data rates. These standards use a constant reference voltage at the input levels. The incoming signals are compared with this constant voltage and the difference between the two defines "on" and "off" states.

☞ Arria GX devices support SSTL and HSTL voltage-referenced I/O standards.

LVTTL

The LVTTL standard is formulated under the EIA/JEDEC Standard, JESD8-B (Revision of JESD8-A): Interface Standard for Nominal 3-V/3.3-V Supply Digital Integrated Circuits.

The standard defines DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVTTL-compatible devices. The 3.3-V LVTTL standard is a general-purpose, single-ended standard used for 3.3-V applications. This I/O standard does not require input reference voltages (V_{REF}) or termination voltages (V_{TT}).

☞ Arria GX devices support both input and output levels for 3.3-V LVTTL operation.

Arria GX devices support a V_{CCIO} voltage level of 3.3 V ±5% as specified as the narrow range for the voltage supply by the EIA/JEDEC standard.

LVCMOS

The LVCMOS standard is formulated under the EIA/JEDEC Standard, JESD8-B (Revision of JESD8-A): Interface Standard for Nominal 3-V/3.3-V Supply Digital Integrated Circuits.

The standard defines DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices. The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. While LVCMOS has its own output specification, it specifies the same input voltage requirements as LVTTL. These I/O standards do not require V_{REF} or V_{TT}.

☞ Arria GX devices support both input and output levels for 3.3-V LVCMOS operation.

Arria GX devices support a V_{CCIO} voltage level of 3.3 V ±5% as specified as the narrow range for the voltage supply by the EIA/JEDEC standard.

1.5 V

The 1.5-V I/O standard is formulated under the EIA/JEDEC Standard, JESD8-11: 1.5-V ±0.1-V (Normal Range) and 0.9-V – 1.6-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. This standard is a general-purpose, single-ended standard used for 1.5-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Arria GX devices support both input and output levels for 1.5-V operation V_{CCIO} voltage level support of 1.8 V ±5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

1.8 V

The 1.8-V I/O standard is formulated under the EIA/JEDEC Standard, EIA/JESD8-7: 1.8-V ±0.15-V (Normal Range), and 1.2-V – 1.95-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. This standard is a general-purpose, single-ended standard used for 1.8-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Arria GX devices support both input and output levels for 1.8-V operation with V_{CCIO} voltage level support of 1.8 V ±5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

2.5 V

The 2.5-V I/O standard is formulated under the EIA/JEDEC Standard, EIA/JESD8-5: 2.5-V ± 0.2-V (Normal Range), and 1.8-V – 2.7-V (Wide Range) Power Supply Voltage and Interface Standard for Non-Terminated Digital Integrated Circuit.

The standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. This standard is a general-purpose, single-ended standard used for 2.5-V applications. It does not require the use of a V_{REF} or a V_{TT}.

Arria GX devices support both input and output levels for 2.5-V operation with V_{CCIO} voltage level support of 2.5 V ±5%, which is narrower than defined in the Normal Range of the EIA/JEDEC standard.

3.3-V PCI

The 3.3-V PCI I/O standard is formulated under the PCI Local Bus Specification Revision 2.2 developed by the PCI Special Interest Group (SIG).

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 2.2 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires 3.3-V $V_{CCIO.}$ Arria GX devices are fully compliant with the 3.3-V PCI Local Bus Specification Revision 2.2 and meet 64-bit/33-MHz operating frequency and timing requirements.

☞ The 3.3-V PCI standard does not require input reference voltages or board terminations. Arria GX devices support both input and output levels.

3.3-V PCI-X

The 3.3-V PCI-X I/O standard is formulated under the PCI-X Local Bus Specification Revision 1.0a developed by the PCI SIG.

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 Gbps for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, you can design devices to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V V_{CCIO}. Arria GX devices are fully compliant with the 3.3-V PCI-X Specification Revision 1.0a and meet the 133-MHz operating frequency and timing requirements. The 3.3-V PCI-X standard does not require input reference voltages or board terminations.

☞ Arria GX devices support both input and output levels operation.

SSTL-2 Class I & SSTL-2 Class II

The 2.5-V SSTL-2 standard is formulated under the JEDEC Standard, JESD8-A: Stub Series Terminated Logic for 2.5-V (SSTL_2).

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed DDR SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operation in conditions where a bus must be isolated from large stubs. SSTL-2 requires a 1.25-V V_{REF} and a 1.25-V V_{TT} to which the series and termination resistors are connected (Figures 8–1 and 8–2).

☞ Arria GX devices support both input and output levels operation.

Figure 8–1. 2.5-V SSTL Class I Termination

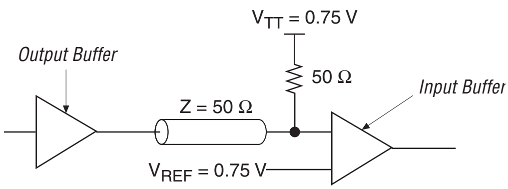
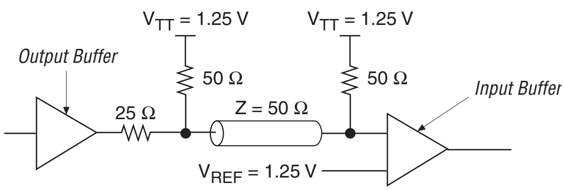


Figure 8–2. 2.5-V SSTL Class II Termination



SSTL-18 Class I & SSTL-18 Class II

The 1.8-V SSTL-18 standard is formulated under the JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8-V (SSTL_18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT} to which the series and termination resistors are connected.

There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera® provides solutions to two derived applications in the JEDEC specification, and names them Class I and Class II to be consistent with other SSTL standards. Figures 8–3 and 8–4 show SSTL-18 Class I and II termination, respectively.

☞ Arria GX devices support both input and output levels operation.

Figure 8–3. Figure9–3.1.8-V SSTL Class I Termination

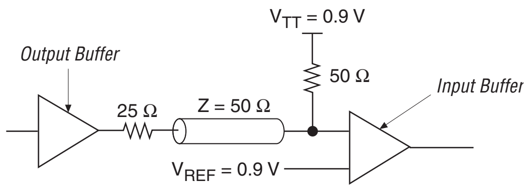
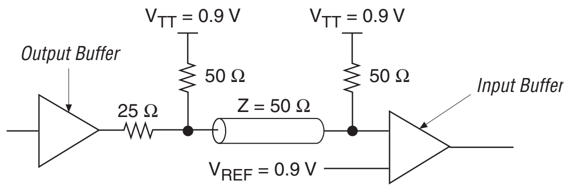


Figure 8–4. Figure9–4.1.8-V SSTL Class II Termination



1.8-V HSTL Class I & 1.8-V HSTL Class II

The HSTL standard is a technology-independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range.

Although JEDEC specifies a maximum V_{CCIO} value of 1.6 V, there are various memory chip vendors with HSTL standards that require a V_{CCIO} of 1.8 V. Arria GX devices support interfaces to chips with V_{CCIO} of 1.8 V for HSTL. Figures 8–5 and 8–6 show the nominal V_{REF} and V_{TT} required to track the higher value of V_{CCIO}. The value of V_{REF} is selected to provide optimum noise margin in the system.

Arria GX devices support both input and output levels operation.

Figure 8–5. 1.8-V HSTL Class I Termination

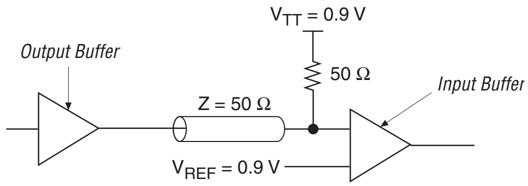
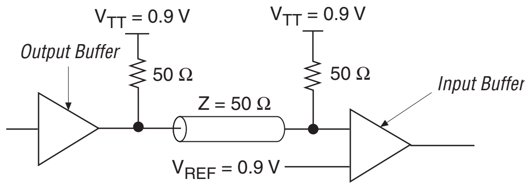


Figure 8–6. 1.8-V HSTL Class II Termination



1.5-V HSTL Class I & 1.5-V HSTL Class II

The 1.5-V HSTL standard is formulated under the EIA/JEDEC Standard, EIA/JESD8-6: A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Arria GX devices are compatible with the 1.8-V HSTL I/O standard in APEX 20KE, APEX20KC, and in Arria GX devices themselves because the input and output voltage thresholds are compatible (Figures 8–7 and 8–8).

Arria GX devices support both input and output levels with V_{REF} and V_{TT}.

Figure 8–7. 1.5-V HSTL Class I Termination

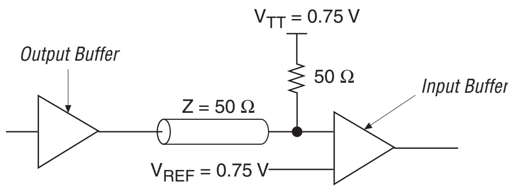
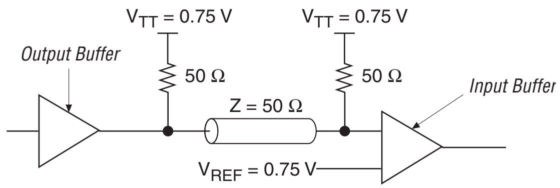


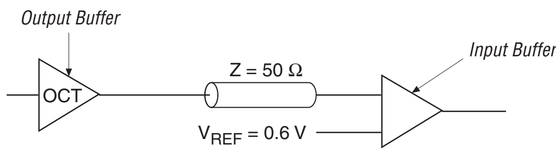
Figure 8–8. 1.5-V HSTL Class II Termination



1.2-V HSTL

Although there is no EIA/JEDEC standard available for the 1.2-V HSTL standard, Altera supports it for applications that operate in the 0.0 to 1.2-V HSTL logic nominal switching range. 1.2-V HSTL can be terminated through series on-chip termination (OCT). Figure 8–9 shows the termination scheme.

Figure 8–9. 1.2-V HSTL Termination



Differential I/O Standards

Differential I/O standards are used to achieve even faster data rates with higher noise immunity. Apart from LVDS, LVPECL, and HyperTransport technology, Arria GX devices also support differential versions of SSTL and HSTL standards.

For detailed information about differential I/O standards, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook.*

Differential SSTL-2 Class I & Differential SSTL-2 Class II

The 2.5-V differential SSTL-2 standard is formulated under the JEDEC Standard, JESD8-9A: Stub Series Terminated Logic for 2.5-V (SSTL_2).

This I/O standard is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. Arria GX devices support both input and output levels. Figures 8–10 and 8–11 show details about differential SSTL-2 termination.

Arria GX devices support differential SSTL-2 I/O standards in pseudo-differential mode, which is implemented by using two SSTL-2 single-ended buffers.

The Quartus® II software only supports pseudo-differential standards on the `INCLK`, `FBIN`, and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support pseudo-differential SSTL-2 I/O standards on the left I/O banks, you can implement these standards on these banks. You need to create two pins in the designs and configure the pins with single-ended SSTL-2 standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended SSTL-2 standards support at these banks.

Figure 8–10. Differential SSTL-2 Class I Termination

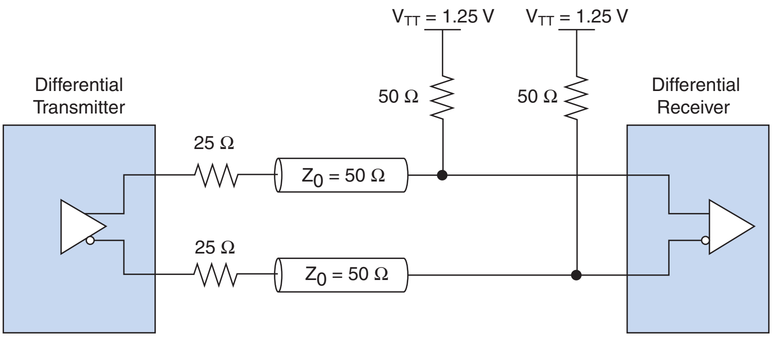
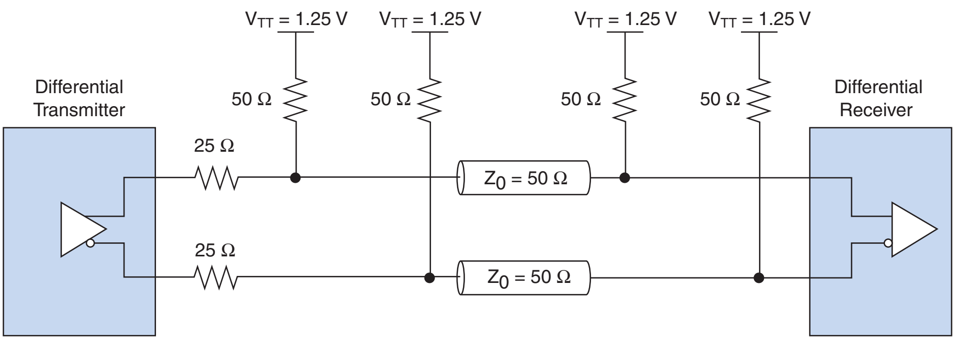


Figure 8–11. Differential SSTL-2 Class II Termination



Differential SSTL-18 Class I & Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under the JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8-V (SSTL_18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks.

Arria GX devices support both input and output levels operation.

Figures 8–12 and 8–13 show details about differential SSTL-18 termination. Arria GX devices support differential SSTL-18 I/O standards in pseudo-differential mode, which is implemented by using two SSTL-18 single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the `INCLK`, `FBIN`, and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support pseudo-differential SSTL-18 I/O standards on the left and I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended SSTL-18 standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended SSTL-18 standards support at these banks.

Figure 8–12. Differential SSTL-18 Class I Termination

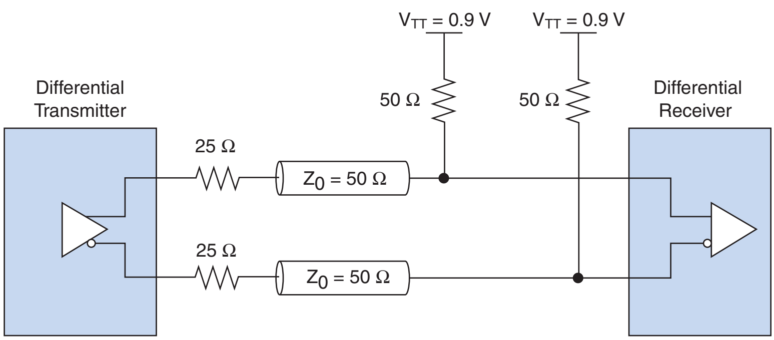
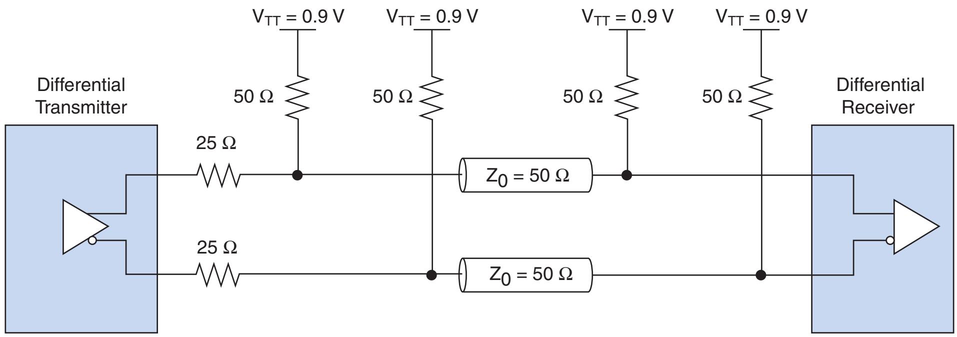


Figure 8–13. Differential SSTL-18 Class II Termination



1.8-V Differential HSTL Class I & 1.8-V Differential HSTL Class II

The 1.8-V differential HSTL specification is the same as the 1.8-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as QDR memory clock interfaces. Arria GX devices support both input and output levels operation. Figures 8–14 and 8–15 show details about 1.8-V differential HSTL termination.

Arria GX devices support 1.8-V differential HSTL I/O standards in pseudo-differential mode, which is implemented by using two 1.8-V HSTL single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the `INCLK`, `FBIN`, and `EXTCLK` ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support 1.8-V pseudo-differential HSTL I/O standards on left I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended 1.8-V HSTL standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended 1.8-V HSTL standards support at these banks.

Figure 8–14. 1.8-V Differential HSTL Class I Termination

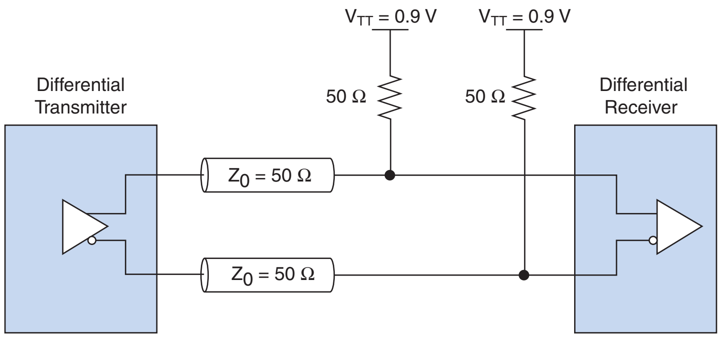
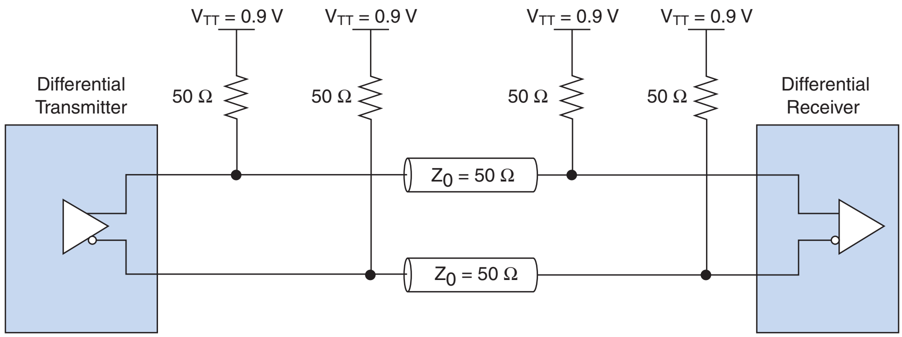


Figure 8–15. 1.8-V Differential HSTL Class II Termination



1.5-V Differential HSTL Class I & 1.5-V Differential HSTL Class II

The 1.5-V differential HSTL standard is formulated under the EIA/JEDEC Standard, EIA/JESD8-6: A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Arria GX devices support both input and output levels operation. Figures 8–16 and 8–17 show details on the 1.5-V differential HSTL termination.

Arria GX devices support 1.5-V differential HSTL I/O standards in pseudo-differential mode, which is implemented by using two 1.5-V HSTL single-ended buffers.

The Quartus II software only supports pseudo-differential standards on the INCLK, FBIN, and EXTCLK ports of enhanced PLL, as well as on DQS pins when DQS megafunction (ALTDQS, Bidirectional Data Strobe) is used. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a pseudo-differential output. A proper V_{REF} voltage is required for the two single-ended input buffers to implement a pseudo-differential input. In this case, only the positive polarity input is used in the speed path while the negative input is not connected internally. In other words, only the non-inverted pin is required to be specified in your design, while the Quartus II software automatically generates the inverted pin for you.

Although the Quartus II software does not support 1.5-V pseudo-differential HSTL I/O standards on left I/O banks, you can implement these standards at these banks. You need to create two pins in the designs and configure the pins with single-ended 1.5-V HSTL standards. However, this is limited only to pins that support the differential pin-pair I/O function and is dependent on the single-ended 1.5-V HSTL standards support at these banks.

Figure 8–16. 1.5-V Differential HSTL Class I Termination

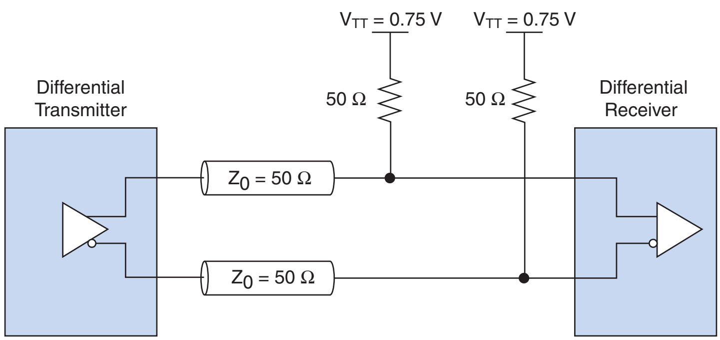
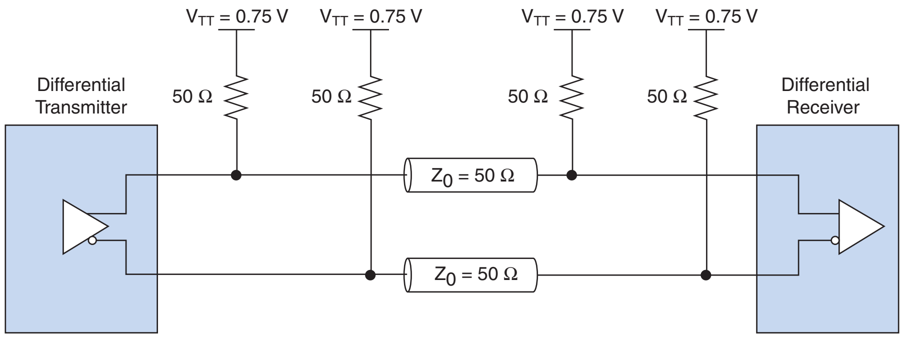


Figure 8–17. 1.5-V Differential HSTL Class II Termination



LVDS

The LVDS standard is formulated under the ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Arria GX devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level. However, LVDS clock output pins in the top and bottom I/O banks require a 3.3-V V_{CCIO} level. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. The ANSI/TIA/EIA-644 standard specifies LVDS transmitters and receivers capable of operating at recommended maximum data signaling rates of 655 Mbps. However, devices can operate at slower speeds if needed, and there is a theoretical maximum of 1.923 Gbps. Arria GX devices are capable of running at a maximum data rate of 840 Mbps and still meet the ANSI/TIA/EIA-644 standard.

Because of the low-voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS), transistor-to-transistor logic (TTL), and positive (or pseudo) emitter coupled logic (PECL). This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. Arria GX devices provide an optional 100-Ω differential LVDS termination resistor in the device using on-chip differential termination. Arria GX devices support both input and output levels operation.

Differential LVPECL

The low-voltage positive (or pseudo) emitter coupled logic (LVPECL) standard is a differential interface standard requiring a 3.3-V V_{CCIO}. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. Figures 8–18 and 8–19 show two alternate termination schemes for LVPECL.

☞ Arria GX devices support both input and output levels operation.

Figure 8–18. LVPECL DC Coupled Termination

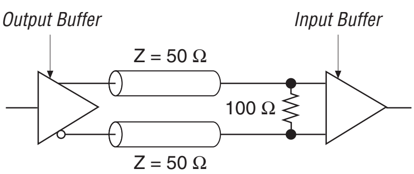
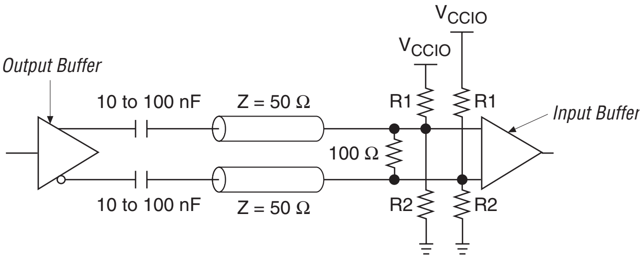


Figure 8–19. LVPECL AC Coupled Termination



HyperTransport Technology

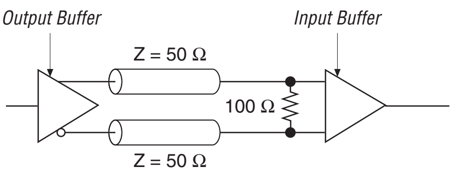
The HyperTransport standard is formulated by the HyperTransport Consortium.

The HyperTransport I/O standard is a differential high-speed, high-performance I/O interface standard requiring a 2.5- or 3.3-V V_{CCIO}. This standard is used in applications such as high-performance networking, telecommunications, embedded systems, consumer electronics, and Internet connectivity devices. The HyperTransport I/O standard is a point-to-point standard in which each HyperTransport bus consists of two point-to-point unidirectional links. Each link is 2 to 32 bits.

The HyperTransport standard does not require an input reference voltage. However, it does require a 100-Ω termination resistor between the two signals at the input buffer. Figure 8–20 shows HyperTransport termination. Arria GX devices include an optional 100-Ω differential HyperTransport termination resistor in the device using on-chip differential termination.

☞ Arria GX devices support both input and output levels operation.

Figure 8–20. HyperTransport Termination



Arria GX External Memory Interfaces

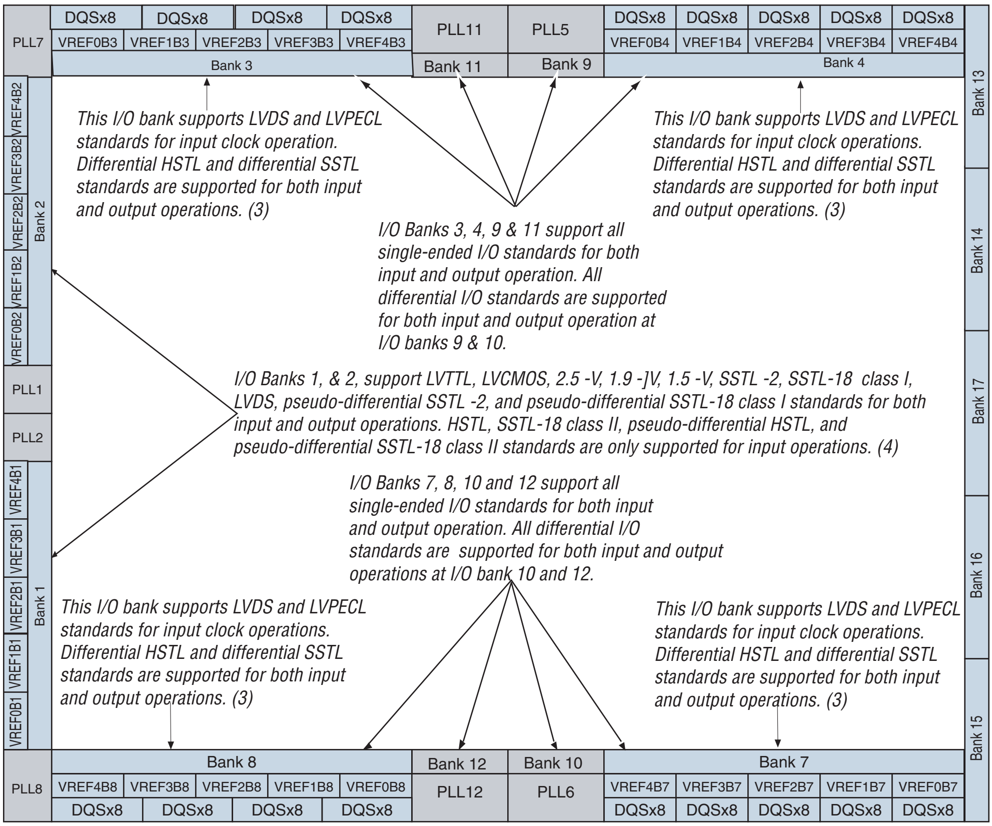
The increasing demand for higher-performance data processing systems often requires memory-intensive applications. Arria GX devices can interface with many types of external memory.

Refer to the *External Memory Interfaces in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook* for more information about the external memory interface support in Arria GX devices.

Arria GX I/O Banks

Arria GX devices have six general I/O banks and four enhanced phase-locked loop (PLL) external clock output banks (Figure 8–21). I/O banks 9 through 12 are enhanced PLL external clock output banks located on the top and bottom of the device.

Figure 8–21. Arria GX I/O Banks *Note (1), (2), (3), (4), (5), (6)*



Notes to Figure 8–21:

(1) Figure 8–21 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature transceiver and DPA circuitry for high speed differential I/O standards. Refer to the *High-Speed Differential I/O Interfaces in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*, or the *Arria GX Transceiver User Guide* for more information about differential I/O standards.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. Refer to the "Differential I/O Standards" on page 8–10 if you need to implement these standards at these I/O banks.

(6) PLLs 7, 8, 11, and 12 are available only in EP1AGX50D, EP1AGX60E, and EP1AGX90E devices.

Programmable I/O Standards

Arria GX device programmable I/O standards deliver high-speed and high-performance solutions in many complex design systems. This section discusses the I/O standard support in the I/O banks of Arria GX devices.

Regular I/O Pins

Most Arria GX device pins are multi-function pins. These pins support regular inputs and outputs as their primary function, and offer an optional function such as DQS, differential pin-pair, or PLL external clock outputs. For example, you can configure a multi-function pin in the enhanced PLL external clock output bank as a PLL external clock output when it is not used as a regular I/O pin.

☞ I/O pins that reside in PLL banks 9 through 12 are powered by the `VCC_PLL`<*5, 6, 11, or 12*>`_OUT` pins, respectively. Some devices/packages do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the `VCCIO3` pin, and any I/O pins that reside in bank 12 are powered by the `VCCIO8` pin.

Table 8–2 shows the I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Arria GX devices.

Table 8–2. Arria GX Regular I/O Standards Support (Part 1 of 2)

I/O Standard	General I/O Bank *(1)*						Enhanced PLL External Clock Output Bank *(2)*			
	1	2	3	4	7	8	9	10	11	12
LVTTL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI			✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI-X			✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class II	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 8–2. Arria GX Regular I/O Standards Support (Part 2 of 2)

I/O Standard	General I/O Bank *(1)*						Enhanced PLL External Clock Output Bank *(2)*			
	1	2	3	4	7	8	9	10	11	12
1.8-V HSTL Class II	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL Class II	*(3)*	*(3)*	✓	✓	✓	✓	✓	✓	✓	✓
1.2-V HSTL				✓	✓	✓				
Differential SSTL-2 Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
Differential SSTL-2 Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
Differential SSTL-18 Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
Differential SSTL-18 Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
1.8-V differential HSTL Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
1.8-V differential HSTL Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
1.5-V differential HSTL Class I	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
1.5-V differential HSTL Class II	*(4)*	*(4)*	*(5)*	*(5)*	*(5)*	*(5)*				
LVDS	✓	✓	*(6)*	*(6)*	*(6)*	*(6)*	✓	✓	✓	✓
HyperTransport technology	✓	✓								
Differential LVPECL			*(6)*	*(6)*	*(6)*	*(6)*	✓	✓	✓	✓

Notes to Table 8–2:

(1) Banks 5 and 6 are not available in Arria GX Devices.
(2) A mixture of single-ended and differential I/O standards is not allowed in enhanced PLL external clock output bank.
(3) This I/O standard is only supported for the input operation in this I/O bank.
(4) Although the Quartus II software does not support pseudo-differential SSTL-2 I/O standards on the left and right I/O banks, you can implement these standards at these banks. Refer to "Differential I/O Standards" on page 8–10 for details.
(5) This I/O standard is supported for both input and output operations for pins that support the DQS function. Refer to "Differential I/O Standards" on page 8–10 for details.
(6) This I/O standard is only supported for the input operation for pins that support PLL `INCLK` function in this I/O bank.

Clock I/O Pins

The PLL clock I/O pins consist of clock inputs (`INCLK`), external feedback inputs (`FBIN`), and external clock outputs (`EXTCLK`). Clock inputs are located on the left I/O banks (banks 1 and 2) to support fast PLLs, and at the top and bottom I/O banks (banks 3, 4, 7, and 8) to support enhanced PLLs. Both external clock outputs and external feedback inputs are located at enhanced PLL external clock output banks (banks 9, 10, 11, and 12) to support enhanced PLLs.

Table 8–3 shows the PLL clock I/O support in the I/O banks of Arria GX devices.

Table 8–3. I/O Standards Supported for Arria GX PLL Pins

I/O Standard	Enhanced PLL *(1)*			Fast PLL
	Input		Output	Input
	INCLK	FBIN	EXTCLK	INCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓
3.3-V PCI	✓	✓	✓	
3.3-V PCI-X	✓	✓	✓	
SSTL-2 Class I	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓
SSTL-18 Class II	✓	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓	✓
1.8-V HSTL Class II	✓	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓	✓
1.5-V HSTL Class II	✓	✓	✓	✓
Differential SSTL-2 Class I	✓	✓	✓	
Differential SSTL-2 Class II	✓	✓	✓	
Differential SSTL-18 Class I	✓	✓	✓	
Differential SSTL-18 Class II	✓	✓	✓	
1.8-V differential HSTL Class I	✓	✓	✓	
1.8-V differential HSTL Class II	✓	✓	✓	
1.5-V differential HSTL Class I	✓	✓	✓	
1.5-V differential HSTL Class II	✓	✓	✓	
LVDS	✓	✓	✓	✓
HyperTransport technology				✓
Differential LVPECL	✓	✓	✓	

Note to Table 8–3:

(1) The enhanced PLL external clock output bank does not allow a mixture of both single-ended and differential I/O standards.

For more information, refer to the *PLLs in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*.

Voltage Levels

Arria GX devices specify a range of allowed voltage levels for supported I/O standards. Table 8–4 shows only typical values for input and output V_{CCIO}, V_{REF}, as well as the board V_{TT}.

Table 8–4. Arria GX I/O Standards & Voltage Levels (Part 1 of 2) Note (1)

I/O Standard	Arria GX					
	V_{CCIO} (V)				V_{REF} (V)	V_{TT} (V)
	Input Operation		Output Operation			
	Top & Bottom I/O Banks	Left & Right I/O Banks (3)	Top & Bottom I/O Banks	Left & Right I/O Banks (3)	Input	Termination
LVTTL	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA
LVCMOS	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA
2.5 V	3.3/2.5	3.3/2.5	2.5	2.5	NA	NA
1.8 V	1.8/1.5	1.8/1.5	1.8	1.8	NA	NA
1.5 V	1.8/1.5	1.8/1.5	1.5	1.5	NA	NA
3.3-V PCI	3.3	NA	3.3	NA	NA	NA
3.3-V PCI-X	3.3	NA	3.3	NA	NA	NA
SSTL-2 Class I	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	1.8	1.8	1.8	1.8	0.90	0.90
SSTL-18 Class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V HSTL Class I	1.8	1.8	1.8	1.8	0.90	0.90
1.8-V HSTL Class II	1.8	1.8	1.8	NA	0.90	0.90
1.5-V HSTL Class I	1.5	1.5	1.5	1.5	0.75	0.75
1.5-V HSTL Class II	1.5	1.5	1.5	NA	0.75	0.75
1.2-V HSTL (4)	1.2	NA	1.2	NA	0.6	NA
Differential SSTL-2 Class I	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-2 Class II	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-18 Class I	1.8	1.8	1.8	1.8	0.90	0.90

Table 8–4. Arria GX I/O Standards & Voltage Levels (Part 2 of 2) Note (1)

I/O Standard	Arria GX					
	V_{CCIO} (V)				V_{REF} (V)	V_{TT} (V)
	Input Operation		Output Operation		Input	Termination
	Top & Bottom I/O Banks	Left & Right I/O Banks (3)	Top & Bottom I/O Banks	Left & Right I/O Banks (3)		
Differential SSTL-18 Class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL Class I	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL Class II	1.8	1.8	1.8	NA	0.90	0.90
1.5-V differential HSTL Class I	1.5	1.5	1.5	NA	0.75	0.75
1.5-V differential HSTL Class II	1.5	1.5	1.5	NA	0.75	0.75
LVDS (2)	3.3/2.5/1.8/1.5	2.5	3.3	2.5	NA	NA
HyperTransport technology	NA	2.5	NA	2.5	NA	NA
Differential LVPECL (2)	3.3/2.5/1.8/1.5	NA	3.3	NA	NA	NA

Notes to Table 8–4:

(1) Any input pins with PCI-clamping-diode enabled force the V_{CCIO} to 3.3 V.

(2) LVDS and LVPECL output operation in the top and bottom banks is only supported in PLL banks 9-12. The V_{CCIO} level for differential output operation in the PLL banks is 3.3 V. The V_{CCIO} level for output operation in the left and right I/O banks is 2.5 V.

(3) The right I/O bank on Arria GX devices consists of transceivers.

(4) 1.2-V HSTL is only supported in I/O banks 4, 7, and 8.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Arria GX Device Handbook* for detailed electrical characteristics of each I/O standard.

On-Chip Termination

Arria GX devices feature on-chip series termination to provide I/O impedance matching and termination capabilities. Apart from maintaining signal integrity, this feature also minimizes the need for external resistor networks, thereby saving board space and reducing costs.

Arria GX devices support on-chip series (R_S) termination for single-ended I/O standards and on-chip differential termination (R_D) for differential I/O standards. This section discusses the on-chip series termination support.

For more information about differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter in volume 2 of the Arria *GX Device Handbook.*

Arria GX devices support I/O driver on-chip series (R_S) termination through drive strength control for single-ended I/Os.

On-Chip Series Termination without Calibration

Arria GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Arria GX devices support on-chip series termination for single-ended I/O standards (see Figure 8–22). The R_S shown in Figure 8–22 is the intrinsic impedance of transistors. The typical R_S values are 25 Ω and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable.

Figure 8–22. Arria GX On-Chip Series Termination without Calibration

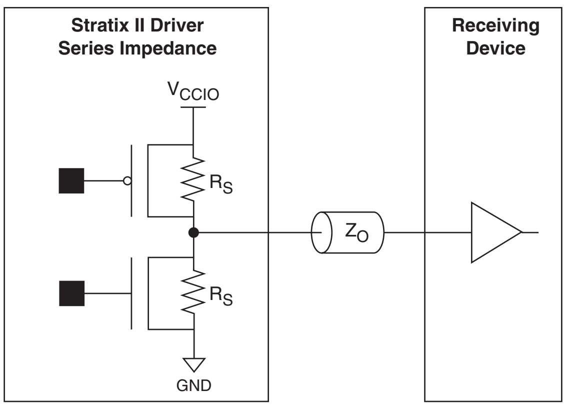


Table 8–5 shows the list of output standards that support on-chip series termination without calibration.

Table 8–5. Selectable I/O Drivers with On-Chip Series Termination without Calibration

I/O Standard	On-chip Series Termination Setting		
	Row I/O	Column I/O	Unit
3.3-V LVTTL	50	50	Ω
	25	25	Ω
3.3-V LVCMOS	50	50	Ω
	25	25	Ω
2.5-V LVTTL	50	50	Ω
	25	25	Ω
2.5-V LVCMOS	50	50	Ω
	25	25	Ω
1.8-V LVTTL	50	50	Ω
		25	Ω
1.8-V LVCMOS	50	50	Ω
		25	Ω
1.5-V LVTTL	50	50	Ω
1.5-V LVCMOS	50	50	Ω
SSTL-2 Class I	50	50	Ω
SSTL-2 Class II	25	25	Ω
SSTL-18 Class I	50	50	Ω
SSTL-18 Class II		25	Ω
1.8-V HSTL Class I	50	50	Ω
1.8-V HSTL Class II		25	Ω
1.5-V HSTL Class I	50	50	Ω
1.2-V HSTL *(1)*		50	Ω

Note to Table 8–5:

(1) 1.2-V HSTL is only supported in I/O banks 4, 7, and 8.

To use on-chip termination for the SSTL Class I standard, select the 50-Ω on-chip series termination setting for replacing the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, select the 25-Ω on-chip series termination setting (to match the 50-Ω transmission line and the near end 50-Ω pull-up to V_{TT}).

For more information about tolerance specifications for on-chip termination without calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Arria GX Device Handbook*.

Design Considerations

While Arria GX devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs.

I/O Termination

I/O termination requirements for single-ended and differential I/O standards are discussed in this section.

Single-Ended I/O Standards

Although single-ended, non-voltage-referenced I/O standards do not require termination, impedance matching is necessary to reduce reflections and improve signal integrity.

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL standards to produce a reliable DDR memory system with superior noise margin.

Arria GX on-chip series termination provides the convenience of no external components. External pull-up resistors can be used to terminate the voltage-referenced I/O standards such as SSTL-2 and HSTL.

Refer to "Arria GX I/O Standards Support" on page 8–2 for more information about the termination scheme of various single-ended I/O standards.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus. Arria GX devices provide an optional differential on-chip resistor when using LVDS and HyperTransport standards.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Arria GX devices.

Non-Voltage-Referenced Standards

Each Arria GX device I/O bank has its own V_{CCIO} pins and supports only one V_{CCIO}, either 1.5, 1.8, 2.5, or 3.3 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 8–6.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Since an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3.3-V LVCMOS inputs (not output or bidirectional pins).

Table 8–6. Acceptable Input Levels for LVTTL & LVCMOS

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ *(1)*		
2.5	✓	✓		
1.8	✓ *(2)*	✓ *(2)*	✓	✓ *(1)*
1.5	✓ *(2)*	✓ *(2)*	✓	✓

Notes to Table 8–6:

(1) Because the input signal does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Arria GX device's I/O bank supports multiple V_{REF} pins feeding a common V_{REF} bus. The number of available V_{REF} pins increases as device density increases. If these pins are not used as V_{REF} pins, they cannot be used as generic I/O pins. However, each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

Because of performance reasons, voltage-referenced input standards use their own V_{CCIO} level as the power source. For example, you can only place 1.5-V HSTL input pins in an I/O bank with a 1.5-V V_{CCIO}.

☞ Refer to "Arria GX I/O Banks" on page 8–20 for details about input V_{CCIO} for voltage-referenced standards.

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

☞ Refer to "I/O Placement Guidelines" on page 8–30 for details about voltage-referenced I/O standards placement.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 2.5-V (inputs, but not outputs), and HSTL I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

I/O Placement Guidelines

The I/O placement guidelines help to reduce noise issues that may be associated with a design such that Arria GX devices can maintain an acceptable noise level on the V_{CCIO} supply. Because Arria GX devices require each bank to be powered separately for V_{CCIO}, these noise issues have no effect when crossing bank boundaries and, as such, these rules need not be applied.

This section provides I/O placement guidelines for the programmable I/O standards supported by Arria GX devices and includes essential information for designing systems using their devices' selectable I/O capabilities.

V_{REF} Pin Placement Restrictions

There are at least two dedicated V_{REF} pins per I/O bank to drive the V_{REF} bus. Larger Arria GX devices have more V_{REF} pins per I/O bank. All V_{REF} pins within one I/O bank are shorted together at device die level.

There are limits to the number of pins that a V_{REF} pin can support. For example, each output pin adds some noise to the V_{REF} level and an excessive number of outputs make the level too unstable to be used for incoming signals.

Restrictions on the placement of single-ended voltage-referenced I/O pads with respect to V_{REF} pins help maintain an acceptable noise level on the V_{CCIO} supply and prevent output switching noise from shifting the V_{REF} rail.

Input Pins

Each V_{REF} pin supports a maximum of 40 input pads.

Output Pins

When a voltage-referenced input or bidirectional pad does not exist in a bank, the number of output pads that can be used in that bank depends on the total number of available pads in that same bank. However, when a voltage-referenced input exists, a design can use up to 20 output pads per V_{REF} pin in a bank.

Bidirectional Pins

Bidirectional pads must satisfy both input and output guidelines simultaneously. The general formulas for input and output rules are shown in Table 8–7.

Table 8–7. Bidirectional Pin Limitation Formulas

Rules	Formulas
Input	<Total number of bidirectional pins> + <Total number of V_{REF} input pins, if any> $\leq$ 40 per V_{REF} pin
Output	<Total number of bidirectional pins> + <Total number of output pins, if any> – <Total number of pins from smallest OE group, if more than one OE groups> $\leq$ 20 per V_{REF} pin

- If the same output enable (OE) controls all the bidirectional pads (bidirectional pads in the same OE group are driving in and out at the same time) and there are no other outputs or voltage-referenced inputs in the bank, the voltage-referenced input is never active at the same time as an output. Therefore, the output limitation rule does not apply. However, since the bidirectional pads are linked to the same OE, the bidirectional pads will all act as inputs at the same time. Therefore, there is a limit of 40 input pads, as follows:

  <Total number of bidirectional pins> + *<Total number of* V_{REF} *input pins>* $\leq$ 40 per V_{REF} pin

- If any of the bidirectional pads are controlled by different OE and there are no other outputs or voltage-referenced inputs in the bank, one group of bidirectional pads can be used as inputs and another group is used as outputs. In such cases, the formula for the output rule is simplified, as follows:

  <Total number of bidirectional pins> – *<Total number of pins from smallest OE group>* $\leq$ 20 per V_{REF} pin

- Consider a case where eight bidirectional pads are controlled by OE1, eight bidirectional pads are controlled by OE2, six bidirectional pads are controlled by OE3, and there are no other outputs or voltage-referenced inputs in the bank. While this totals 22 bidirectional pads, it is safely allowable because there would be a possible maximum of 16 outputs per V_{REF} pin, assuming the worst case where OE1 and OE2 are active and OE3 is inactive. This is useful for DDR SDRAM applications.

- When at least one additional voltage-referenced input and no other outputs exist in the same V_{REF} group, the bidirectional pad limitation must simultaneously adhere to the input and output limitations. The input rule becomes:

  <Total number of bidirectional pins> + *<Total number of* V_{REF} *input pins>* $\leq$ 40 per V_{REF} pin

  Whereas the output rule is simplified as:

  <Total number of bidirectional pins> 20 per V_{REF} pin

- When at least one additional output exists but no voltage-referenced inputs exist, the output rule becomes:

  <Total number of bidirectional pins> + *<Total number of output pins>* – *<Total number of pins from smallest OE group>* $\leq$ 0 per V_{REF} pin

- When additional voltage-referenced inputs and other outputs exist in the same V_{REF} group, the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. The input rule is:

  <Total number of bidirectional pins> + *<Total number of V_{REF} input pins>* ≤ 40 per V_{REF} pin

  Whereas the output rule is given as:

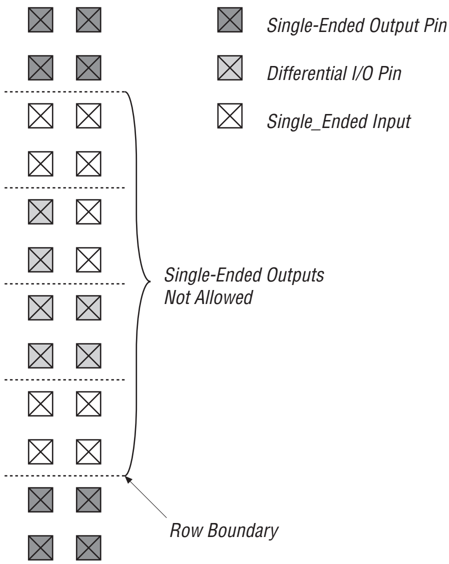
  <Total number of bidirectional pins> + *<Total number of output pins>* – *<Total number of pins from smallest OE group>* ≤ 0 per V_{REF} pin

I/O Pin Placement with Respect to High-Speed Differential I/O Pins

Regardless of whether or not the SERDES circuitry is utilized, there is a restriction on the placement of single-ended output pins with respect to high-speed differential I/O pins. As shown in Figure 8–23, all single-ended outputs must be placed at least one LAB row away from the differential I/O pins. There are no restrictions on the placement of single-ended input pins with respect to differential I/O pins. Single-ended input pins may be placed within the same LAB row as differential I/O pins. However, the single-ended input's IOE register is not available. The input must be implemented within the core logic.

This single-ended output pin placement restriction only applies when using the LVDS or HyperTransport I/O standards in the left I/O banks. There are no restrictions for single-ended output pin placement with respect to differential clock pins in the top and bottom I/O banks.

Figure 8–23. Single-Ended Output Pin Placement with Respect to Differential I/O Pins



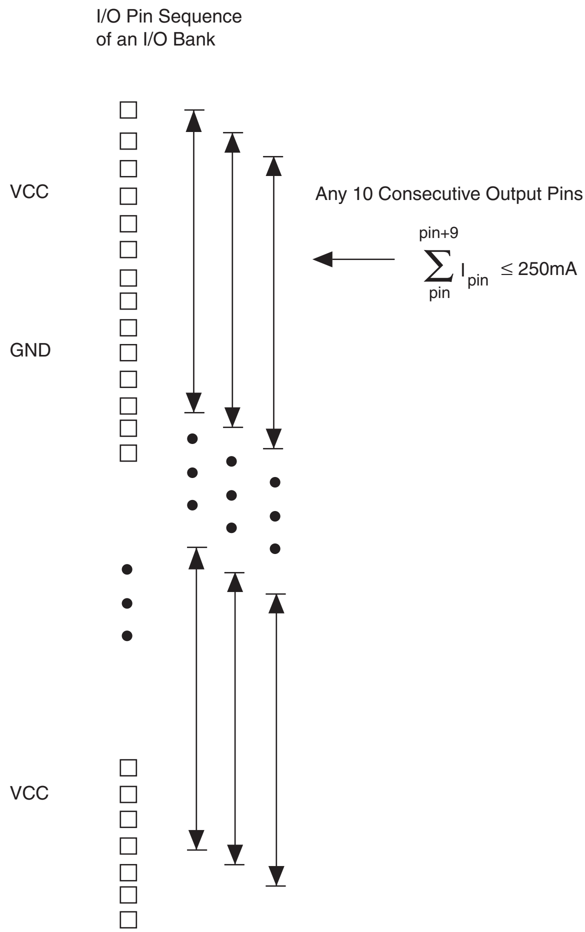
DC Guidelines

Power budgets are essential to ensure the reliability and functionality of a system application. You are often required to perform power dissipation analysis on each device in the system to come out with the total power dissipated in that system, which is composed of a static component and a dynamic component.

The static power consumption of a device is the total DC current flowing from V_{CCIO} to ground.

For any ten consecutive pads in an I/O bank of an Arria GX device, Altera recommends a maximum current of 250 mA, as shown in Figure 8–24, because the placement of V_{CCIO}/ground (GND) bumps are regular, 10 I/O pins per pair of power pins. This limit is on the static power consumed by an I/O standard, as shown in Table 8–8. Limiting static power is a way to improve reliability over the lifetime of the device.

Figure 8–24. DC Current Density Restriction *Notes (1), (2)*



Notes to Figure 8–24:

(1) The consecutive pads do not cross I/O banks.

(2) V_{REF} pins do not affect DC current calculation because there are no V_{REF} pads.

Table 8–8 shows the I/O standard DC current specification.

Table 8–8. Arria GX I/O Standard DC Current Specification (Part 1 of 2) *Note (1)*

I/O Standard	I_{PIN} (mA), Top & Bottom I/O Banks	I_{PIN} (mA), Left I/O Banks *(2)*
LVTTL	*(3)*	*(3)*
LVCMOS	*(3)*	*(3)*

I/O Standard	I_{PIN} (mA), Top & Bottom I/O Banks	I_{PIN} (mA), Left I/O Banks (2)
2.5 V	(3)	(3)
1.8 V	(3)	(3)
1.5 V	(3)	(3)
3.3-V PCI	1.5	NA
3.3-V PCI-X	1.5	NA
SSTL-2 Class I	12 (4)	12 (4)
SSTL-2 Class II	24 (4)	16 (4)
SSTL-18 Class I	12 (4)	10 ((4)
SSTL-18 Class II	20 (4)	NA
1.8-V HSTL Class I	12 (4)	12
1.8-V HSTL Class II	20 (4)	NA
1.5-V HSTL Class I	12 (4)	8
1.5-V HSTL Class II	20 (4)	NA
Differential SSTL-2 Class I	12	12
Differential SSTL-2 Class II	24	16
Differential SSTL-18 Class I	12	10
Differential SSTL-18 Class II	20	NA
1.8-V differential HSTL Class I	12	12
1.8-V differential HSTL Class II	20	NA
1.5-V differential HSTL Class I	12	8
1.5-V differential HSTL Class II	20	NA
LVDS	12	12
HyperTransport technology	NA	16
Differential LVPECL	10	10

Table 8–8. Arria GX I/O Standard DC Current Specification (Part 2 of 2) Note (1)

Notes to Table 8–8:

(1) The current value obtained for differential HSTL and differential SSTL standards is per pin and not per differential pair, as opposed to the per-pair current value of LVDS and HyperTransport standards.

(2) This does not apply to the right I/O banks of Arria GX devices. Arria GX devices have transceivers on the right I/O banks.

(3) The DC power specification of each I/O standard depends on the current sourcing and sinking capabilities of the I/O buffer programmed with that standard, as well as the load being driven. LVTTL, LVCMOS, 2.5-V, 1.8-V, and 1.5-V outputs are not included in the static power calculations because they normally do not have resistor loads in real applications. The voltage swing is rail-to-rail with capacitive load only. There is no DC current in the system.

(4) This I_{PIN} value represents the DC current specification for the default current strength of the I/O standard. The I_{PIN} varies with programmable drive strength and is the same as the drive strength as set in Quartus II software. Refer to the *Arria GX Architecture* chapter in volume 1 of the *Arria GX Device Handbook* for a detailed description of the programmable drive strength feature of voltage-referenced I/O standards.

Table 8–8 only shows the limit on the static power consumed by an I/O standard. The amount of power used at any given moment could be much higher, and is based on the switching activities.

Conclusion

Arria GX devices provide I/O capabilities that allow you to work in compliance with current and emerging I/O standards and requirements. With the Arria GX device features, such as programmable driver strength, you can reduce board design interface costs and increase the development flexibility.

References

Refer to the following references for more information:

- Interface Standard for Nominal 3V/ 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- 2.5-V +/- 0.2V (Normal Range) and 1.8-V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- 1.8-V +/- 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- 1.5-V +/- 0.1 V (Normal Range) and 0.9 V - 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- PCI-X Local Bus Specification, Revision 1.0a, PCI Special Interest Group.
- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9A, Electronic Industries Association, December 2000.
- Stub Series Terminated Logic for 1.8 V (SSTL-18), Preliminary JC42.3, Electronic Industries Association.
- High-Speed Transceiver Logic (HSTL)—A 1.5-V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/JESD8-6, Electronic Industries Association, August 1995.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

Referenced Documents

This chapter references the following documents:

- *Arria GX Architecture* chapter in volume 1 of the *Arria GX Device Handbook*
- *DC & Switching Characteristics* chapter in volume 1 of the *Arria GX Device Handbook*
- *External Memory Interfaces in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*
- *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*
- *PLLs in Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*

Document Revision History

Table 8–9 shows the revision history for this chapter.

Table 8–9. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2008 v1.2	Updated “1.5-V HSTL Class I & 1.5-V HSTL Class II” section.	—
	Minor text edits.	—
August 2007 v1.1	Added the “Referenced Documents” section.	—
	Minor text edits.	—
May 2007 v1.0	Initial release.	—