

This errata sheet provides updated information about known Stratix® IV GX device issues affecting HardCopy® IV GX devices.

Table 1 lists specific Stratix IV GX issues and if HardCopy IV GX devices are affected by each issue.

Table 1. Stratix IV GX Device Issues Affecting HardCopy IV GX Devices (Part 1 of 2) (Note 1), (2)

| Known Stratix IV GX Issue | Affected Stratix IV GX Devices | Stratix IV GX Planned Fix | HardCopy IV GX Affected? |
|---|---|--|--------------------------|
| <p>“PCI 66 MHz Timing Closure” The PCI 66 MHz interface in the HardCopy device will not close timing if the column IOs (top/bottom) are used.</p> | None | — | Yes |
| <p>“PLL phasedone Signal Stuck at Low” In some cases, the HardCopy IV GX phase-locked loop (PLL) blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift.</p> | All Stratix IV GX (ES and production) devices | Quartus II software version 12.0 and later | Yes |
| <p>“V_{CCHIP} Power Supply Requirement for PCIe Gen2 x8 Applications” Transceiver blocks (on the left and right sides) will not operate correctly if both V_{CCHIP_L} and V_{CCHIP_R} are not powered on when one of the transceiver blocks is configured in PCI Express® (PCIe®) Gen2 x8 mode.</p> | None | — | Yes |
| <p>“Higher Power Supply Current During Power-Up for VCCPD and VCCA_L/R” Higher power-up current requirements are needed for V_{CCHPD} and V_{CCA_L/R} power supplies.</p> | All Stratix IV GX (ES and production) devices | Refer to “Higher Power Supply Current During Power-Up for VCCPD and VCCA_L/R” (3) | Yes |
| <p>The PCIe rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established.</p> | All Stratix IV GX (ES and production) devices | Quartus® II 10.1 SP1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.1. | Yes |
| <p>The Quartus II software incorrectly sets the CDR unit when the transceiver channel is configured in any mode except PCIe mode and the CDR is configured to automatic lock mode.</p> | All Stratix IV GX (ES and production) devices | Quartus II software 10.1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.0 SP1. | Yes |

Table 1. Stratix IV GX Device Issues Affecting HardCopy IV GX Devices (Part 2 of 2) (Note 1), (2)

| Known Stratix IV GX Issue | Affected Stratix IV GX Devices | Stratix IV GX Planned Fix | HardCopy IV GX Affected? |
|--|---|---|--------------------------|
| The transceiver may not be initialized correctly if your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode. | All Stratix IV GX (ES and production) devices | No plan to fix silicon. Apply the reset sequence in “Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode.” | Yes |
| The Quartus II software incorrectly maps the PCIe interfaces when using the hard IP block. | All Stratix IV GX (ES and production) devices | For more information, refer to “Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block.” | Yes |
| Affected Stratix IV GX production devices may exhibit higher than expected jitter on general purpose I/O pins. | <ul style="list-style-type: none"> ■ EP4SGX70 ■ EP4SGX110 ■ EP4SGX290 ■ EP4SGX360, ■ EP4SGX530 | Silicon Revision | No |
| Stratix IV GX configuration fails in FPP mode when the DCLK frequency is set to 125 MHz with a 60/40 or 40/60 duty cycle. | All production devices | — | No |
| Stratix IV GX configuration fails in FPP mode when the minimum data hold time (tDH) is set to 0 ns for uncompressed and unencrypted configuration data, or 24 ns for compressed and/or encrypted data. | All production devices | — | No |
| The transmitter PLL lock status signal (pll_locked) does not de-assert when the pll_powerdown signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8. | All Stratix IV GX (ES and production) devices | No plan to fix silicon. | Yes |
| M144K RAM blocks may lock up if there is a glitch in the clock source. | All production devices | — | Yes |
| ×N clock line performance limits data rates depending on clock source configuration. | All production devices | — | Yes |
| The device fails to power up and exit POR at low temperatures when V _{CC} is powered after V _{CCAUX} . | All production devices | — | No |

Notes to Table 1:

- (1) For details and solutions of an issue, refer to the [Errata Sheet for Stratix IV GX Devices](#).
- (2) Solutions affect both Stratix IV GX and HardCopy IV GX devices (if applicable).
- (3) The Stratix IV GX solution does not apply to HardCopy IV GX devices.

PCI 66 MHz Timing Closure

The PCI 66 MHz interface in the HardCopy IV GX device will not close timing if the column (top/bottom) IO pins are used. To close timing on the PCI 66 MHz interface, the PCI 66 MHz clock must drive the periphery clock (PCLK) network, which can only be driven from the row (left/right) IO pins. Ensure that you assign this PCI clock to a row IO pin that has direct access to the PCLK network.

Additionally, you must provide external off-chip clamping diodes because the row IOs do not support on-chip clamping diodes. HardCopy IV GX customers will require FPGA/HardCopy board modifications to accommodate the external clamping diodes.

The HardCopy IV GX device will not meet timing even if the Quartus II version 10.1 or earlier compilation may show that the PCI 66 MHz interface related paths meet the core timing.



The Quartus II software version 11.1 is the minimum software version for handoff.

The above are general guidelines and may not work under all conditions. If you plan to use the PCI 66 MHz interface in your HardCopy IV GX design, contact Altera® Technical Support at www.altera.com/mysupport for more information.

There is no planned issue fix for HardCopy IV GX devices.

PLL phasedone Signal Stuck at Low

In some cases, the HardCopy IV GX PLL blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift. When the PLL phasedone signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL phasedone signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the phasestep signal.

To resolve the PLL phasedone signal stuck at low issue, the Altera PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL phasedone signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the phasedone signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the [PLL Phasedone Stuck at Low Solution](#).

If you need additional support, file a service request using [mySupport](#).

V_{CCHIP} Power Supply Requirement for PCIe Gen2 x8 Applications

If your HardCopy IV GX device implements PCIe Gen2 x8 mode on one transceiver side (left or right), both V_{CCHIP_L} and V_{CCHIP_R} must be powered up in order for the two transceiver sides to function correctly.

Although this issue does not affect Stratix IV GX devices, ensure that both these power supplies are taken into consideration in your board design if you plan to migrate to HardCopy IV GX devices.

Higher Power Supply Current During Power-Up for V_{CCPD} and V_{CCA_L/R}

HardCopy IV GX devices require higher power-up current levels for the V_{CCPD} power supply than previously specified. The Quartus® II software and PowerPlay Early Power Estimator (EPE) version 9.1SP2 and later versions correctly show the V_{CCPD} power-on current for production devices.

HardCopy IV GX functionality is not affected by this issue, even if your V_{CCPD} and/or V_{CCA_L/R} power supplies are designed with output current levels below what the Quartus II software and/or EPE specify. HardCopy IV GX devices will power-up and operate correctly as expected, provided the supplies power up monotonically and the minimum voltage requirement is met. V_{CCPD} must meet the minimum power supply voltage requirement for the device to exit power-on reset (POR). After the device exits POR, the V_{CCPD} current requirements return to what is reported by Altera's power estimation tools. Overall thermal power and operating current levels are not affected by this issue.

If there are other devices on the board that share the V_{CCPD} and/or V_{CCA_L/R} power supplies, you can use the Quartus II software and/or the EPE to estimate power supply current requirements. This analysis may be needed if the other devices on the board have stringent power supply integrity requirements.

There is no planned fix for the higher power-up current requirements.

Document Revision History

Table 2 lists the revision history for this Errata Sheet.

Table 2. Document Revision History

| Date | Version | Changes |
|---------------|---------|--|
| February 2012 | 1.2 | <ul style="list-style-type: none"> ■ Added the "PCI 66 MHz Timing Closure" section. ■ Added the "PLL phasedone Signal Stuck at Low" section. |
| August 2011 | 1.1 | Added the "VCCHIP Power Supply Requirement for PCIe Gen2 x8 Applications" section. |
| March 2011 | 1.0 | Initial release. |