

## **Stratix® III Device Family Pin Connection Guidelines PCG-01004-1.2**

© 2008 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

PLEASE REVIEW THE FOLLOWING TERMS AND CONDITIONS CAREFULLY BEFORE USING THE PIN CONNECTION GUIDELINES("GUIDELINES") PROVIDED TO YOU. BY USING THESE GUIDELINES, YOU INDICATE YOUR ACCEPTANCE OF SUCH TERMS AND CONDITIONS, WHICH CONSTITUTE THE LICENSE AGREEMENT ("AGREEMENT") BETWEEN YOU AND ALTERA CORPORATION ("ALTERA"). IF YOU DO NOT AGREE WITH ANY OF THESE TERMS AND CONDITIONS, DO NOT DOWNLOAD, COPY, INSTALL, OR USE OF THESE GUIDELINES.

1. Subject to the terms and conditions of this Agreement, Altera grants to you the use of this pin connection guideline to determine the pin connections of an Altera® programmable logic device-based design. You may not use this pin connection guideline for any other purpose.
2. Altera does not guarantee or imply the reliability, or serviceability, of the pin connection guidelines or other items provided as part of these guidelines. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.
3. In no event shall the aggregate liability of Altera relating to this Agreement or the subject matter hereof under any legal theory (whether in tort, contract, or otherwise), exceed One US Dollar (US\$1.00). In no event shall Altera be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these guidelines even if advised of the possibility of such damages.
4. This Agreement shall be governed by the laws of the State of California, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the courts in the County of Santa Clara, State of California for the resolution of any dispute or claim arising out of or relating to this Agreement. The parties hereby agree that the party who is not the substantially prevailing party with respect to a dispute, claim, or controversy relating to this Agreement shall pay the costs actually incurred by the substantially prevailing party in relation to such dispute, claim, or controversy, including attorneys' fees.

BY DOWNLOADING OR USING THESE GUIDELINES, YOU ACKNOWLEDGE THAT YOU HAVE READ THIS AGREEMENT, UNDERSTAND IT, AND AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. YOU AND ALTERA FURTHER AGREE THAT IT IS THE COMPLETE AND EXCLUSIVE STATEMENT OF THE AGREEMENT BETWEEN YOU AND ALTERA, WHICH SUPERSEDES ANY PROPOSAL OR PRIOR AGREEMENT, ORAL OR WRITTEN, AND ANY OTHER COMMUNICATIONS BETWEEN YOU AND ALTERA RELATING TO THE SUBJECT MATTER OF THIS AGREEMENT.

Pin Connection Guidelines Agreement © 2008 Altera Corporation. All rights reserved.

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
<i>Supply and Reference Pins</i>			
VCCL	Power	VCCL supplies power to the core voltage power supply pins.	Altera recommends that you tie these pins to 1.1 V. However, for low power designs using Stratix III -4L speed grade devices, VCCL is powered by 0.9 V. If 1.1 V is used, this plane may be connected to the same power plane as VCC.
VCC	Power	VCC supplies power to the peripheral circuitry.	Connect these pins to a 1.1-V power supply. This plane may be shared with the VCCL power plane if VCCL is using 1.1 V. For best jitter performance on your PLL dedicated output clock, Altera recommends that you isolate VCC from VCCL, and use separate power supply decoupling (see note 2) when all the following design conditions are true: <ul style="list-style-type: none"> <li>• Core clock domain frequencies &lt; 100MHz (found in Quartus II output report file)</li> <li>• Design utilization (in sub-100MHz clock domains) &gt; 40% of total resources (found in Quartus II output report file)</li> <li>• Combinatorial logic (in sub-100MHz clock domains) with toggle rate &gt; 100%, as reported by Quartus II PowerPlay Power Analyzer</li> </ul>
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, Altera recommends that the pin be connected to the VCCIO of the bank in which the RUP pin resides, or GND. When using OCT, tie these pins to the required VCCIO banks through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. Refer to the Stratix III data sheet for the desired resistor value of the I/O standard used.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor Rdn must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, Altera recommends that the pin be connected to GND. When using OCT, tie these pins to GND through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. Refer to the Stratix III data sheet for the desired resistor value of the I/O standard used.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and LVTTTL(3.0 V, 3.3 V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), 3.0-V PCI/PCI-X and LVTTTL(3.0 V, 3.3 V) I/O standards.	Connect these pins to the desired voltage level required for the I/O standard on these banks. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, these pins are used as the voltage-referenced pins for the bank.	If VREF pins are not used, you should connect them to either the VCCIO in the bank where the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.

**Stratix<sup>®</sup> III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 2.5 V, even if the PLL is not used. Altera recommends that you keep these pins isolated from other VCC for better jitter performance.	Connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear supply. Power on the PLLs operating at the same frequency should be decoupled. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 1.1 V, even if the PLL is not used.	Connect these pins to 1.1 V, even if the PLL is not used. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VCCPT	Power	Power supply for the programmable power technology. Connect to 2.5 V.	Use an isolated linear 2.5-V power supply for these pins. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VCCPGM	Power	Dedicated Configuration power supply. Can be connected to 1.8 V, 2.5 V, 3.0 V or 3.3 V depending on the particular design.	Connect this pin to either 1.8 V, 2.5 V, 3.0 V, or 3.3 V power supply. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.3 V, 3.0 V, or 2.5 V. VCCPD for 3.3-V I/O standard is 3.3 V, VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.	The VCCPD pins require 2.5 V, 3.0 V or 3.3 V and must ramp-up from 0 V to 2.5V, 3.0 V, or 3.3 V within 100 ms to ensure successful configuration. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
VCCBAT	Power	Battery back-up power supply for design security volatile key register. Connect to 2.5 V.	Connect this pin to a 2.5-V non-volatile battery power source.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O bank. Connect to 2.5 V.	Connect these pins to a 2.5-V power source. Decoupling depends on the design decoupling requirements of the specific board. See Note 2.
GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.	These pins must be left unconnected.
NC	No Connect	Do not drive signals into these pins.	These pins must be left unconnected.
<b><i>Dedicated Configuration/JTAG Pins</i></b>			
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn, CRC_ERROR) are on or off before and during configuration. A logic high (1.8 V, 2.5 V, 3.0 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1 kΩ pull-up resistor or tied directly to GND depending on the use desired for the device. Refer to the description column.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix III device.	If the temperature-sensing diode is not used, connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix III device.	If the temperature-sensing diode is not used, connect this pin to GND.

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
MSEL[2..0]	Input	Configuration input pins that set the Stratix III device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCPGM or GND. Refer to the "Configuring Stratix III Devices" chapter in volume 1 of the Stratix III Handbook. If only JTAG configuration is used, connect these pins to ground.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single-device configuration and JTAG programming, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin. When using EPC2 devices, only external 10-kΩ pull-up resistors to VCCPGM should be used.
nCEO	Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single-device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	The OE and nCS pins of the enhanced configuration devices and EPC2 devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on these pins. For EPC2 devices, only external 10-kΩ pull-up resistors to VCCPGM should be used.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.8 V, 2.5 V, 3.0 V, or 3.3 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect this pin to a 1-kΩ pull-down resistor to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	Connect this pin to a 1-kΩ pull-up resistor to VCCPD.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	Connect this pin to a 1-kΩ pull-up resistor to VCCPD.
TDO	Output	Dedicated JTAG output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	If not used, tie this pin to a 1-kΩ pull-up resistor to VCCPD.

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
<b><i>Clock and PLL Pins</i></b>			
CLK[1,3,8,10]p	Clock, Input	Dedicated high-speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	Connect unused pins to GND.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	Connect unused pins to GND.
CLK[4..7,12..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[4..7,12..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.	Connect unused pins to GND.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.	Connect unused pins to GND.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	The left and right PLL each supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	Connect unused pins to GND.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock		Connect unused pins to GND.
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	Connect unused pins to GND.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock		Connect unused pins to GND.
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	Connect unused pins to GND.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.	Connect unused pins to GND.
<b><i>Optional/Dual-Purpose Configuration Pins</i></b>			
nCSO	Output	Dedicated output control signal from the Stratix III FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode, nCSO is not used. Also, when this pin is not used as an output, Altera recommends that you leave the pin unconnected.
ASDO	Output	Control signal from the Stratix III FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode, ASDO is not used. Also, when this pin is not used as an output, Altera recommends that you leave the pin unconnected.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix III device. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface.	

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and used when the CRC error detection circuit is enabled.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to ground.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to ground.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA0 is not used and this pin is not used as an I/O, Altera recommends that you leave this pin unconnected.
DATA[7..1]	I/O, Input	Dual-purpose configuration data input pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[7..1] are not used and these pins are not used as I/O, Altera recommends that you leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin that can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, Altera recommends that you connect this pin to ground.
<b>Differential I/O Pins</b>			
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used, they can be tied to GND.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used, they can be tied to GND.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers, but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used, they can be tied to GND.

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
<i>External Memory Interface Pins</i>			
DQS[1..44][T,B], DQS[1..40][L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.	When these I/O pins are not used, they can be tied to GND.
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.	When these I/O pins are not used, they can be tied to GND.
DQ[1..44][T,B], DQ[1..40][L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	When these I/O pins are not used, they can be tied to GND.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	When these I/O pins are not used, they can be tied to GND.
CQn[1..44][T,B], CQn[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	When these I/O pins are not used, they can be tied to GND.

**Altera provides these guidelines only as recommendations. It is your responsibility, as a designer, to apply simulation results to the design to verify proper device functionality.**

**Notes:**

(1) These pin connection guidelines are created based on the largest Stratix III device, EP3SL340.

(2) Capacitance values for the power supply should be selected after considering the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on the current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques, such as innerplaning capacitance with low inductance, should be considered for higher-frequency decoupling.

**Stratix® III Device Family Pin Connection Guidelines**  
**PCG-01004-1.2**

**Revision History**

<b>Revision</b>	<b>Description of Changes</b>	<b>Date</b>
1.0	Initial release	10/19/2007
1.1	Changed VCCPD[1..8][A,B,C] pin description and guidelines	4/9/2008
1.2	Changed VCCPGM, RUP[1..8]A, VCCL, VCC, VCCIO[1..8][A,B,C], PORSEL, and nIO_PULLUP connection guidelines. Divided CLK[0,2,4,5,6,7,9,11..15]p,n into separate CLK[0,2,9,11]p, CLK[0,2,9,11]n, CLK[4..7,12..15]p, CLK[4..7,12..15]n.	4/11/2008