

This application note describes the implementation of a deterministic latency PHY that complies with the Common Public Radio Interface (CPRI) protocol in Altera® Stratix® V and Arria® V devices with transceivers. It also describes the transceiver configuration and clocking scheme to achieve the deterministic latency functional mode.

This application note contains the following sections:

- “Introduction to the CPRI Specification” on page 1
- “Implementing Deterministic Latency for CPRI Interfaces” on page 3
- “Transceiver Support for CPRI Applications” on page 6
- “CPRI Enhancements in the Stratix V and Arria V Devices” on page 9
- “Backwards Compatibility” on page 10
- “6G Reference Design Example for Arria V GX” on page 10
- “Upcoming RE Design Example Features” on page 13
- “CPRI Channel Placement Restriction” on page 14

Introduction to the CPRI Specification

The CPRI specification defines the interface of radio base stations between the radio equipment controller (REC) and the radio equipment (RE). The physical layer supports both the electrical interface (for example, traditional radio base stations) and the optical interface (for example, radio base stations with remote radio head). The scope of the CPRI specification is restricted to the link interface only, which is basically a point-to-point interface. Such a link has all the features necessary to enable a simple and robust usage of any given REC and RE network topology, including a direct interconnection of multiport REs as shown in [Figure 1](#).

Figure 1 shows the different topologies for the REC and RE network.

Figure 1. Basic Configuration in CPRI Topologies

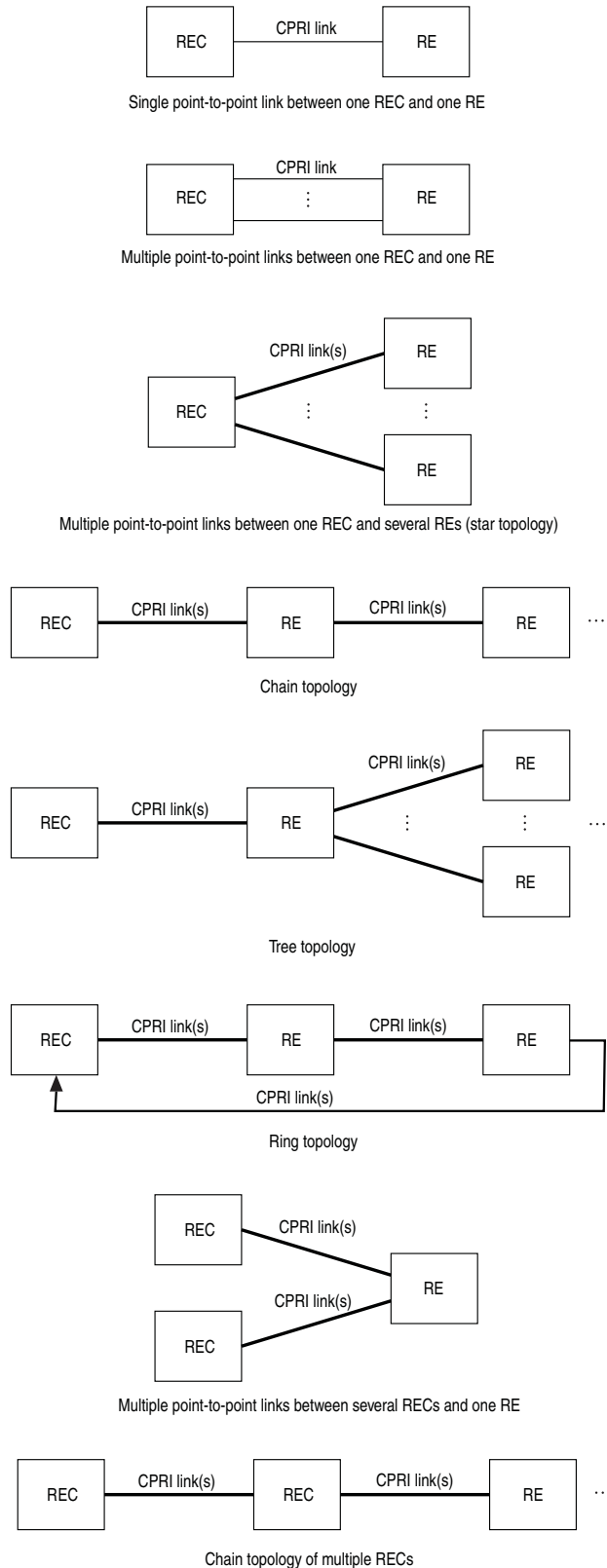
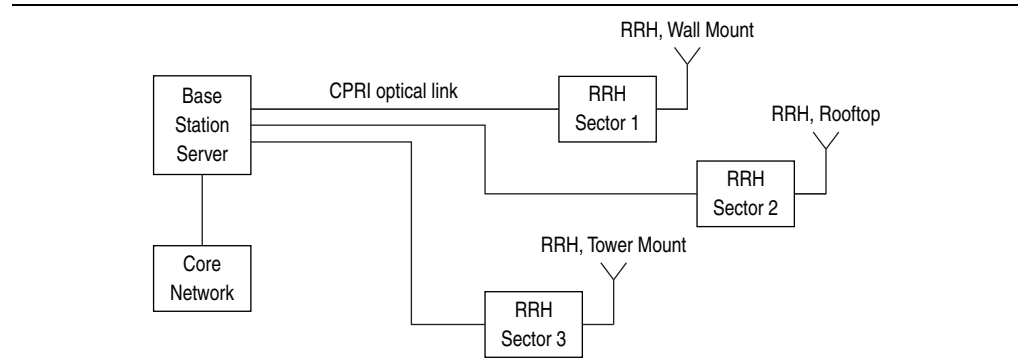


Figure 2 shows a distributed open base station architecture, which has evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the CPRI specification introduced standardized interfaces separating the base station server and the remote radio head (RRH) part of a base station by an optical fiber.

Figure 2 illustrates an example architecture where a 2G/3G/4G base station is connected to RRHs over optical fibers.

Figure 2. Example of a Distributed Open Base Station Architecture



CPRI can be used to carry the radio frequency (RF) data to the RRH in different sector cells. This architecture reduces costs for service providers because only the remote radio heads containing the RE need to be situated in environmentally challenging locations. The base stations can be centrally located in less challenging locations where footprint, climate, and availability of power are more easily managed.

 For more information about the CPRI specification, refer to [CPRI Specification V4.1](#).

Implementing Deterministic Latency for CPRI Interfaces

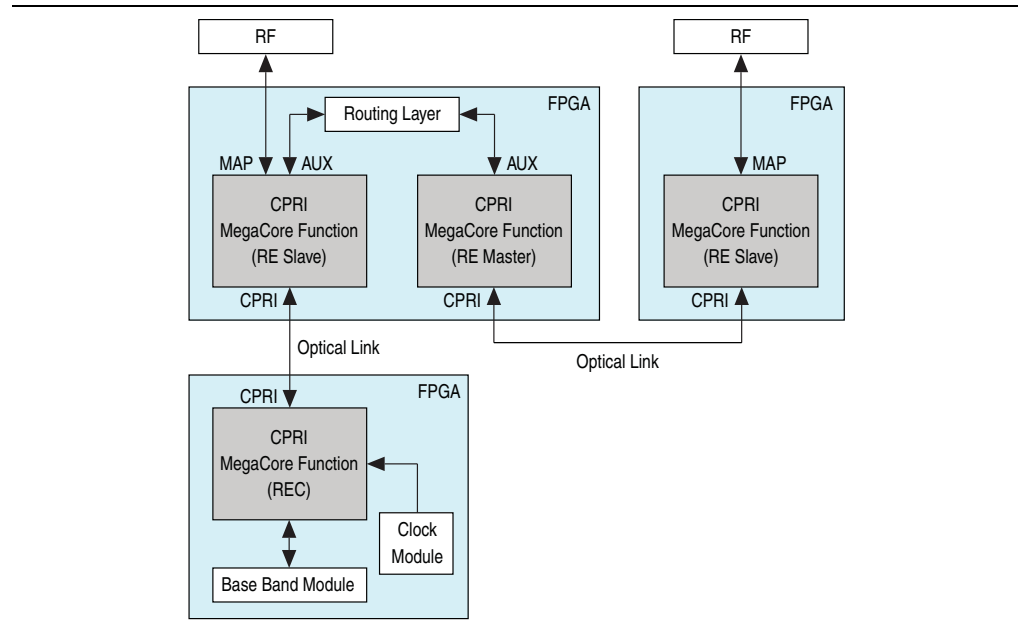
Deterministic Latency PHY IP core supports many industry-standard protocols that require deterministic latency, including the following protocols:

- CPRI
- Open Base Station Architecture Initiative (OBSAI)
- 1588 Ethernet
- Custom Deterministic Latency protocols

For the Quartus® II software version 11.1, this feature only supports CPRI protocol in the Stratix V and Arria V devices.

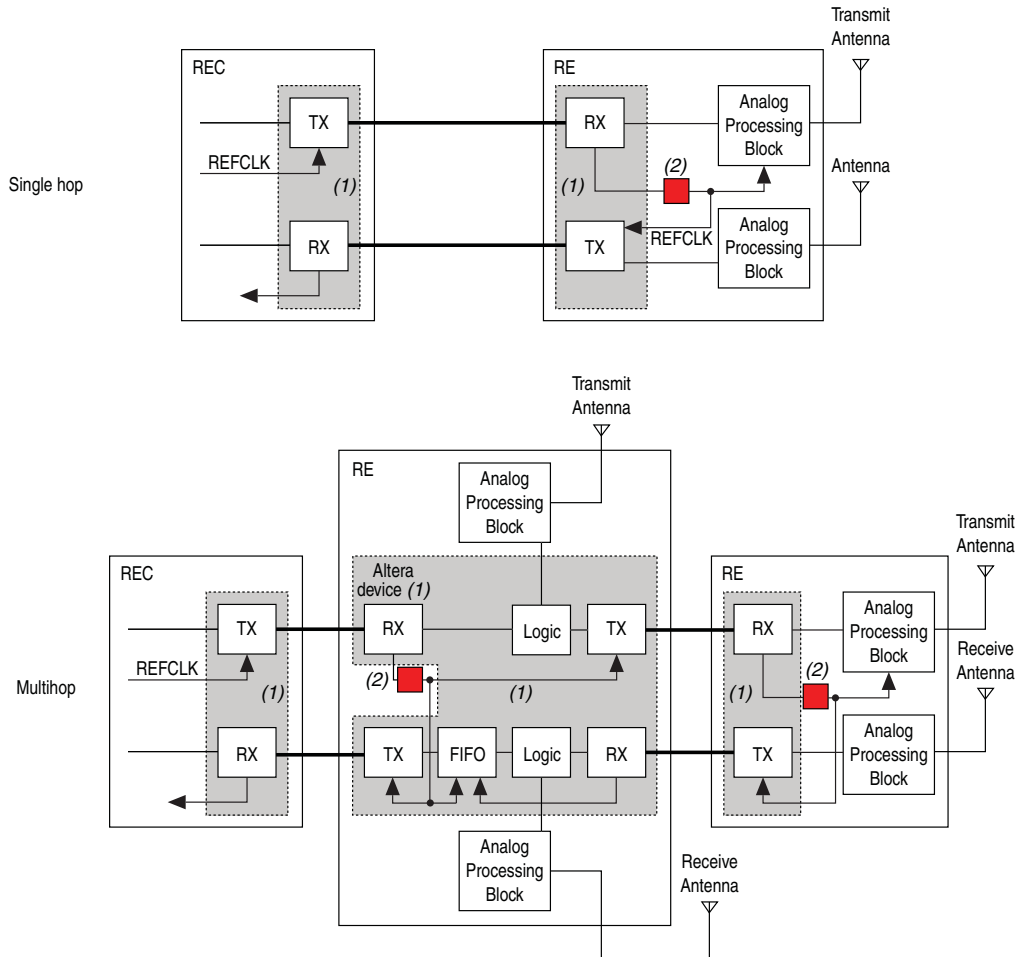
CPRI interface is a high-speed serial interface developed for the cellular phone network REC to uplink and downlink data from available remote RE. Figure 3 shows the structure of a typical CPRI application on devices.

Figure 3. Typical CPRI Application on Devices



With high bandwidth, data can be uplinked or downlinked from multiple antennas. Multiple REs can be chained to a single REC (multihop). Figure 4 shows the single hop and multihop connections.

Figure 4. Single Hop and Multihop Connections



Notes to Figure 4:

- (1) Arria V FPGA
- (2) External cleanup PLL

To avoid transmission interference in time division multiplexed systems, every radio in a cell network requires accurate delay estimates with minimal delay uncertainty. Otherwise, transmission interference can occur in systems such as time-division multiple-access (TDMA), global system for mobile communications (GSM), or code division multiple access (CDMA), in which multiple radios share a common frequency. Lower delay uncertainty is always desired for increased spectrum usage efficiency and bandwidth. The Stratix V and Arria V devices are designed with features to minimize the delay uncertainty for both RECs and REs.

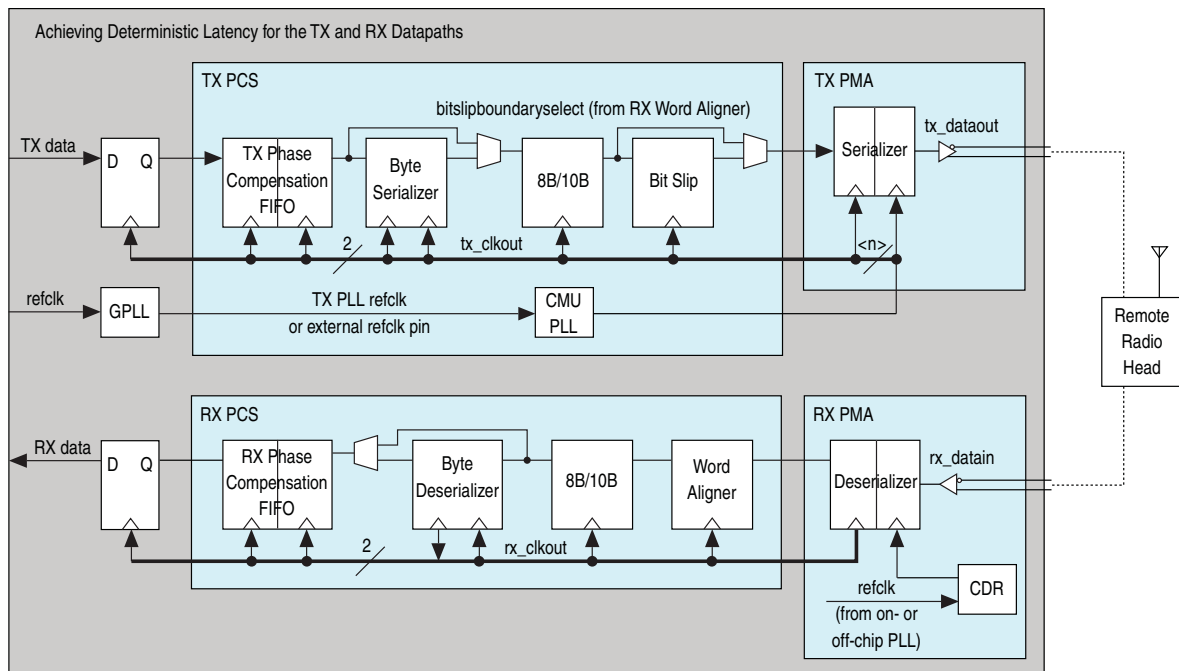
Transceiver Support for CPRI Applications

Clause 3.6.2 of the CPRI specification requires the round-trip delay measurement accuracy, excluding the cable, to be within ± 16.276 ns for single hop and multihop connections. In multihop connections, the allowed delay uncertainty is accumulated over the number of hops in the connection.

The Stratix V, Arria V GT, and Arria V GX devices include embedded transceivers with deterministic latency features that easily meet the delay accuracy requirements of the CPRI specification. The deterministic latency features enable you to accurately compute the transceiver datapath latencies when using the CPRI standardized interfaces.

Figure 5 shows an example of the REC datapaths with the Stratix V or Arria V transceiver.

Figure 5. Typical REC Block Diagram



For more information about the supported data rates for CPRI implementation using transceivers in the Stratix V, Arria V GT, and Arria V GX devices, refer to [Table 1 on page 9](#).

TX and RX Phase Compensation FIFO Buffers

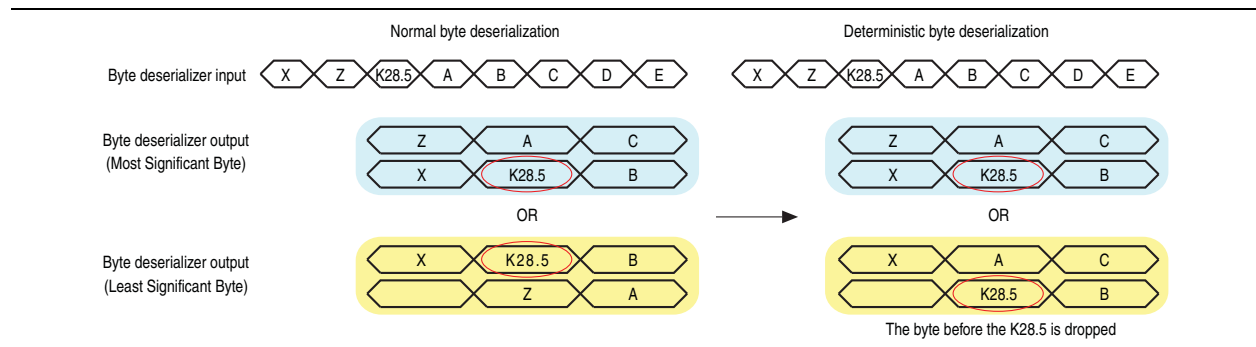
The transmit (TX) and receive (RX) phase compensation FIFO buffers are always in register mode. In this mode, the write clocks for these FIFO buffers are not used. The latency of the phase compensation FIFO buffers is one clock cycle when the FIFO buffers are in register mode.

Byte Serializer and Byte Deserializer

The byte serializer and byte deserializer support /1 (bypass) and /2 serialization and deserialization. Compared to Stratix IV, the new feature on deterministic /2 deserializer ensures the word alignment pattern, which is K28.5 (0011111010) for CPRI protocol, is always placed in the least significant byte (LSB) with fixed latency of three cycles. This feature is enabled automatically by the deterministic latency state machine and does not require the user logic to check on the K28.5 position in the byte deserialized data for actual latency.

Figure 6 shows the location of the word alignment pattern for normal and deterministic byte deserialization.

Figure 6. Normal and Deterministic Byte Deserialization



For more information about the clock adjustment for deterministic latency, refer to “6G Reference Design Example for Arria V GX” on page 10.

8B/10B Encoder and Decoder

For Deterministic Latency PHY IP, the Quartus II software version 11.1 only supports the transceiver configuration with 8B/10B encoder and decoder enabled.


Word Aligner

The word aligner supports both auto-alignment mode (manual alignment in ALTGX and GUI) and deterministic latency state machine. The word aligner for both modes automatically performs an initial alignment to the specified word pattern after the deassertion of reset. After the initial alignment, the rx_enapatternalign signal is asserted to initiate another pattern alignment. The second alignment is needed only when the data is corrupted in the middle of the process or when realignment is required. For the deterministic latency state machine, extra shifting may occur in the RX datapath if the rx_enablepatternalign signal is asserted when bit slipping is partially done. The rx_enablepatternalign signal should only be asserted under the following conditions:

- The rx_syncstatus signal is asserted, or
- The rx_bitslipboundaryselectout signal changes from a non-zero value to zero. Monitor the value for the rx_bitslipboundaryselectout signal when the rx_syncstatus signal stays at a low value.

For physical medium attachment (PMA) single width (3G mode), the `rx_enablepatternalign` signal is always kept high. The `rx_syncstatus` signal only toggles high for one clock cycle when a new word boundary is found.

In auto-alignment mode, the word aligner searches for a specific character, which is K28.5 (0011111010) for CPRI protocol, in the data-stream and aligns the special character against the data stream. When the word aligner detects the correct pattern, it generates a signal to the barrel shifter and rotates the data by N bits to properly align the words. The rotated and aligned data is then sent to the physical coding sublayer (PCS). The RX word aligner can generate the number of bits slipped on its `bitslipboundaryselectout [4:0]` output. In 3G (10-bit) mode, the output is the number of bits slipped. If no bits were slipped, the output is 0. In 6G (20-bit) mode, the output is 19 minus the number of bits slipped. If no bits were slipped, the output is 19. Before alignment is achieved, the output is 15 (5'b01111) in 3G mode and 31 (5'b11111) in 6G mode.

 For more information about the word alignment pattern, refer to the simulation waveform in the reference design examples.

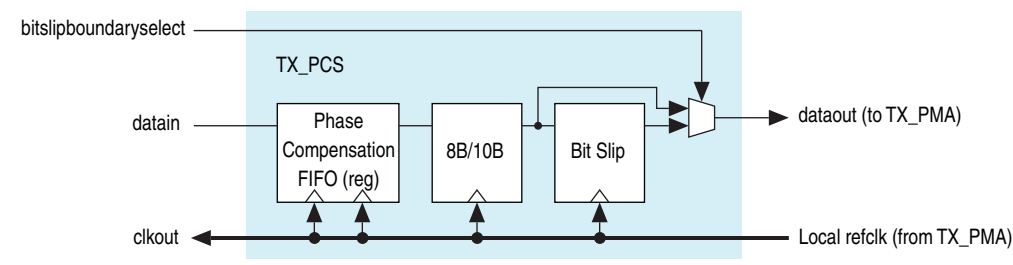
TX Bit Slipper

In the CPRI specification, fixed latency is required regardless of the number of resets. To support this requirement, the receiver path uses the RX bit slipper to determine the number of bits it has to slip to achieve the word alignment.

This feature is enabled when the word aligner is in auto-alignment mode. When this feature is enabled, set the `BITSLIP_ENABLE` parameter to `TRUE` and the `bitslipboundaryselect [4:0]` input to the number of bits to slip (0 to 9 in 3G 10-bit mode, or 0 to 19 in 6G 20-bit mode).

Figure 7 shows the architecture of the TX bit slipper.

Figure 7. TX Bit Slipper



Data Rate Support

PLL sharing is possible for an individual channel with its own local divider. Two PLLs are needed to support 0.6144x (614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps, 4.9152 Gbps, and 9.8304 Gbps) and 3.072x (3.072 Gbps and 6.144 Gbps) data rates with clock divider value 8 (for data rates from 614.4 Mbps to 4.9152 Gbps) and clock divider value 1, 2, or 4 (for the rest of the data rates). The Quartus II software version 11.1 supports up to 6.144 Gbps for a maximum of 4 channels per bank in the Stratix V and Arria V devices. For a single channel, one PLL is sufficient. Auto rate negotiation can be set in a PLL reconfiguration.

Table 1 lists sample channel width options and CPRI data rates in the deterministic latency mode.

Table 1. Sample Channel Width Options for Supported Serial Data Rates

Serial Data Rate (Mbps)	Channel Width (FPGA-PCS Fabric)			
	Single Width		Double Width	
	8-Bit	16-Bit	16-Bit	32-Bit
614.4	✓	✓	—	—
1228.8	✓	✓	✓	✓
2457.6	—	✓	✓	✓
3072	—	✓ ⁽¹⁾	✓ ⁽¹⁾	✓
4915.2	—	—	—	✓ ⁽¹⁾
6144	—	—	—	✓ ⁽¹⁾

Note to Table 1:

(1) Applicable to C4, C5, and I5 speed grades only.

CPRI Enhancements in the Stratix V and Arria V Devices

Enhancements in the Stratix V and Arria V transceivers over the Stratix IV transceivers support the deterministic latency requirements in the CPRI specification. The following list describes the enhancements:

- Enhancement on the PCS block to support 9.8304 Gbps, which is a higher data rate introduced in CPRI specification version 4.2.
- New feature for deterministic /2 deserialization, in which the byte deserializer ensures the word alignment pattern is always placed in the least significant byte (LSB) with a fixed latency of three cycles.
- Deterministic latency state machine in the word aligner reduces the known delay variation from the word alignment process and automatically synchronizes and aligns the word boundary by slipping a clock cycle in the deserializer. When the RX word aligner receives an incoming signal, it detects the word alignment pattern (K28.5) and identifies the word boundary. Certain number of bits may be slipped to achieve the word alignment. The word aligner sends an instruction signal to the PMA deserializer to synchronize and align the boundary by slipping a clock cycle. At every rising edge of the incoming signal, the rx_clkslip signal instructs the PMA deserializer to slip one bit in the serial domain. When the PCS finishes toggling the rx_clkslip signal, the PCS expects the PMA to slip the serial clock by a requested number of times and align the data successfully. This feature supports both single width and double width data, and allows fixed latency on the RX path without relying on the latency compensation using TX bit slipper on the TX path. User logic is not required to manipulate the TX bit slipper for constant round-trip delay, or monitor the bitslipboundaryselectout to know the single direction delay between the base station and the antenna. In manual mode, the TX bit slipper is able to compensate one unit interval (UI) of uncertainty.

Figure 8 shows the deterministic latency state machine.

Figure 8. Deterministic Latency State Machine in Word Aligner

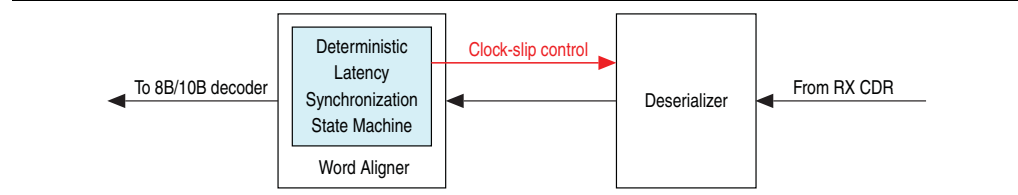


Table 2 describes the existing and new methods to achieve the deterministic latency mode in the Stratix V and Arria V devices.

Table 2. Methods to Achieve Deterministic Latency Mode in the Stratix V and Arria V Devices

Existing Feature ⁽¹⁾		New Feature ⁽²⁾	
Description	Requirement	Description	Requirement
Manual alignment with bit position indicator provides deterministic latency. Delay variation up to 1 parallel clock cycle.	Extra user logic to manipulate the TX bit slipper with a bit position indicator from the word aligner for constant total round-trip delay. ⁽³⁾	Deterministic latency state machine alignment reduces the known delay variation in word alignment operation.	None.
K28.5 position varies in byte deserialized data. Delay variation up to ½ parallel clock cycle.	Extra user logic to manually check the K28.5 position in byte deserialized data for actual latency. ⁽³⁾	K28.5 is always placed in the least significant byte position in byte deserialized data. The clock is adjusted to provide constant latency.	None.

Notes to Table 2:

- (1) Backward compatible with CPRI designs in the Stratix V and Arria II devices.
- (2) New deterministic latency feature in the Arria II devices.
- (3) For more information about user logic requirements and local clock routing that are applicable to the `tx_clkout` and `rx_clkout` paths, refer to *AN610: Implementing Deterministic Latency for CPRI and OBSAI Protocols in Altera Devices*.


 For more information about deterministic latency, refer to the *Deterministic Latency PHY IP Core* chapter in the *Altera Transceiver PHY IP Core User Guide*.


Backwards Compatibility

This PHY IP is not directly backward compatible with ALTGX variants because of the significant change in standard interfaces. The PHY IP bonded-mode configuration is not supported for the CPRI protocol.

6G Reference Design Example for Arria V GX

This section describes the design example at the transceiver level in RE for the Arria V GX devices.

 The design example is only for transceiver level simulation without any CPRI IP involvement.

 Altera offers a complete easy-to-use IP core for building CPRI specification version 4.1 and lower interfaces to speed development time. CPRI Specification version 4.2 will be supported by the IP core in the future release of the Quartus II software.

 For more information about the Altera CPRI IP solution, refer to the [Altera CPRI IP](#).

Design Example in ModelSim or Other Simulation Tool

To run the test for the design example in ModelSim or other simulation tools, follow these steps:

1. Open and restore the **.qar** archived file in the Quartus II software version 11.1 with the RE design example file: **av_6g_cpri_re_ref_design_timing_closed.qar**.
2. On the Tools menu, click **MegaWizard Plug-in Manager**. Select **Edit an existing custom megafunction variation** and enter the existing megafunctions – Deterministic Latency PHY IP Core (**top_cpri_tx.v** and **top_cpri_rx.v**) and Transceiver Reconfiguration Controller. Click **Finish** to regenerate all of the available megafunctions in the project (2 megafunctions for RE) to provide the necessary simulation files from the Quartus II software to the subsequent ModelSim simulation.

You now have all the necessary files to start with the simulation.

3. Open ModelSim-Altera version 6.6 (version 6.5 or below is not supported for this simulation) or another tool and locate the restored project in your directory.
4. For ModelSim, type the following command at the transcript panel to initialize the simulation:

```
do top_simulation_script_full_compilation.tcl
```

This script is only needed for the first time to compile a full simulation that generates all the necessary simulation files in ModelSim.

If no changes are made to the megafunctions, you can reduce the simulation duration with the following script:

```
do top_simulation_script_reduced_compilation_time.tcl
```

5. When the simulation is completed, you are able to see the waveforms from the simulation result.


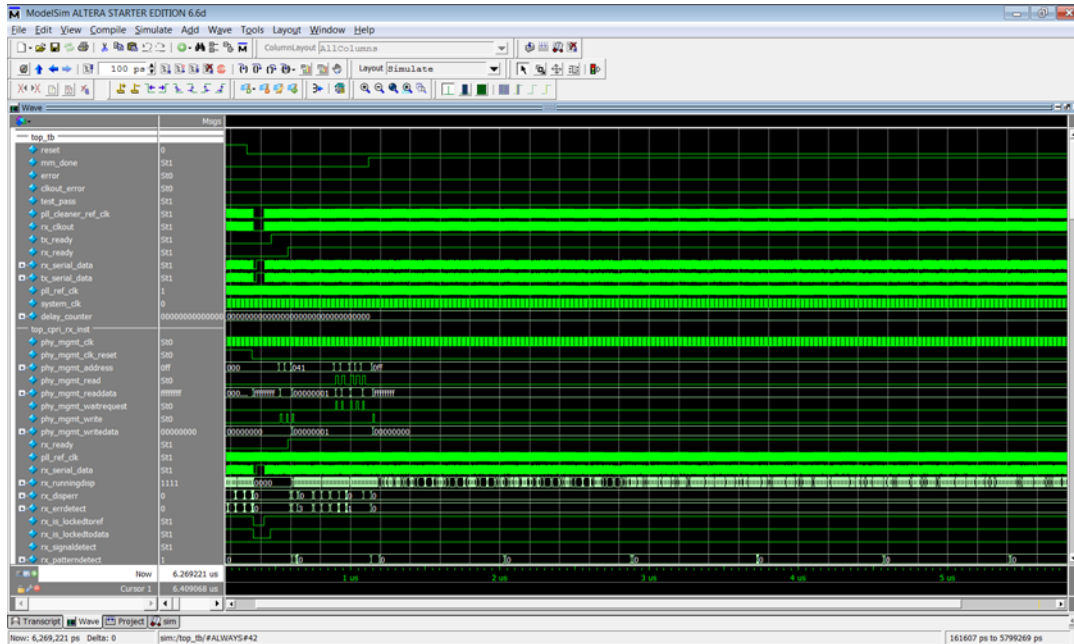
 The waveforms shown are meant for functional simulation only.

Figure 9 shows the RE simulation result.

Figure 9. RE Simulation Result



RE Design Example

The following list describes the test bench structure for RE:

- **reset**—This instance manages the reset sequence of the Avalon® Memory Mapped (Avalon-MM) interface instance (**mgmt_master**). This instance generates a 300 ns pulse to kick-start the transceiver operation.
- **mgmt_master**—This instance is the master control of the Avalon-MM interface of the transceiver PHY. The read and write transactions to test the transceiver PHY are to reset the TX path and the RX path and read whether the `pma_tx_pll`, `rx_is_lockedtohref`, and `rx_is_lockedtodata` status signals are asserted before the `rx_syncstatus` signal.
- **latency count**—The simulation method for calculating the deterministic latency (fixed or known latency) at transceiver level. This instance is useful to determine the latency, especially in hardware design verification tests.
- **cpri_src**—This instance generates one CPRI data frame and four frames of PRBS7 patterns to the 32-bit `tx_parallel` data input of the deterministic latency PHY instance.
- **cpri_6g_tx**—The deterministic latency PHY generated by the MegaWizard Plug-in Manager for the transmitter in RE configurations.
- **cpri_6g_rx**—The deterministic latency PHY generated by the MegaWizard Plug-in Manager for the receiver in RE configurations.

- **frequency_checker**—This instance consists of two frequency checkers that verify the frequency precision of the tx_clkout and rx_clkout PLL clocks. It can be the frequency ppm threshold detector for validation purposes. The recovered clock runs at 153.6 MHz (6.144 Gbps divided by 40 bits) and takes a larger sample size to meet the frequency ppm threshold tolerance.
- **rxstatus_checker**—This instance checks the correctness of the receiver status signals, such as the rx_syncstatus, rx_patterndetect, rx_disperr, and rx_errdetect signals.
- **cpri_sink**—This instance is a frame checker to verify the correctness of the received data, which consists of one CPRI data frame and four frames of PRBS7 patterns.

To perform the test for RE, follow these steps:

1. Start a test bench examination of the transceiver basic functionality and status with the Avalon-MM interface tests.
2. Perform the frequency verification tests for the tx_clkout and rx_clkout PLL clocks. The clkout_error signal is the indicator for the violation of the frequency ppm tolerance. As for RE applications, such as remote radio head, the PLL output clock, rx_clkout is connected to the external PLL cleaner and feedback to the input reference clock of the transmitter.
3. Monitor the receiver status signals.
4. After the rx_syncstatus signal indicates that the synchronization of the word aligner pattern is asserted, the CPRI data frame and four frames of PRBS7 patterns are verified at the received data. If no error is observed for both the status signals and the received data for about 7.587 us throughout the simulation duration, a pass status is asserted to indicate the success of the verification process.



For more information about the Avalon-MM interface with Deterministic Latency PHY IP core and detailed parameter settings in the MegaWizard, refer to the *Deterministic Latency PHY IP Core* chapter in the *Altera Transceiver PHY IP Core User Guide*.



For more information about Avalon-MM interface, refer to *Altera Avalon Memory-Mapped Interface Specification*.

Upcoming RE Design Example Features

The following list describes the upcoming features for RE:

- 9.8304 Gbps CPRI protocol support in the Arria V GT devices.
- Dynamic reconfiguration support in auto speed negotiation and redundancy in topologies network.
- TX phase lock loop (PLL) feedback

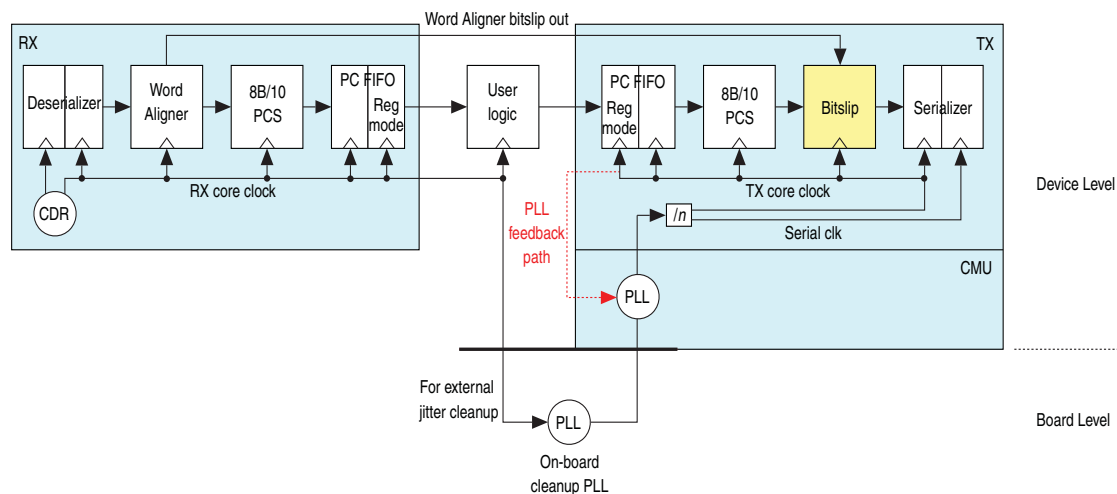
TX PLL Feedback

To ensure low skew clock fan-out for both `tx_clkout` and `rx_clkout` routing to clock networks, such as global clock (GCLK) and region clock (RCLK), follow one of these methods:

- Utilize the feedback PLL path to align the phase of the TX core clock to be the same phase as the input clock source to the TX PLL. In [Figure 10](#), the input clock source is the RX core clock.
- Measure the phase difference with a FIFO buffer that uses some sampling techniques.
- Feed CPRI system with recovered clock to the TX PLL input directly, as shown in [Figure 10](#).

[Figure 10](#) shows a CPRI system without the byte serializer and byte deserializer. It is optional to add the byte serializer and byte deserializer to the CPRI system.

Figure 10. CPRI System with Recovered Clock Feeding Directly to the TX PLL Input



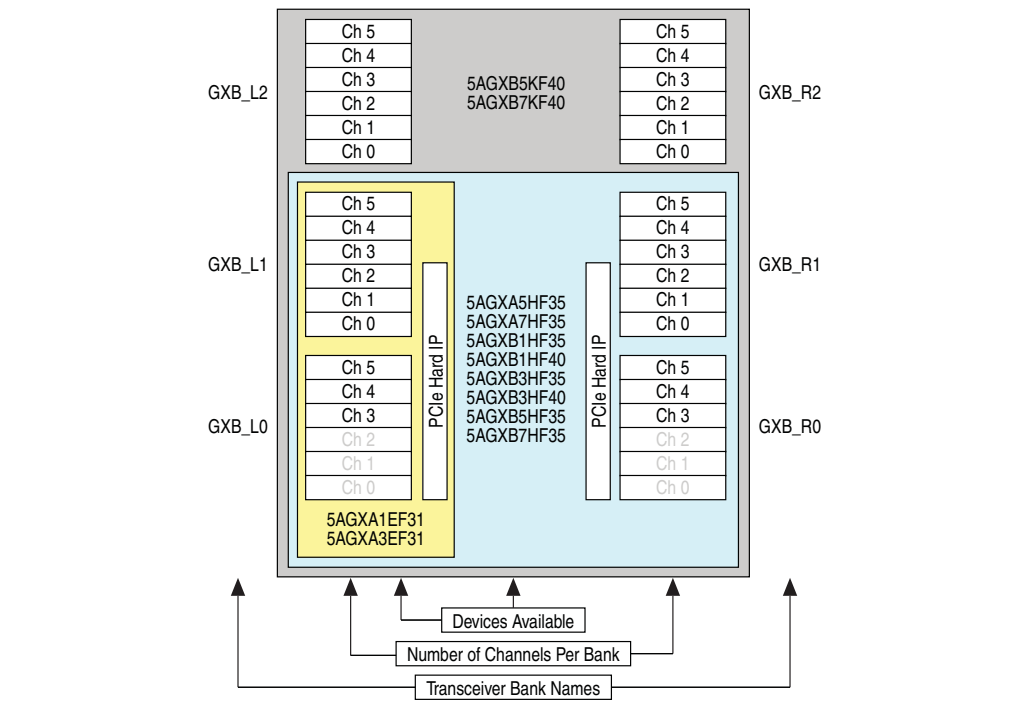
 For suggestions about features supported in a CPRI PHY design example, file a service request at <https://mysupport.altera.com/>.

CPRI Channel Placement Restriction

The Quartus II software version 11.1 has a restriction on channel placement for Deterministic Latency PHY IP Core. Channel placement can be in any location except the lowest 3 channels, which are Ch 0, Ch 1, and Ch 2 in the GXB_L0 and GXB_R0 transceiver banks.

Figure 11 shows the channel placement restriction for Deterministic Latency PHY IP Core.

Figure 11. Channel Placement Restriction for CPRI Specification in the Arria V Devices



Document Revision History

Table 3 lists the revision history for this document.

Table 3. Document Revision History

Date	Version	Changes
January 2012	1.0	Initial release.

