AN 578: Manual Placement of CMU PLLs and ATX PLLs in Stratix IV GX and GT Devices

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Introduction

This application note describes the steps involved in the manual placement of CMU phase-locked loops (PLLs) and ATX PLLs in Altera's Stratix® IV GX and GT FPGAs. Altera's Quartus® II software automatically places the CMU PLLs and ATX PLLs by default.

The default placement of CMU PLLs by the Quartus II software may not be optimum for all bonded configurations, except for the PCI Express (PIPE) ×8 bonded configuration and the Basic ×8 bonded configuration. Check the default placement to decide if it is optimum for skew requirements in your Basic (PMA Direct) ×N bonded design. If it is not, manual placement of the CMU PLLs is recommended.

The default placement of ATX PLLs by the Quartus II software is performed arbitrarily for all bonded configurations, except for the PCI Express (PIPE) ×8 bonded configuration. Check the default placement to decide if it is optimum for skew requirements in your design. If it is not, manual placement of the ATX PLLs is recommended.

This application note uses the Basic (PMA Direct) xN bonded configuration as an example scenario, where skew is a critical parameter and is dependent on the location of the transmitter PLL (CMU PLL or ATX PLL).

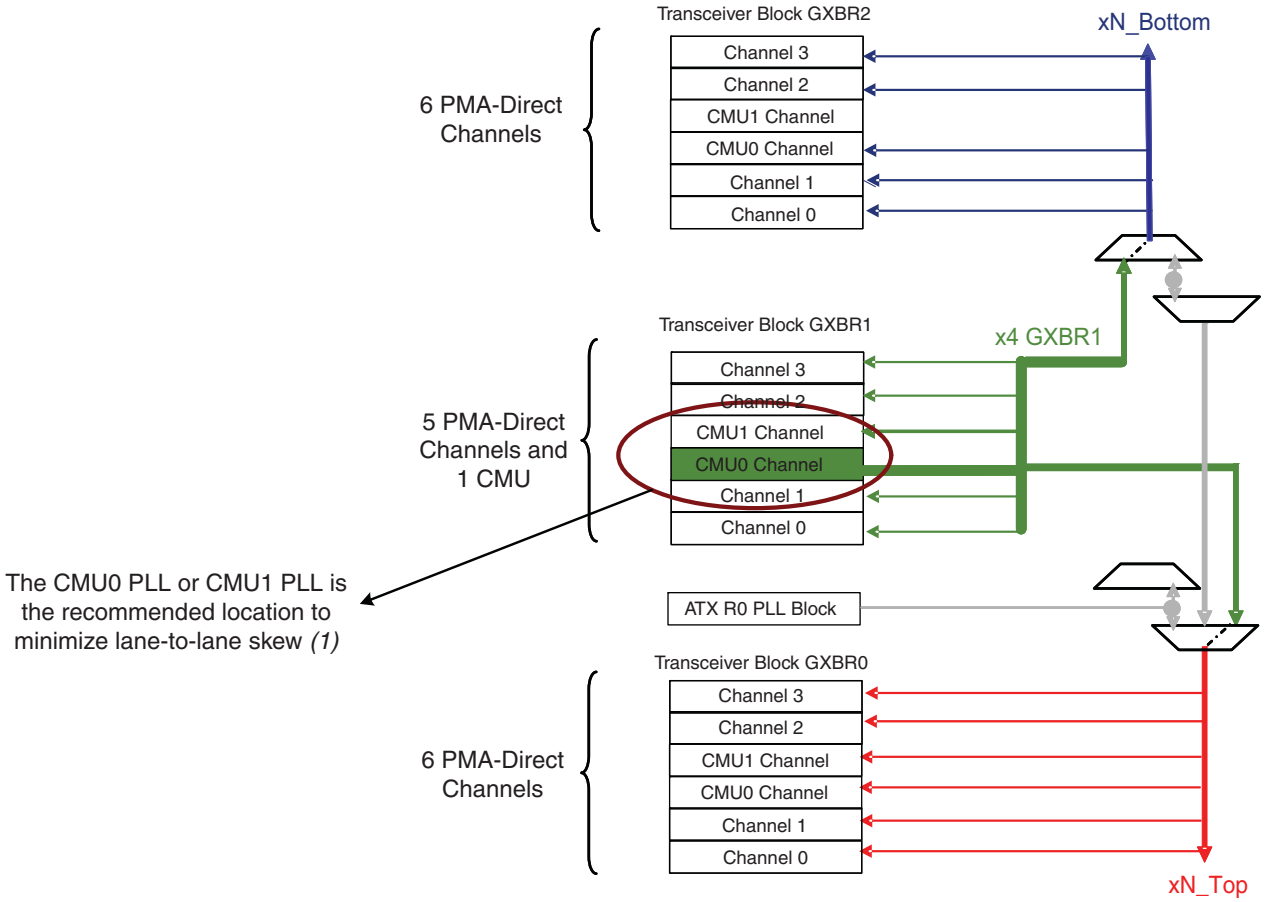
Example Scenario of Transmitter PLL Placement in Basic (PMA Direct) ×N Bonded Configurations

The following sections explain the CMU PLL and ATX PLL placement requirements in the Basic (PMA Direct) xN configuration.

CMU PLL Placement Requirement

To understand how the CMU PLL placement requirements achieve low lane-to-lane skew, consider a Stratix IV GX device with three transceiver blocks on each side. Figure 1 shows the CMU0 PLL of the middle transceiver block supplying transceiver clocks to all of the bonded channels.

Figure 1. CMU PLL Placement Requirement in a Basic (PMA Direct) xN Configuration *(Note 2)*



Notes to Figure 1:

(1) Even though both the CMU0 PLL and CMU1 PLL are the recommended locations to minimize lane-to-lane skew, the design example depicted in Figure 1 uses CMU0 PLL to generate the transceiver clocks for all the bonded channels.

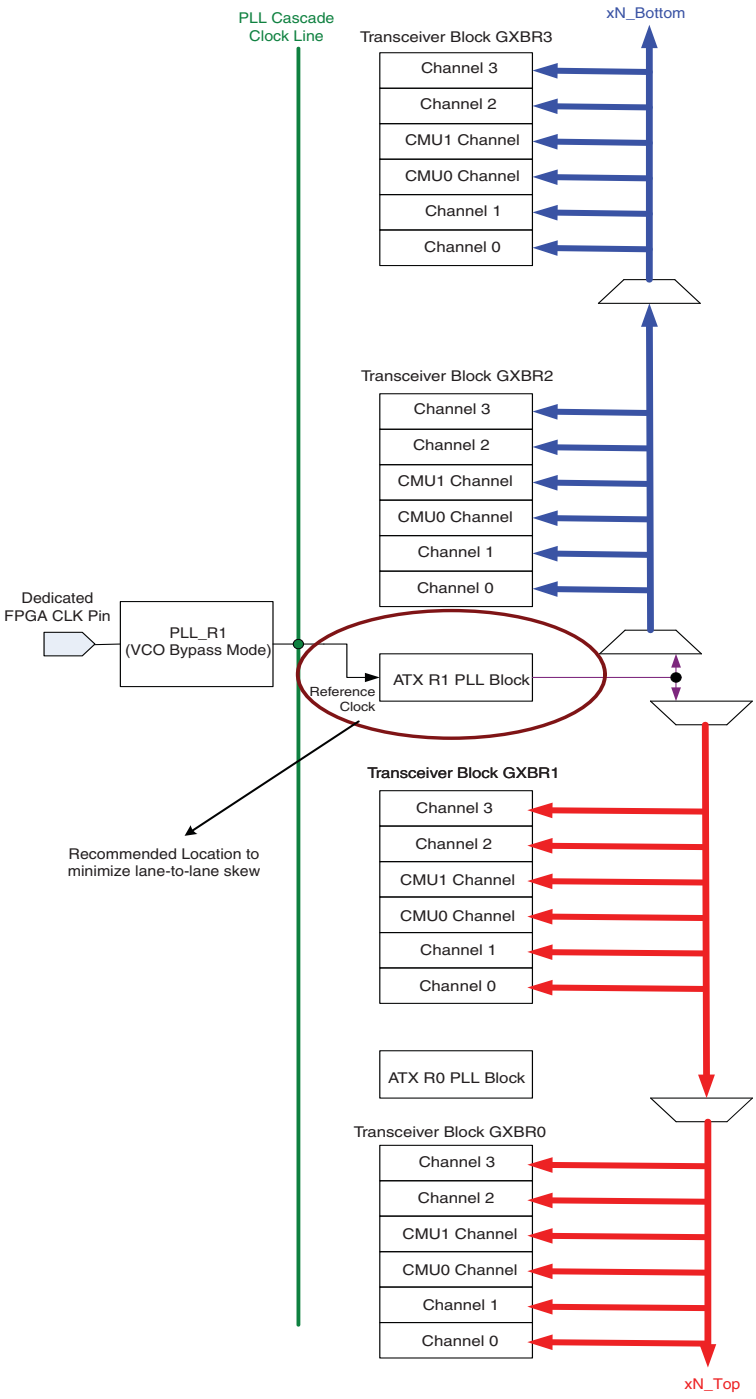
(2) Figure 1 shows a Stratix IV GX FPGA with three transceiver blocks on each side.

The equal-clock network skew introduced by the clock multiplexer in both directions leads to low lane-lane skew. Check the placement of the CMU PLL and if needed, manually place the transmitter PLL in the middle transceiver block (GXBR1) to minimize the lane-to-lane skew. Both "Method 1—Using the X and Y Coordinates" on page 4 and "Method 2—Using the IOBANK Information" on page 10 are applicable for the manual placement of CMU PLLs.

ATX PLL Placement Requirement

To understand the ATX PLL placement requirements needed to achieve low lane-to-lane skew, consider a Stratix IV GX device with four transceiver blocks on each side. Figure 2 shows the ATX PLL between GXBR1 and GXBR2, which supplies the transceiver clocks to all the bonded channels, in a Basic (PMA Direct) ×N configuration with 24 bonded channels (side-wide bonding).

Figure 2. ATX PLL Placement Requirement in a Basic (PMA Direct) xN Configuration where 24 Channels (Side-Wide Bonding) Are Bonded *(Note 1)*



Note to Figure 2:

(1) Figure 2 shows a Stratix IV GX FPGA with four transceiver blocks on each side.

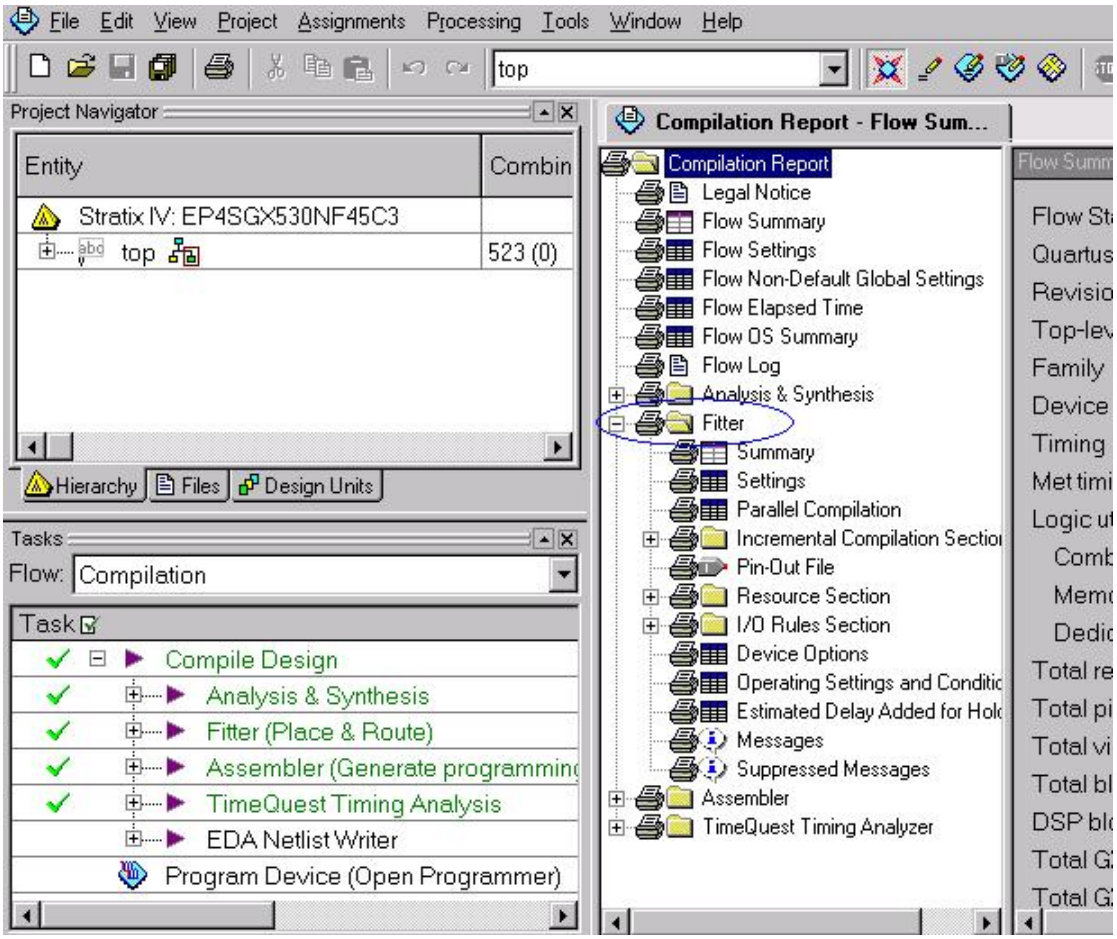
The equal-clock network skew introduced by the clock multiplexer in both directions leads to low lane-lane skew. Check the default assignment made by the Quartus II software. If this is optimum for the skew specifications in your design, manual placement of the ATX PLL is not required. Otherwise, it is recommended to manually place the ATX PLL between GXBR1 and GXBR2 to minimize the lane-to-lane skew. Method 1 discusses the steps involved in the manual placement of ATX PLLs.

Method 1—Using the X and Y Coordinates

This method is applicable to the manual placement of both CMU PLLs and ATX PLLs, in both Stratix IV GX and GT devices.

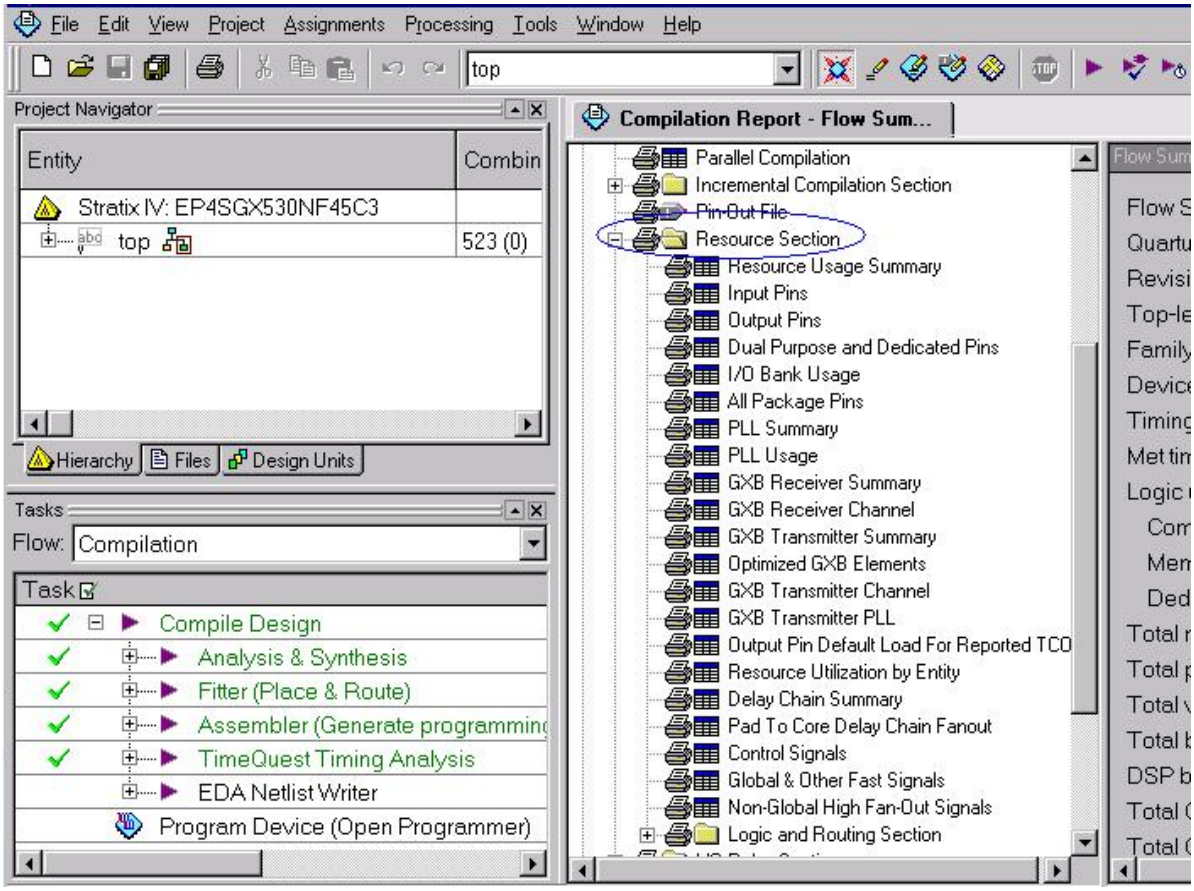
1. Select the **Fitter** option in the **Compilation Report** as shown in Figure 3.

Figure 3. Fitter Option in the Compilation Report



2. Select the **Resource Section** from the **Fitter** options as shown in Figure 4.

Figure 4. Resource Section Option in the Compilation Report

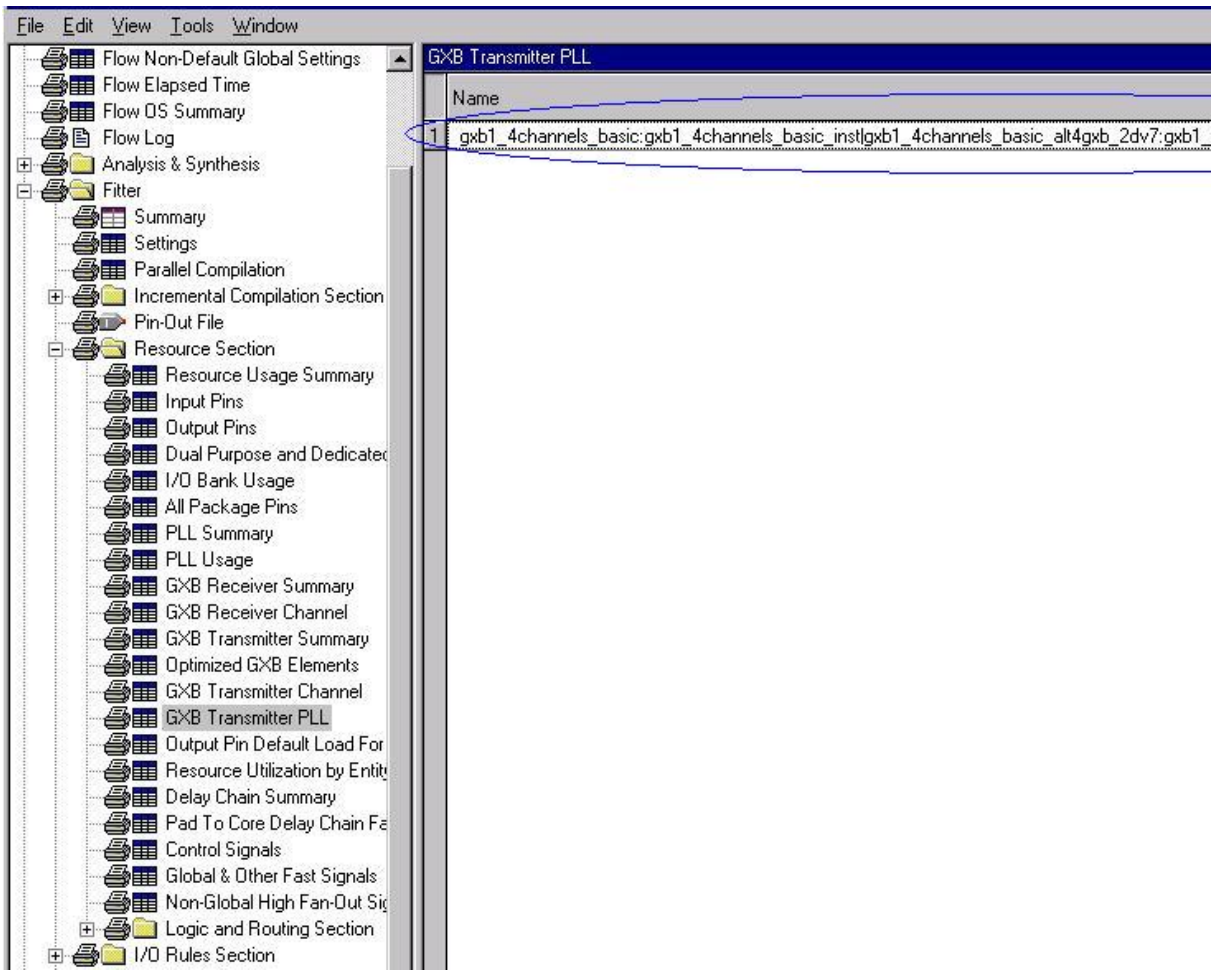


3. Select the **GXB Transmitter PLL** from the **Resource Section** options as shown in Figure 5.

   A typical design may contain multiple transmitter PLLs. The **Compilation Report** shows the transmitter PLL node information for each of the transmitter PLLs used in the design. Select the node associated with the appropriate transmitter PLL (based on the instance name relevant to the bonded configuration). Write down this node information and use it as described in this method (Step 7).

   Figure 5 shows an example scenario where the design contains a single transmitter PLL.

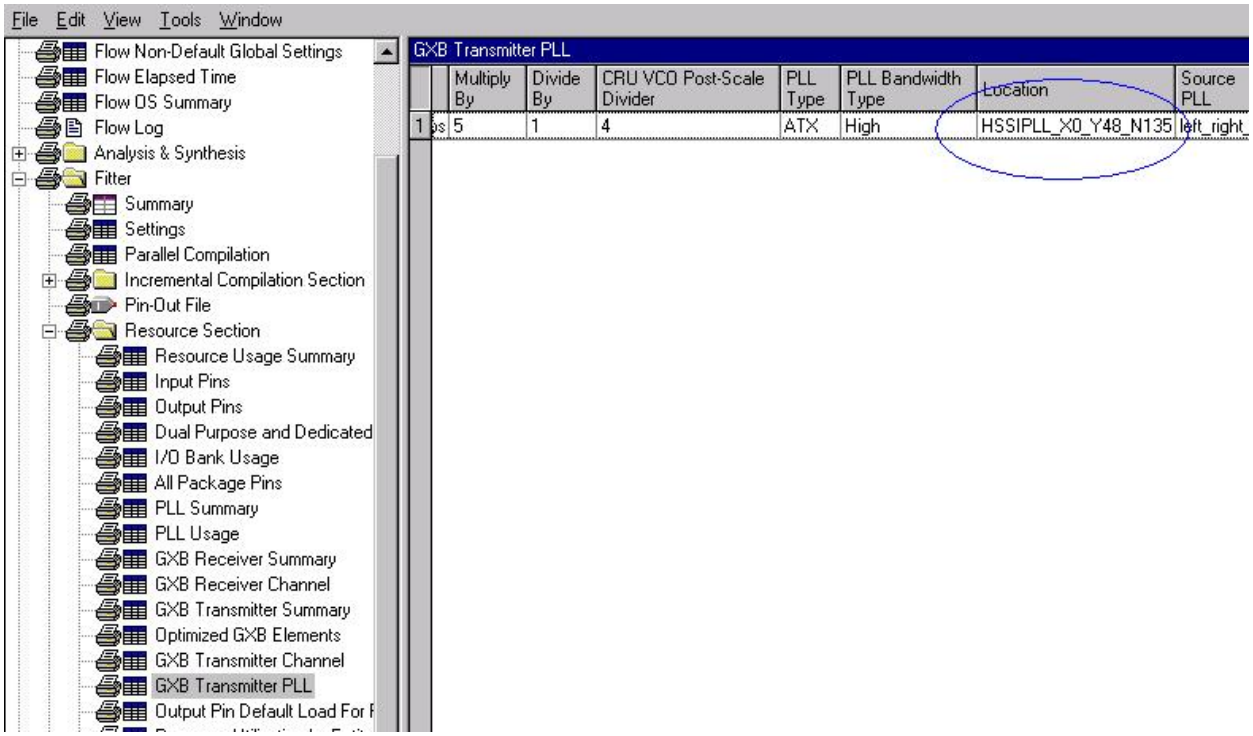
Figure 5. GXB Transmitter PLL Node Information in the Compilation Report



4. In the **GXB Transmitter PLL** option, observe the transmitter PLL type and write down the location assigned to the transmitter PLL node by the Quartus II software by default. The transmitter PLL location is described using X and Y coordinates.

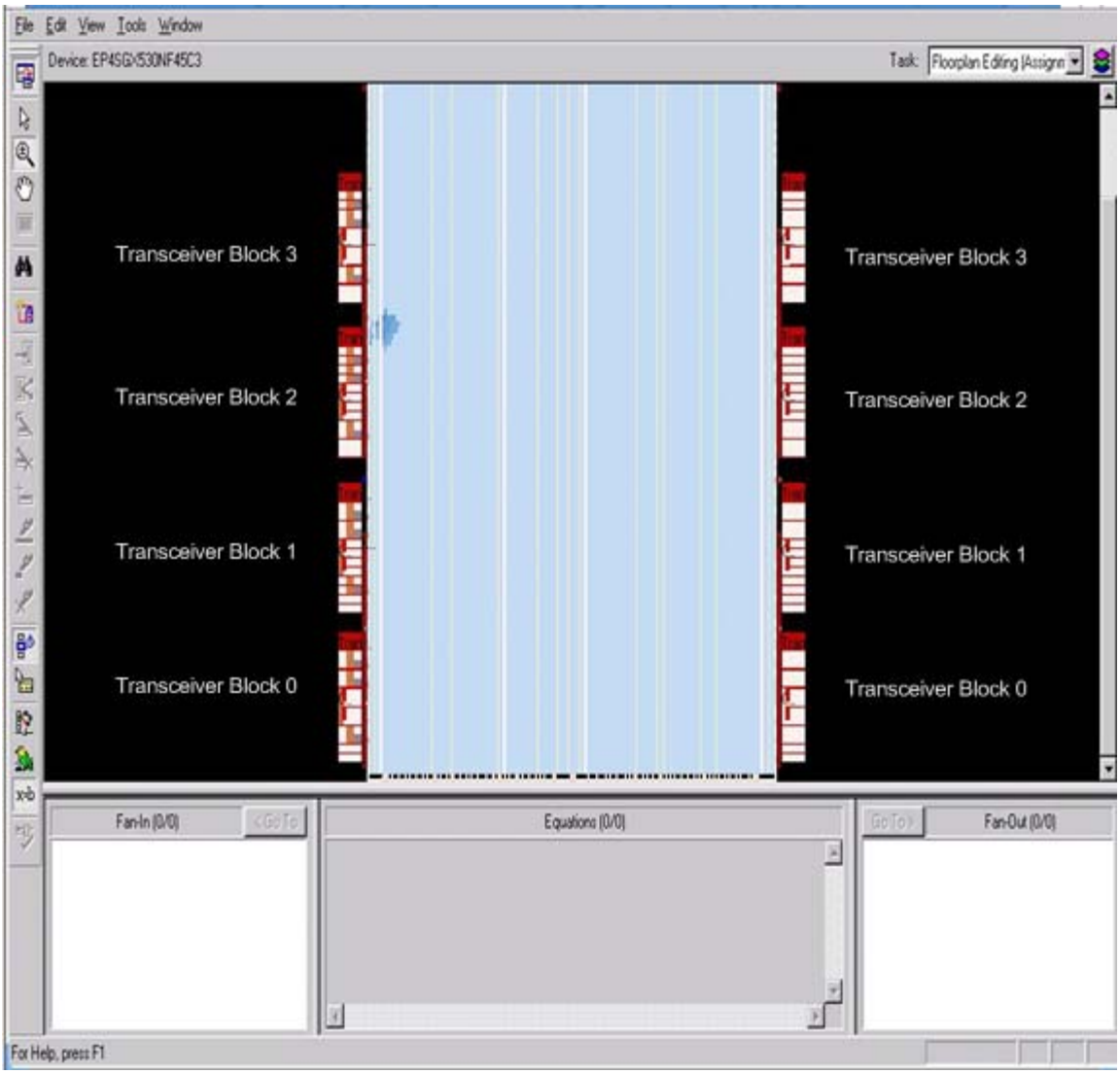
   You will need the transmitter PLL location to determine if the default placement is optimum for your design. You can determine this by checking the transmitter PLL location in the Chip Planner. Step 5 and Step 6 of this method explain how to view the location of a transmitter PLL in the Chip Planner. Figure 6 shows an example of the transmitter PLL location information in the compilation report.

Figure 6. Transmitter PLL Location Information in the Compilation Report



5. Open the **Chip Planner** to view the physical location of the transmitter PLL in the device. Figure 7 shows the EP4SGX530NF45C3 device as an example.

Figure 7. Chip Planner Showing the Physical Location of the Four Transceiver Blocks in the EP4SGX530NF45C3 Device

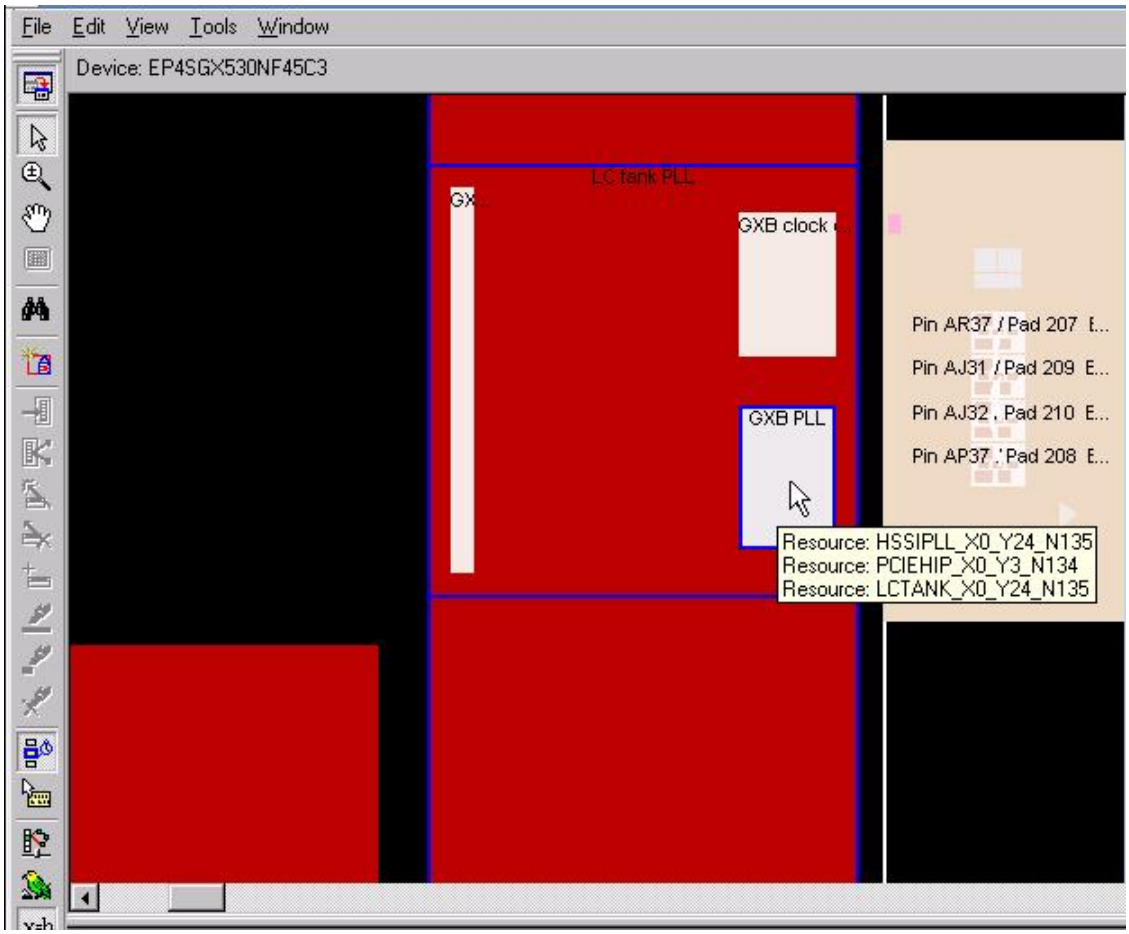


For more information about the location of transmitter PLLs in Stratix IV GX devices, refer to the Stratix *IV Transceiver Architecture* chapter and *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

6. Zoom into the transmitter PLL blocks to observe the physical location of the transmitter PLL (Figure 8). This is assigned by the Quartus II software by default. The X and Y coordinates are the same as those shown in the compilation report (Step 4 of this method).

   If this is not the intended transmitter PLL for the design, note the X and Y coordinates of the desired transmitter PLL in the chip planner and manually assign it as shown in Step 7.

Figure 8. Chip Planner Showing the Physical Location of the ATX PLL Automatically Assigned by the Quartus II Software



7. To manually assign the desired transmitter PLL location, you will need:
   a. Transmitter PLL node information obtained in Step 3 of this method.
   b. Desired transmitter PLL X and Y coordinates obtained in Step 6 of this method.
8. Open the Quartus Settings File (**.qsf**) and include this assignment:

```
set_location_assignment HSSIPLL_X0_Y48_N135 -to
"gxb1_4channels_basic:gxb1_4channels_basic_inst|gxb1_4channels_basi
c_alt4gxb_lev7:gxb1_4channels_basic_alt4gxb_lev7_component|tx_pll"
```

   where **HSSIPLL_X0_Y48_N135** includes the X and Y coordinates of the desired transmitter PLL.

9. Compile the design. Open the chip planner to confirm that the manually assigned transmitter PLL in Step 7 of this method matches the X and Y coordinates of the transmitter PLL assigned to the transmitter PLL node.

Method 2—Using the IOBANK Information

This method is applicable only to the manual placement of CMU PLLs in both Stratix IV GX and GT devices. "Method 1—Using the X and Y Coordinates" on page 4 and Method 2 differ in that Method 1 requires the X and Y coordinates of the desired transmitter PLL in the **.qsf**, while Method 2 requires the IOBANK information associated with each transceiver block in which the desired transmitter PLL resides in the **.qsf**. Table 1 shows the layout of the IOBANK information of the transceiver blocks in the Chip Planner.

Table 1. IOBANK Information in the Chip Planner

Left Side of the Device	Right Side of the Device
IOBANK_QL3 (Top)	IOBANK_QR3 (Top)
IOBANK_QL2	IOBANK_QR2
IOBANK_QL1	IOBANK_QR1
IOBANK_QL0 (Bottom)	IOBANK_QR0 (Bottom)

1. Select the Fitter option in the compilation report as shown in Figure 3 on page 4.
2. Select the Resource Section option as shown in Figure 4 on page 5.
3. Select the GXB Transmitter PLL option.

After you obtain the transmitter PLL node information, you can assign the transceiver block information of the desired CMU PLL as shown in Figure 5 on page 6 to the transmitter PLL node in the **.qsf**. Step 4 of this method explains the IOBANK-based assignment.

4. To assign the desired CMU PLL location manually, you will need:
   a. The transmitter PLL node information obtained in Step 3.
   b. The desired CMU PLL transceiver block (and IOBANK) information
5. Open the **.qsf** and include this assignment:

```
set_location_assignment IOBANK_QL1 -to
"gxb1_4channels_basic:gxb1_4channels_basic_inst|gxb1_4channels_basi
c_alt4gxb_nsv7:gxb1_4channels_basic_alt4gxb_nsv7_component|tx_pll"
```

   where **IOBANK_QL1** has the transceiver block information of the desired CMU PLL.

6. Compile the design. Open the chip planner to confirm that the manually assigned CMU PLL in Step 4 matches the X and Y coordinates of the manually assigned CMU PLL in the compilation report.

Conclusion

In some scenarios, the Quartus II software cannot automatically place the transmitter PLLs by considering the skew requirements of your design. Therefore, it is necessary for you to decide whether a manual placement of the CMU PLL and ATX PLLs is required, and if so, to follow the steps laid out in this application note.

References

- *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*
- *Stratix IV Transceiver Architecture* chapter in volume 2 of the *Stratix IV Device Handbook*

Document Revision History

Table 2 shows the revision history for this application note.

Table 2. Document Revision History

Date and Revision	Changes Made	Summary of Changes
May 2009, v1.0	Initial Release.	—

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