

## Introduction

This document provides design guidelines and factors to consider during the HardCopy® II development flow. Altera recommends following these guidelines throughout the design process to ensure the design is ready for handoff to the Altera® HardCopy Design Center for back-end processing. This document references other relevant information, including detailed specifications, device feature descriptions, and other relevant guidelines.

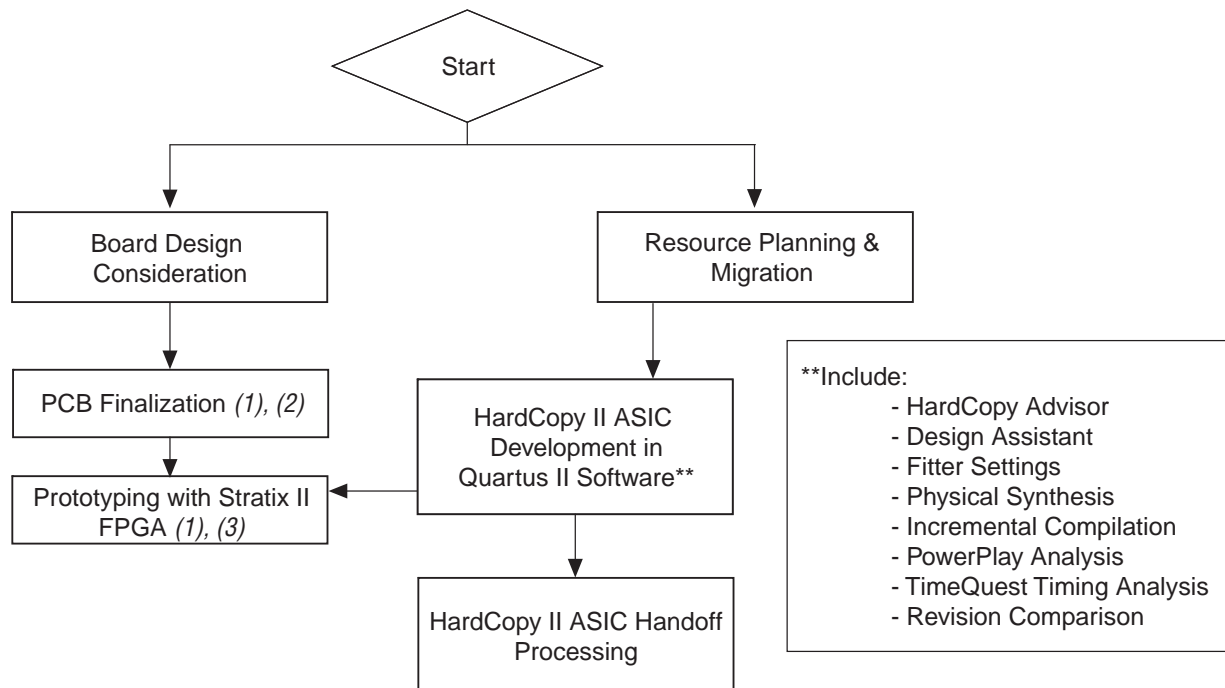
The document discusses various stages of the design flow in the order they are typically performed, as shown in [Table 1](#).

**Table 1.** Summary of Design Flow Stages and Guideline Topics

Design Flow Stage	Topics
<a href="#">“Board Design Considerations” on page 2</a>	Pin settings, power-up mode, configuration pins, power estimation, signal integrity, board simulation
<a href="#">“Resource Planning for HardCopy II ASICs” on page 11</a>	Logic resources, I/O planning, package offerings, speed grade, clock and PLL planning, memory block planning, DSP block planning
<a href="#">“HardCopy II ASIC Development Flow” on page 35</a>	Methods for HardCopy II development flow
<a href="#">“HardCopy Advisor” on page 39</a>	HardCopy Advisor recommendations for HardCopy II ASIC development
<a href="#">“Quartus II Settings for HardCopy II ASIC Development” on page 42</a>	Limit DSP and RAM resources, enable Design Assistant, TimeQuest Timing Analyzer settings
<a href="#">“Quartus II Software Features Supported for HardCopy II ASICs” on page 49</a>	Physical synthesis optimization, LogicLock™ regions, PowerPlay power analyzer, incremental compilation, Fitting and HardCopy readiness overview
<a href="#">“Timing Closure and Verification” on page 57</a>	Timing analysis, timing constraints, and Stratix® II FPGA and HardCopy II revision verification
<a href="#">“HardCopy II ASIC Handoff Process” on page 60</a>	HardCopy II ASIC handoff process

## HardCopy II ASIC Design Guideline Flow Chart

[Figure 1](#) shows a top-level view of the HardCopy II ASIC development flow that is associated with the stages from [Table 1](#).

**Figure 1.** HardCopy II ASIC Design Guideline Flow**Notes to Figure 1:**

- (1) The phases of PCB finalization and prototyping with Stratix II FPGA are not covered in this document.
- (2) PCB Finalization: In this phase, PCB is designed and finalized concurrently with the design of the Stratix II FPGA and the HardCopy II ASIC.
- (3) Prototyping with Stratix II FPGA: Use the Stratix II FPGA to prototype the HardCopy II ASIC for both register transfer level (RTL) and initial software verification.

## Board Design Considerations

When designing for the HardCopy II device, various factors affect the PCB design. This section includes important guidelines for the following topics:

- “Device Power-Up Mode” on page 3
- “Power Pin Connections” on page 4
- “Connecting Configuration Pins” on page 5
- “Pin Planning in the Quartus II Software” on page 7
- “Signal Integrity Considerations for Board Design” on page 10
- “Board-Level Simulation and I/O Analysis” on page 10



For more information about board design guidelines, refer to Altera’s Board Design Guidelines Solution Center at:

[www.altera.com/support/devices/board/brd-index.html](http://www.altera.com/support/devices/board/brd-index.html). The Solution Center references application notes and other documentation that can help you implement successful high-speed PCBs.

## Device Power-Up Mode

When designing a board that will be used for both the Stratix II FPGA prototype and the HardCopy II ASIC device, there are two power-up options that you should consider.

- Instant on (no added delay)
- Instant on after 50 ms (additional delay)

HardCopy II devices support both instant on and instant on after 50 ms power-up modes. Instant on mode, which is the simplest of the available options, operates like an ASIC at power on. This mode can be used in most cases without regard to the original Stratix II FPGA configuration mode and without any hardware or software changes. In some cases, however, a software revision or a board re-design may be necessary to guarantee that correct configuration data is sent to the remaining programmable devices. Such modifications are easily made in the early stages of the board design process if it is determined that one or more of the Stratix II FPGAs will be replaced with an equivalent HardCopy II series device. Board-design techniques such as jumper connectors and 0- $\Omega$  resistors enable such modifications without re-designing the board.



The instant on after 50 ms mode is similar to instant on mode, except that there is an additional delay of 50 ms. This mode is suitable in cases where a delay is necessary to allow the configuration device to become operational, or to allow one or more pre-determined events to be completed before the HardCopy II device asserts CONF\_DONE.

Instant on is the traditional power-up scheme of most ASIC and nonvolatile devices. The instant on mode is the fastest power-up option where the HardCopy II device powers up independently while other components on the board still require initialization and configuration. Therefore, you must verify all signals that propagate to and from the HardCopy II device (for example, reference clocks and other input pins) are stable and do not affect the HardCopy II device's operation.

You must choose one of the power-up options when submitting the design database to Altera for migrating to a HardCopy II device. After the HardCopy II devices are manufactured, the power-up option cannot be changed.



For more information about power-up modes, refer to the *Description, Architecture, and Features* chapter in the *HardCopy II Device Handbook*.

### Hot Socketing and Power Sequencing Support

HardCopy II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a HardCopy II device or a board in a system during system operation without causing undesirable effects to the running system bus or the board inserted into the system. The hot socketing feature helps you use HardCopy II devices on PCBs that contain a mixture of voltages. With the HardCopy II hot socketing features, you no longer have to ensure a proper power-up sequence for each device on the board.

- For more information about HardCopy II hot socketing, refer to the *DC and Switching Specifications and Operating Conditions* chapter in the *HardCopy II Device Handbook*.

## Power Pin Connections

When designing a board, check that all the power pins are connected correctly, determine any unique requirements for power pins on your board, and determine which devices on your board can share the same power rail.

- For a list of the supply voltages required for the HardCopy II device and their recommended operation conditions, refer to the *DC and Switching Specifications and Operating Conditions* chapter in the *HardCopy II Device Handbook*.

For HardCopy II devices, Altera recommends that you use a linear regulator to power the VCCA pins, which supply power to the PLL analog circuits. The linear regulator reduces power noise and improves the system's overall performance. You can also power the digital voltage rails by a linear or switching regulator, depending on the efficiency and cost requirements.

### Early Power Estimation

To aid in board power and thermal management, Stratix II and HardCopy II power consumption must be accurately estimated to develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink, and cooling system. Determining the power consumption early in the design cycle allows for proper planning of power budgets and avoids surprises for designers developing the PCB.

Use the Altera PowerPlay Early Power Estimator spreadsheet during the board design and layout phase to obtain a power estimate so you can properly design for power management.

- For more information about how to use the PowerPlay Early Power Estimator spreadsheet, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

### PLL Board Design Guidelines

Because PLLs contain analog components embedded in a digital device, the following guidelines are provided for designing a board for PLL usage and minimizing jitter:

- Ensure all VCCA and VCCD power pins are connected to a 1.2-V power supply, even if you do not use all of the PLLs in the device.
- Run a thick trace (at least 20 mils) from the power supply to each VCCA pin.
- Use an isolated linear regulator to power VCCA.
- Connect all VCCD power pins to the quietest digital supply on the board.
- Filter each VCCA and VCCD pin with a decoupling circuit.
- Use a ferrite bead and tantalum parallel capacitor for VCCA and VCCD where the power enters the board.

## Connecting Configuration Pins

To properly configure a Stratix II FPGA prototype device, the configuration pins must be connected on the board. When designing a board to use a Stratix II prototype, most configuration pins required by the Stratix II device are not required by the HardCopy II device. To maximize I/O pin counts on a HardCopy II ASIC, minimize use of configuration pins that do not carry over from the Stratix II FPGA to the HardCopy II ASIC. Table 2 lists the dedicated and optional configuration pins that a Stratix II device can use and shows whether or not their optional functionality is used on the HardCopy II device.

**Table 2.** Power Up and Configuration Pin Compatibility (Part 1 of 2)

Stratix II Pin Name		I/O Bank	HardCopy II Use	
Main Function	Optional Function		Main Function	Optional Function
MSEL3	—	B4	—	—
MSEL2	—	B4	—	—
MSEL1	—	B4	—	—
MSEL0	—	B4	—	—
VCCSEL	—	B8	✓	✓
nCONFIG	—	B8	✓	✓
nSTATUS	—	B3	✓	✓
CONF_DONE	—	B3	✓	✓
nCE	—	B3	✓	✓
nCEO	—	B7	✓	✓
PORSEL	—	B7	✓	✓
nIO_PULLUP	—	B7	✓	✓
PLL_ENA	—	B7	✓	✓
I/O pin	CLKUSR	B8	✓	—
I/O pin	DEV_OE	B8	✓	✓
I/O pin	DEV_CLRn	B8	✓	✓
I/O pin	INIT_DONE	B3	✓	✓
DCLK	—	B3	✓	—
I/O pin	DATA0	B3	✓	—
I/O pin	DATA1	B3	✓	—
I/O pin	DATA2	B3	✓	—
I/O pin	DATA3	B3	✓	—
I/O pin	DATA4	B3	✓	—
I/O pin	DATA5	B3	✓	—
I/O pin	DATA6	B3	✓	—
I/O pin	DATA7	B3	✓	—
I/O pin	RDYnBSY	B3	✓	—
I/O pin	CRC_ERROR	B3	✓	—
I/O pin	CS	B8	✓	—
I/O pin	nCS	B8	✓	—

**Table 2.** Power Up and Configuration Pin Compatibility (Part 2 of 2)

Stratix II Pin Name		I/O Bank	HardCopy II Use	
Main Function	Optional Function		Main Function	Optional Function
I/O pin	nRS	B8	✓	—
I/O pin	nWS	B8	✓	—
I/O pin	RUnLU	B8	✓	—
I/O pin	PGM2	B3	✓	—
I/O pin	PGM1	B3	✓	—
I/O pin	PGM0	B3	✓	—
I/O pin	ASDO	B3	✓	—
I/O pin	nCSO	B3	✓	—

Most optional configuration pins listed in [Table 2](#) support the various configuration schemes available in the Stratix II FPGAs. Parallel programming and remote update configuration modes use most of the pins in [Table 2](#). HardCopy II devices do not support the configuration emulation mode.

HardCopy II device can use the Nios® II Flash Programmer to program parallel CFI compliant flash devices. For EPCS serial configuration devices, they connect to the Stratix II device through the dedicated active serial configuration pins (DCLK, SDO, SCE, and DATA0) on the Stratix II device. However, these four dedicated pins are not available in the HardCopy II device. You must reserve four 3.3 V general purpose I/O pins in the HardCopy II device. From the SOPC Builder of Quartus II software, you have to select **HardCopy II device** from the **Device Family** pull-down menu. This generates the following signals to appear at the top of the SOPC Builder system.

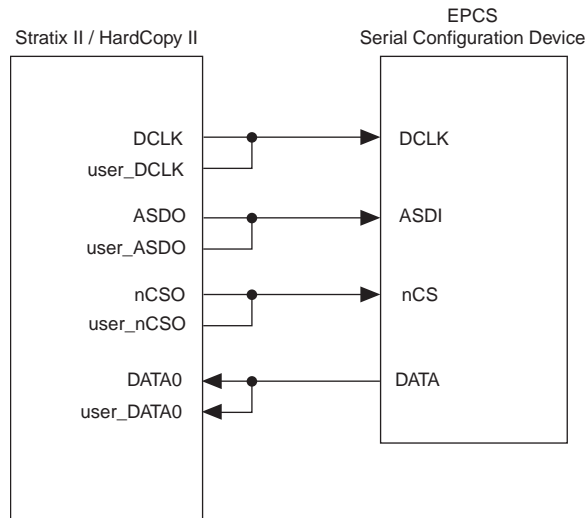
- `dclk_from_the_epcs_controller`
- `sce_from_the_epcs_controller`
- `sdo_from_the_epcs_controller`
- `data0_to_the_epcs_controller`



Altera recommends that you use Quartus II software version 8.0 or later to generate the signals. Contact MySupport for help in supporting EPCS serial device and HardCopy II device with the Nios II Flash Programmer for Quartus II software version earlier than 8.0.

Figure 2 illustrates the connections you make at the board-level in your design.

**Figure 2.** EPCS Serial Configuration Device Connections with Stratix II and HardCopy II Devices



The I/O pins (`user_DCLK`, `user_ASDO`, `user_nCSO`, and `user_DATA0`) are 3.3 V general purpose I/O generated in HardCopy II device. They will be used by the Nios II Flash Programmer and configuration pins (`DCLK`, `ASDO`, `nCSO`, and `DATA0`) that are used to load the Stratix II configuration data.

If some of these dual-purpose pins are required to configure the Stratix II FPGA but are unused after configuration, these pins are completely unused on the HardCopy II device. Removing the Stratix II device and its corresponding configuration device may leave these pins floating on the HardCopy II device if such pins are assigned as inputs by the user without any external means of driving them to a stable level. Thus, when designing the board and selecting the state of dual-purpose pins, consider the state of these pins after power up and when the device enters user mode.


## Pin Planning in the Quartus II Software

In cases where the board design team requires a Quartus® II pin-out file, verify the pin locations in the place-and-route software as soon as possible to avoid the need for board redesign.

Select the appropriate Stratix II and HardCopy II companion devices in the Quartus II software when you start pin planning. You can create a preliminary pin-out file using the Quartus II Pin Planner before the source code is designed, based on standard I/O interfaces (such as memory and bus interfaces) and any other I/O related assignments defined by system requirements. Then, you can use I/O Assignment Analysis to validate I/O related assignments that you make or modify throughout the design process. During the early pin planning for a HardCopy II ASIC design, Altera recommends the following guidelines for pin planning of HardCopy II designs:

- Use dedicated clock input pins for input clocks.
- When driving into PLLs, refer to PLL and clock networks from the device handbook to match dedicated clock pins and PLL locations. (Refer to “[PLL Connectivity](#)” on page 20.)

- For DDR design, use dedicated PLL clock output pins to drive the SDRAM reference clocks.
- For high-speed I/O applications, use I/O pins with differential and SERDES features.
- Place resets and high fan-out inputs on primary clock inputs, if possible.
- Each I/O bank can support multiple I/O standards if they require the same  $V_{CCIO}$  voltage level. Group compatible I/O standards in each bank to avoid pin placement issues.
- Note device configuration pin-out requirements on the Stratix II FPGA, as the HardCopy II device may not require these pins.
- HC210W pins labeled NC (no connect) should be disconnected from the board. On other HardCopy II devices, this may be optional as indicated by the HardCopy II pin-out files.

 For more information regarding I/O assignments, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

### Checking Pin-Tables for Connectivity Requirements

When designing a board for a Stratix II FPGA and a HardCopy II device, be aware that certain product and package combinations may have different connectivity requirements. To avoid pitfalls which include failure to connect configuration devices properly for a Stratix II FPGA, or failure to power up a needed voltage reference pin on either device, Altera recommends that you review and use the pin-out files that contain detailed pin information for the Stratix II and HardCopy II companion devices.

When you refer to the HardCopy II pin table, pins labeled NC are reserved and should be completely disconnected from the board. Failing to do so may yield unexpected behavior.

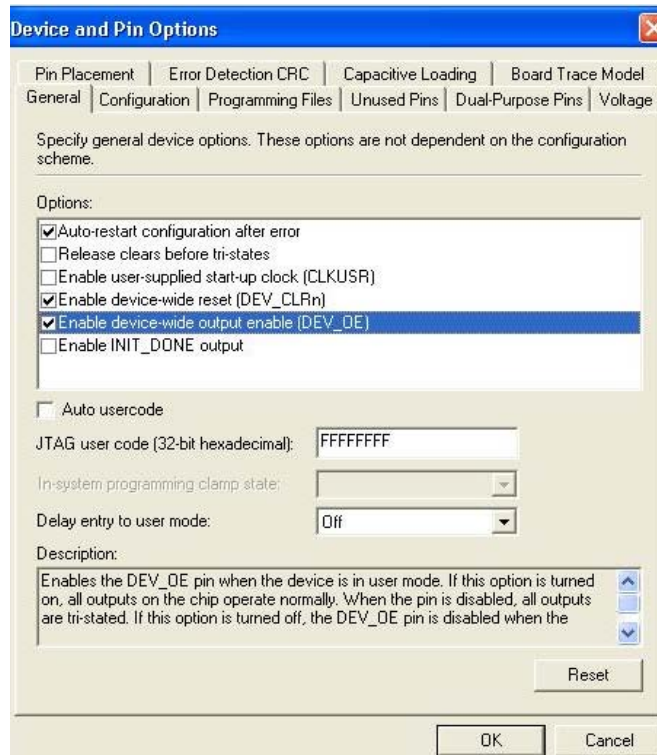
 For information about Stratix II and HardCopy II pin-outs, refer to the pin-out files for Altera devices available at <http://www.altera.com/literature/lit-dp.jsp>.

### Availability of Device-Wide Pins

HardCopy II devices support device-wide reset ( $DEV\_CLRn$ ) and device-wide output enable ( $DEV\_OE$ ). In a HardCopy II device, the optional device-wide reset ( $DEV\_CLRn$ ) allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as designed. The optional device-wide output enable,  $DEV\_OE$ , allows you to

override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. You can enable these optional pins in the Quartus II software under **Device & Pin Options** before compiling your design. Figure 3 shows the settings you should select in the **Device & Pin Options** dialog box.

**Figure 3.** Device and Pin Options Dialog Box



### Specifying the State of Unused Pins

To allow flexibility in board design, you can specify the state of unused pins as one of the following five states in the Quartus II software:

- Inputs that are tri-stated
- Outputs that drive ground
- Outputs that drive an unspecified signal
- Input tri-stated with bus-hold
- Input tri-stated with weak pull-up

Altera recommends that you follow the default setting of Quartus II software to specify the state of these unused pins as “input tri-stated with weak pull-up” in the Assignment Editor. To improve signal integrity on the board, set unused pins as outputs that drive ground and tie them directly to the ground plane on the board. Doing so reduces inductance by creating a shorter return path and reduces noise on the neighboring I/O.

When you compile your design, the Quartus II software generates the pin report file (.pin) to specify how you should connect the device pins. Unused I/O pins are marked in the report file according to the unused pins option you set in the Quartus II software.

## Signal Integrity Considerations for Board Design

This section contains board design guidelines related to simultaneous switching noise (SSN) and I/O termination.

### Simultaneous Switching Noise

SSN becomes a concern when too many pins (in close proximity) change voltage levels at the same time. Noise generated by SSN can reduce noise margin and cause incorrect switching. Although SSN dominates in the device package, poor board layout can contribute to SSN.

 For board layout recommendations that can help reduce some of the noise, refer to the PCB guidelines in Altera's Board Design Guidelines Solution Center at [www.altera.com/support/devices/board/brd-index.html](http://www.altera.com/support/devices/board/brd-index.html).

Breaking out large bus signals on board layers close to the device can help reduce SSN. If two signal layers are next to each other, route traces orthogonally and use a separation of two to three times the trace width, if possible.

### I/O Termination

Voltage-referenced I/O standards require both an input reference voltage,  $V_{REF}$ , and a termination voltage,  $V_{TT}$ . The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL2 I/O standards to produce a reliable DDR memory system with superior noise margin.


Typically, single-ended, non-voltage-referenced I/O standards do not require termination. However, to improve signal integrity and reduce unwanted transmission line reflections, you can match your source driver impedance to the transmission line impedance by using on-chip termination or customizing your drive strength setting. You can verify your settings using Altera's IBIS models. The IBIS models can be downloaded at:

[http://www.altera.com/support/software/download/ibis/ibs-ibis\\_index.html](http://www.altera.com/support/software/download/ibis/ibs-ibis_index.html)

HardCopy II on-chip series and parallel termination provides the convenience of no external components. Alternatively, you can use external pull-up resistors to terminate the voltage-referenced I/O standards such as SSTL and HSTL.

## Board-Level Simulation and I/O Analysis

To ensure that the I/O signaling meets receiver threshold levels on your board setup, perform full board routing simulation with third-party board-level simulation tools using the IBIS model. You can generate the IBIS model from the Quartus II software. In the Quartus II software, select **IBIS** under **Board-level signal integrity analysis** on the **EDA Tool Settings** page of the **Settings** dialog box.

 For more information about this simulation flow, refer to the *Signal Integrity with Third-Party Tools* chapter in volume 3 of the *Quartus II Handbook*.

When you include a Stratix II FPGA with high-speed interfaces in a board design, knowing the signal integrity and board routing propagation delay is vital for proper system operation. Analyze board-level timing as part of I/O and board planning.


You can configure board trace models of selected I/O standards and generate “board-aware” signal integrity reports with the Quartus II software. When **Enable Advanced I/O Timing** is turned on, the TimeQuest Timing Analyzer uses simulation results for the I/O buffer, package, and board trace model to generate more accurate I/O delays and extra reports to give insight into signal behavior at the system level. You can use these advanced timing reports as a guide to make changes to the I/O assignments and board design to improve timing and signal integrity.

## Resource Planning for HardCopy II ASICs

HardCopy II ASIC resource planning is dependent on the availability of Stratix II FPGA resources. Certain resources in Stratix II FPGAs are not available in HardCopy II ASICs. The first stage of HardCopy II ASIC resource planning is to choose the Stratix II device density, speed grade, package, and core voltage that best suit your design needs. Before you begin compiling a design in a third-party synthesis tool or by using the Quartus II software, set the correct Stratix II FPGA and the HardCopy II ASIC companion device based on the devices’ best resource balance for your design requirements. This step ensures that equivalent resources are used in the Stratix II FPGA and HardCopy II ASIC.

In this section, the following resource planning areas for HardCopy II ASICs are covered:

- “Available Logic Resources” on page 12
- “I/O Planning” on page 12
- “Package Offering” on page 16
- “Speed Grade” on page 17
- “Clock and PLL Planning” on page 17
- “Memory Blocks Planning” on page 32
- “DSP Blocks Planning” on page 35

 For information about the resources in each HardCopy II device, including logic, memory blocks, multipliers, and phase-locked loops (PLLs), as well the various package offerings and I/O pin counts, refer to the *Description, Architecture, and Features* chapter in volume 1 of the *HardCopy II Device Handbook*.

## Available Logic Resources

Both Stratix II and HardCopy II devices offer a range of densities that provide different amounts of device logic resources. For the logic resource planning of both Stratix II and HardCopy II companion devices, the required logic density of the Stratix II device must be determined and selected to ensure the logic resource availability in the HardCopy II companion device. Select a Stratix II device that meets your design needs with some safety margin, in case you want to add more logic later in the design cycle or expand your design. The Quartus II software includes a device resource guide to help select the optimal HardCopy II device based on the design requirements.

Selecting a HardCopy II device with more logic resources makes it possible for you to implement larger and potentially more complex designs. This requires a larger HardCopy II device, which may result in higher product cost. Smaller HardCopy II devices have less logic resources available and lower static power.



For more information about the device resource guide, refer to the *Quartus II Support for HardCopy II Devices* chapter in volume 1 of the *HardCopy Series Handbook*.

## I/O Planning

HardCopy II devices offer pin-to-pin compatibility with the Stratix II devices, making them drop-in replacements for these Stratix II FPGAs. Therefore, the same system board and software developed for the Stratix II FPGA prototype and field trials can be retained, enabling fast time-to-market for high-volume production.

### Pin Planning with the Quartus II Software

The HardCopy II family offers multiple core sizes and pin packages to match your Stratix II FPGA design. To facilitate this conversion process, the Quartus II software offers various features to guide you through the Stratix II FPGA and HardCopy II design process. This section focuses mainly on the pin planning process and offers recommendations for facilitating migration to a HardCopy II device.

Quartus II software features include:

- “Companion Device Settings” on page 13 — ensures compatibility between the Stratix II FPGA and HardCopy II devices
- “I/O Assignment Analysis” on page 13 — evaluates I/O settings
- “Fast Input and Fast Output Registers” on page 13

In addition, to achieve the best I/O performance with a HardCopy II device, this section offers recommendations for I/O placement, configuration, unused pins, and signal integrity.

### Companion Device Settings

The HardCopy II design flow allows migration from different Stratix II devices to the same HardCopy II device. For example, both EP2S130 and EP2S180 designs can be migrated to a HC230 device even though they have different amounts of resources. When you specify the HardCopy II companion device in your design project, the Quartus II software ensures that both your Stratix II design and HardCopy II design are equivalent by using resources that are common to both devices. Therefore, you must select your companion device to ensure compatibility between the Stratix II FPGA and the HardCopy II devices.

### I/O Assignment Analysis

HardCopy II devices offer three distinct types of I/O elements (IOEs), each of which supports a specific set of I/O features and standards. You can run the **I/O Assignment Analysis** in the Quartus II software to verify your I/O settings and assignments without the actual design files. For example, the Quartus II software can check the supported I/O standards or identify incompatible I/O settings on assigned I/Os. Altera recommends you do not leave any I/O with unassigned I/O standards, configuration, or termination schemes before you run the **I/O Assignment Analysis** in the Quartus II software. Otherwise, by default, the Quartus II software assigns these I/Os to LVTTTL, which may not be compatible with your intended I/O standard.

The following I/O information is also required by the Quartus II software:

1. Weak pull-up and weak pull-down passive elements identified on the I/O assignment
2. Output capacitance loading for both output only and bidirectional pins
3. Output drive strength
  - a. The default output drive strength is 24 mA assigned by the Quartus II software.
  - b. You must determine if the I/O needs 24 mA drive strength on the HardCopy II device even though the 24 mA drive strength may pose no problem on the Stratix II FPGA. Refer to the section [“Managing Signal Integrity” on page 16](#).
4. Set the **Allow voltage overdrive for LVTTTL/LVCMOS input pins** option.
  - a. This option specifies whether the Fitter allows input pins with LVTTTL or LVCMOS I/O standards to be placed inside an I/O bank with a lower  $V_{CCIO}$  voltage than the voltage specified by the pins.
  - b. Over-driving the I/O bank results in higher leakage current, which can cause the design to function in unintended ways.

### Fast Input and Fast Output Registers

To achieve the fastest register to pin timing, use the fast input and fast output registers wherever possible. These registers are located in the I/O elements of both the Stratix II FPGA and HardCopy II device. They can be enabled under the **Fast Input Register** and **Fast Output Register Logic** options in the Quartus II software. Moreover, these register-to-pin paths are pre-defined and provide more consistent I/O timing results between the Quartus II software and back-end processes. For

example, when you convert your Stratix II FPGA design to a HardCopy II design, the back-end place-and-route tool re-routes your design in the HardCopy II device according to the specified timing and design constraints. I/O routings and the corresponding I/O timing from the back-end tool may differ slightly from Quartus II timing reports even though both results meet the timing constraints.

## I/O Management

This section discusses various types of I/Os, including clock, power, configuration, external memory interfaces, and unused resources, as well as their recommended settings.

### Managing Clock Pins

In both Stratix II FPGAs and HardCopy II devices, certain I/Os are specifically designed for transmitting and receiving clock signals. Especially for a PLL, each clock source can come from any of the four clock pins located on the same side of the device as the PLL. There are also three differential or six single-ended external clock output pins, such as `PLL5_OUT`, fed from the PLL counters. (Refer to the section [“Clock and PLL Planning” on page 17.](#)) These I/Os are specifically designed for clock transmission.

The PLL can drive out to any regular I/O pin through the global or regional clock network. However, jitter on the output clock may vary. Generally, source-synchronous designs impose stringent timing requirements. Therefore, use dedicated PLL output pins to drive the reference clocks in this case.

Similar to fast input and fast output registers, the routing of dedicated clock pins is also pre-defined and thus ensures consistent timing results between the Quartus II software and back-end processes. Pre-defined routing improves timing prediction of the design.

In addition to functioning as a clock, these I/Os can be used for high fan-out inputs such as global reset. Because these clock inputs are routed to global and regional clock networks internally, the Quartus II software automatically routes these high fan-out signals to the global or regional clocks to improve the fitting result. You can also manually assign these high fan-out nets to global networks if all the clock pins are not available. For more information, refer to the section [“High Fan-Out Clock Nets” on page 18.](#)

### External Memory and Other Source-Synchronous Interfaces

Many high-speed external memory or source-synchronous interfaces require stringent timing requirements for write and read operations. Also, the input buffers require a reference voltage to improve signal speed. Therefore, special care should be taken when placing these I/O interfaces.

Dedicated clock output pins for clocks going off-chip are required for HardCopy II designs using memory interfaces (DDR, DDR2, QDR, RLDRAM). You must use dedicated clock pins in Stratix II FPGAs whenever possible for output clocks, particularly if you plan to migrate your design to a HardCopy II device. For more information about clock pins, refer to [“Managing Clock Pins” on page 14.](#)

Due to the difference in the interconnect delays between the Stratix II FPGA and HardCopy II ASIC, the use of non-primary clock inputs as clock inputs in a design may cause a timing closure problem when migrating the Stratix II FPGA to a HardCopy II ASIC. If primary clock inputs are not available, you can place the I/O close to clock input on the pin planner to improve timing closure.

 For more information about designing source-synchronous interfaces, refer to [AN 477: Design RGMII Interface with FPGA and HardCopy Devices](#).


### Managing Power and $V_{REF}$ Pins

As mentioned earlier, the Quartus II software enables resources that can be migrated to a HardCopy II device when you specify the HardCopy II companion device in your Stratix II FPGA project. One task the Quartus II software performs is to verify power and  $V_{REF}$  pins in both the Stratix II FPGA and the HardCopy II device. For example, certain Stratix II FPGA user I/Os are handled as No Connect (NC) in HardCopy II devices. Also, certain pins that are NC in HardCopy II devices are power pins in a Stratix II FPGA. Therefore, always specify your HardCopy II companion device for your Stratix II FPGA prototype constraints in the pin assignments in your Quartus II project. Let the Quartus II software guide the design process. Pin assignments are constrained in the Stratix II FPGA design revision, so that the HardCopy II device selected is pin-compatible. You can also refer to the HardCopy II pin tables for more information.

### Managing Configuration Pins

When you design a board for a Stratix II device and its companion HardCopy II device, most configuration pins required by the Stratix II device are not required by the HardCopy II device. To allow for more I/O availability in a HardCopy II device, Altera recommends minimizing configuration pins that will not carry over from a Stratix II device into a HardCopy II device. Stratix II devices have dedicated and optional configuration functions for their configuration pins. A HardCopy II device can use the pin's optional function from Stratix II device. In the Quartus II software, these pins are allowed to set as dual purpose pins. As the dual purpose pins, they will only switch to their I/O designation when the device enters user mode (when INIT\_DONE is asserted).

In addition, migrating from a Stratix II to a HardCopy II device may leave some dual-purpose configuration pins such as nCS, nRS, and nWS floating on the HardCopy II device. Therefore, it is important to consider the after-configuration requirements of these pins and set them appropriately in the Quartus II software.

 For more information about after-configuration requirements for pins, refer to [Migrating Stratix II Device Resources to HardCopy II Devices](#) in volume 2 of the *HardCopy II Device Handbook*.

### Managing Unused I/O Pins

HardCopy II devices offer up to 951 user I/Os. Frequently, designs may not use all available I/O pins. Altera recommends that you follow the HardCopy Advisor's default setting to configure these unused pins as **input tri-stated with weak pull-up**. If enhancement of SSN performance is needed, you can also configure them as **output driving ground** and connect them to the ground plane on the board.

## Managing Signal Integrity

Managing signal integrity is extremely important, even for slow speed applications. For example, an input clock with a slow edge rate may be more susceptible to noise even though its operating frequency is low. The following three topics are discussed in this section:

- Input edge rate
- Output drive strength
- I/O simulation

Input edge rate is application-dependent. For slower input edge rate signals, you can set ground pins on the adjacent output pins or turn on slow slew rate on the adjacent output pins to reduce switching noise on the board. For clock and asynchronous control input signals, you can set the edge rate as fast as possible to avoid potential signal integrity issues.

 For more information, refer to *Input Signal Edge Rate Guidance White Paper*.

Avoid placing an input clock pin and a fast output switching pin on the same pair of differential I/Os. Differential I/Os are designed to be tightly coupled to improve noise margin; thus, a signal from a fast output switching pin may couple to the input clock signal.

The Quartus II software's default output drive strength may be too high in many applications. Assigning the proper output drive strength improves signal integrity while achieving timing requirements. Therefore, it is beneficial to evaluate the appropriate output drive strengths that the system requires. Altera provides a complete set of IBIS and SPICE models to allow users to simulate the various settings. Always use IBIS or SPICE simulations to make sure that the I/O selections are appropriate for your board. The IBIS models can be downloaded at [http://www.altera.com/support/software/download/ibis/ibs-ibis\\_index.html](http://www.altera.com/support/software/download/ibis/ibs-ibis_index.html).

## Package Offering

HardCopy II companion devices are available in a space-saving FineLine BGA package with various I/O pin counts. In addition, certain package sizes support vertical migration for the Stratix II FPGA devices.

**Table 3** lists the available Stratix II and HardCopy II companion pairs.

**Table 3.** Stratix II and HardCopy II Companion Devices (Part 1 of 2)

Package	Companion Pair	
	HardCopy II Device	Stratix II Device
484-pin FineLine BGA	HC210W (1)	EP2S30
484-pin FineLine BGA	HC210W (1)	EP2S60
484-pin FineLine BGA	HC210W (1), (2)	EP2S90
484-pin FineLine BGA	HC210	EP2S30
484-pin FineLine BGA	HC210	EP2S60
484-pin FineLine BGA	HC210 (2)	EP2S90 (3)
672-pin FineLine BGA	HC220	EP2S60

**Table 3.** Stratix II and HardCopy II Companion Devices (Part 2 of 2)

Package	Companion Pair	
	HardCopy II Device	Stratix II Device
780-pin FineLine BGA	HC220	EP2S90
780-pin FineLine BGA	HC220 (2)	EP2S130
1020-pin FineLine BGA	HC230	EP2S90
1020-pin FineLine BGA	HC230	EP2S130
1020-pin FineLine BGA	HC230 (2)	EP2S180
1020-pin FineLine BGA	HC240	EP2S180
1508-pin FineLine BGA	HC240	EP2S180

**Note to Table 3:**

- (1) The HC210W device uses a wire bond package, while the Stratix II FPGA prototype device uses a pin-compatible flip-chip package.
- (2) Depending on design specific resource utilization, an opportunistic migration path may exist between this device pair. Be sure to confirm that your design is a potential candidate for such a path by fitting with the Quartus II software and consulting an Altera applications engineer.
- (3) This is a Hybrid FineLine BGA package for Stratix II FPGA. For more details, refer to the [Package Information for Stratix II and Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II Device Handbook*.

## Speed Grade

The speed grade of the Stratix II device determines the device timing performance and timing closure as well as power usage. A HardCopy II device does not have speed grades as a Stratix II FPGA does. The Quartus II software optimizes and analyzes your design using timing constraints to achieve the performance requirements and timing closure for the HardCopy II device. For information about timing constraints, refer to the section [“Timing Constraints Using the TimeQuest Timing Analyzer”](#) on page 58.

## Clock and PLL Planning

Determining your system clock requirements ensures that you have a robust system. You should understand clocks and PLL resource availability for both the Stratix II FPGA and HardCopy II companion device and correspondingly plan the design clocking scheme. Consider your requirements for timing performance, as well as how much logic is driven by a particular clock.

### Clock Networks

HardCopy II devices provide low skew and low delay clock networks. These clocks are organized into a hierarchical clock structure that provides up to 48 unique clock domains within the entire HardCopy II device and allows 24 unique clock sources per device quadrant. There are up to 12 PLLs per device, and 16 differential dedicated global clock input pins or 32 single-ended clock inputs.

Use the dedicated clock pins and routing for clock signal inputs to your design. The dedicated clock pins drive the clock network directly, ensuring lower skew than other I/O pins. Use the dedicated routing network to have a predictable delay with less skew for high fan-out signals. You can also use the clock pins and clock network to drive control signals such as asynchronous reset.

Specific clock inputs connect to specific PLLs, which can drive specific low skew routing networks. Analyze the global resource availability for each PLL and the PLL availability for each clock input pin. For more information about PLL connections, refer to the section [“PLL Connectivity” on page 20](#).

Use the following descriptions to help determine which clock networks are appropriate for the clock signals in your design:

- The global clock (GCLK) networks can drive throughout the entire device, serving as low skew clock sources for device logic. This clock region has the maximum delay compared to other clock regions but allows the signal to reach everywhere within the device. This option is good for routing global reset and clear signals or routing clocks throughout the device.
- The regional clock (RCLK) networks only pertain to the quadrant they drive into. The RCLK networks provide the lowest clock delay and skew for logic contained within a single device quadrant.
- I/O elements (IOEs) and internal logic can also drive GCLKs and RCLKs to create internally generated global or regional clocks and other high fan-out control signals, such as synchronous or asynchronous clears and clock enables.
- PLLs cannot be driven by internally-generated GCLKs or RCLKs. The reference clock input of the PLL must come from dedicated clock input pins, particularly if your design is interfacing with an external memory.

For more information about PLL and clock networks, refer to the [Description, Architecture, and Features](#) chapter in volume 1 of the *HardCopy II Device Handbook*.

If your system requires more dedicated clocking resources than are available in the target device, consider assigning low fan-out and low-frequency signals to non-dedicated clocking resources. Use the **Global Signal** assignment in the Quartus II Assignment Editor to select the type of global routing, or set the assignment to **Off** to specify that the signal should not use any global routing resources.

### High Fan-Out Clock Nets

In Stratix II FPGAs and HardCopy II devices, the 16 global clock and 32 regional clock networks are typically used for clocks. They are also used for high fan-out signals in the Quartus II software. These global resources are pre-built and do not take up regular routing resources.

While compiling the Stratix II FPGA, the Quartus II software determines which nets are critical to promote to global resources based on the Stratix II FPGA floorplan. When the HardCopy II companion device is compiled, the Quartus II software uses the same global resources as in the Stratix II FPGA compile because the global resource usage has to match for revision comparison. This does not take into account the HardCopy II design floorplan and its routing congestion. Using global and regional resources can help relieve routing congestion in a HardCopy II design floorplan. Because the Quartus II software promotes the global clock automatically, regional clocks are only used automatically in fitting when global resources have all been used. Manual regional clock specification for select signals can free up global resources for other purposes.

In the **Resource** section of the Fitter report, you can see if there are high fan-out nets that are not assigned to global resources. If there are global resources available, the high fan-out nets can be assigned to global resources. This must be done in both the Stratix II FPGA and HardCopy II companion revisions. If the assignment was made to the Stratix II FPGA revision first, the HardCopy II companion revision assumes these assignments after the Stratix II FPGA revision is compiled and migrated.

### PLL Resources

Both HardCopy II devices and Stratix II FPGAs support enhanced and fast PLLs, but HardCopy II devices have a different number of PLLs than Stratix II devices. You should ensure that the prototype Stratix II design uses the same PLL resources that are available in the HardCopy II device.

Table 4 shows which PLLs are supported for each Stratix II FPGA device and HardCopy II device pair. Depending on the device and package combination, not all PLLs in Stratix II are supported by HardCopy II devices. For example, the Stratix II EP2S60 device has 4 fast PLLs and 2 enhanced PLLs supported, but the HardCopy II HC210W companion device only supports 2 fast PLLs and 2 enhanced PLLs. In general, fast PLLs are removed from the sides that do not support high-speed IOEs.



For the HardCopy II PLL number designations, refer to the *Migrating Stratix II Device Resources to HardCopy II Devices* chapter in volume 3 of the *HardCopy II Device Handbook*.

**Table 4.** Stratix II and HardCopy II Companion Device PLL Availability Guide

Stratix II and HardCopy II Companion Devices	Package	Fast PLLs								Enhanced PLLs			
		1	2	3	4	7	8	9	10	5	6	11	12
EP2S30 HC210W	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S60 HC210W	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S90 HC210W	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S30 HC210	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S60 HC210	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S90 HC210	484-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S60 HC220	672-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S90 HC220	780-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S130 HC230	780-pin FineLine BGA	✓	✓	●	●	—	—	—	—	✓	✓	—	—
EP2S90 HC230	1020-pin FineLine BGA	✓	✓	●	●	✓	✓	●	●	✓	✓	✓	✓
EP2S130 HC230	1020-pin FineLine BGA	✓	✓	●	●	✓	✓	●	●	✓	✓	✓	✓
EP2S180 HC230	1020-pin FineLine BGA	✓	✓	●	●	✓	✓	●	●	✓	✓	✓	✓
EP2S180 HC240	1020-pin FineLine BGA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180 HC240	1508-pin FineLine BGA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

**Notes to Table 4:**

- (1) ✓ — PLLs are available in both Stratix II and HardCopy II devices.
- (2) ● — PLLs are available in the Stratix II device only.

HardCopy II PLLs are functionally identical to Stratix II PLLs, but the target HardCopy II device may not support the same number of fast PLLs as the prototype Stratix II FPGA. Because HardCopy II fast PLLs and enhanced PLLs offer a similar feature set, an enhanced PLL can be used in place of a fast PLL. The type of PLL used in the design should be chosen using the Quartus II software to accommodate the resources available in the HardCopy II device.

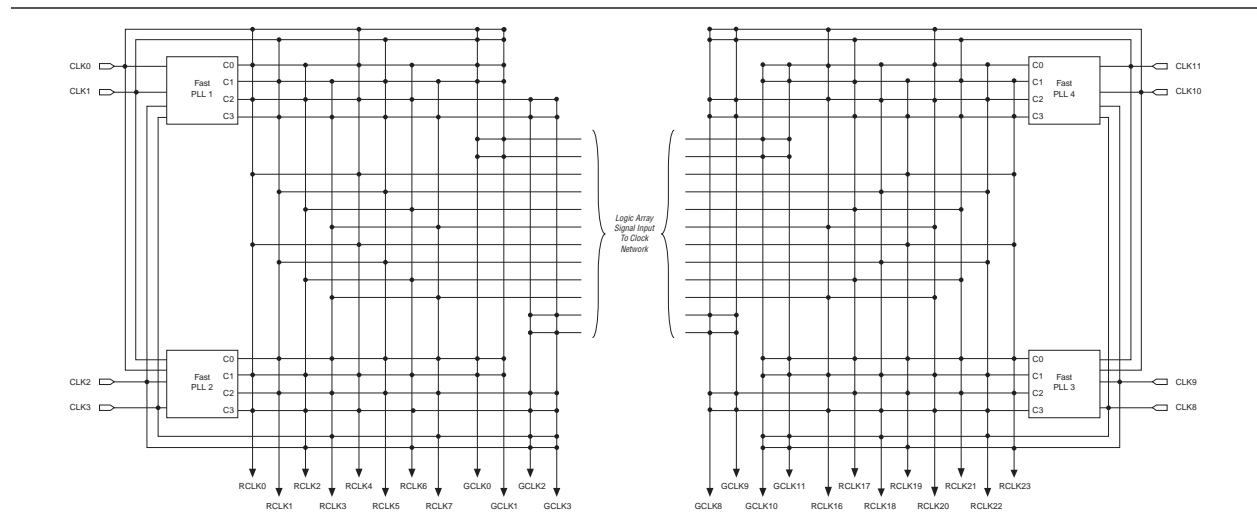
During the prototyping stage, the Quartus II software provides a migration path from the Stratix II FPGA device to a HardCopy II device. When the companion device is selected, the Quartus II software uses the PLL resources that are common to both the Stratix II FPGA device and the HardCopy II device, thereby ensuring compatibility.

### PLL Connectivity

While planning your design's clocking scheme, note the available clock resources in the selected HardCopy II device. A HardCopy II device has up to 12 PLLs (eight fast PLLs and four enhanced PLLs).

Figure 4 and Figure 5 show the fast PLL connections to the regional clock networks (RCLK0 - RCLK7, RCLK16 - RCLK23) and global clock networks (GCLK0 - GCLK3, GCLK8 - GCLK11). There is no dedicated clock output pin connected to the fast PLLs' outputs PLL1-4 and PLL7-10. The fast PLL global and regional outputs can drive out any I/O pin as an external clock output pin. For information about connecting dedicated I/O pins to the fast PLLs' input clocks, refer to Table 5 through Table 9.

**Figure 4.** Fast PLL Connectivity for a HardCopy II ASIC



**Figure 5.** Fast PLL Connectivity for a HardCopy II ASIC

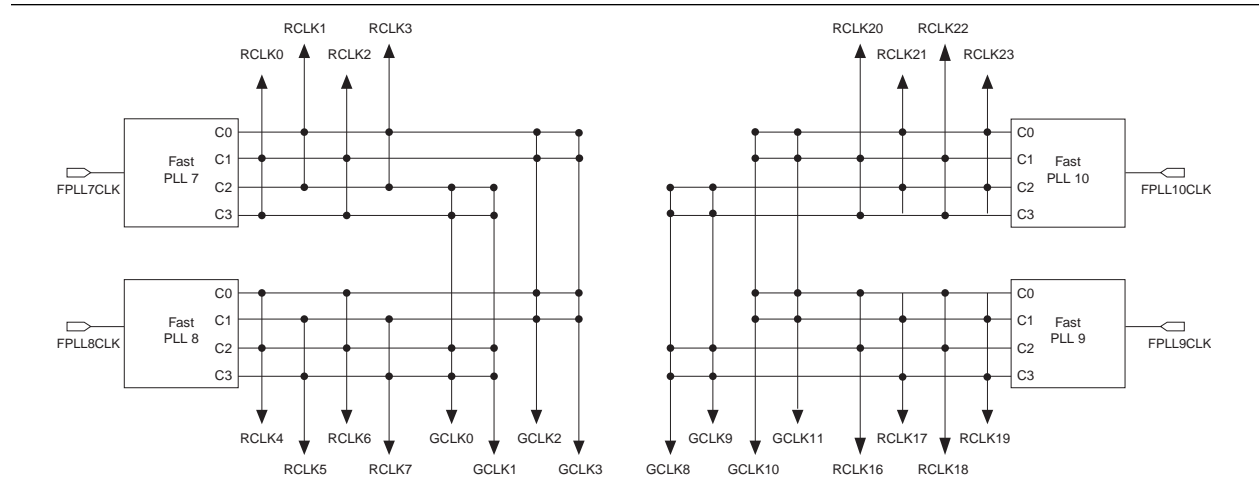


Figure 6 shows the enhanced PLL connection of PLL5, PLL6, PLL11, and PLL12 to the regional clock networks, global clock networks (GCLK4 - GCLK7, GCLK12 - GCLK15) and up to six single-ended clock outputs (three differential pairs). Any of the six outputs can feed the dedicated external clock output pins.

**Figure 6.** Enhanced PLL Connectivity for a HardCopy II ASIC

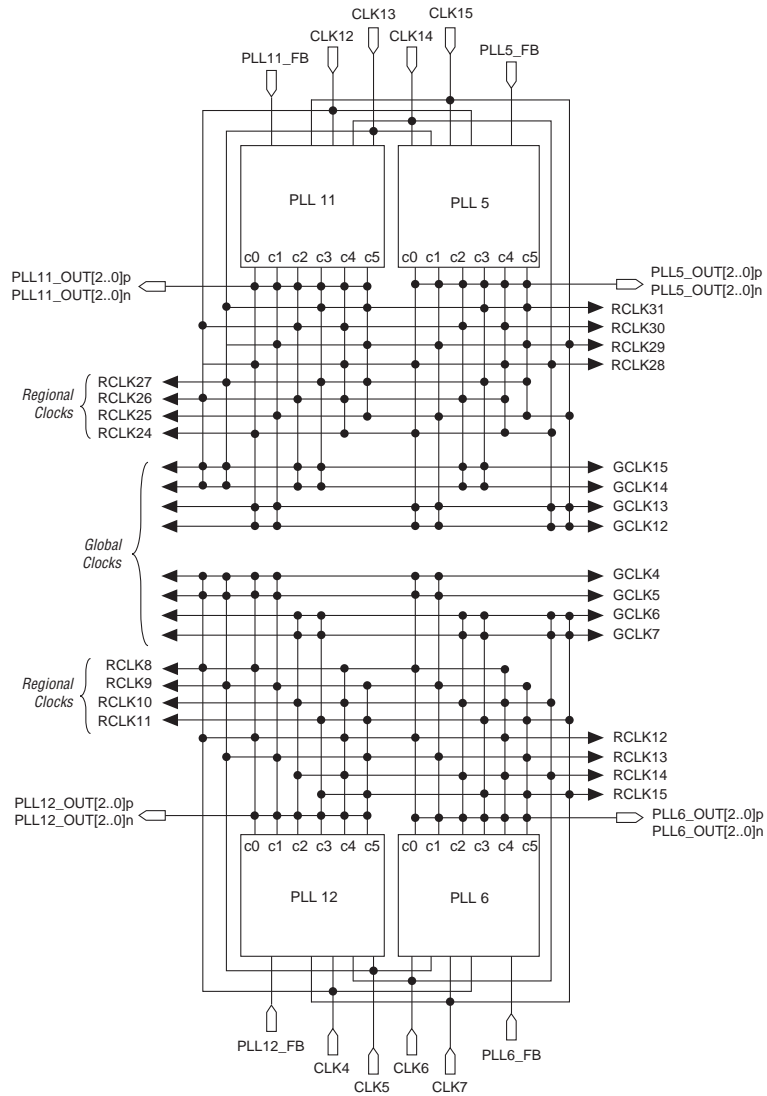


Table 5 through Table 9 show the dedicated I/O pin connections for the HardCopy II fast and enhanced PLLs.

**Table 5.** Dedicated I/O Pin Names for Package F484 (Note 1)

Package F484 (2)	Input Clocks			Output Clocks			
	Inclk		Fbin	C0-C3		C4-C5	
	P(N)	P(N)	P(N)	P(N)		P(N)	
PLL1	L21 (L20)	N22(N21)	—	(3)			
	M21(M20)	N20(N19)					
PLL2	L21(L20)	N22(N21)					
	M21(M20)	N20(N19)					
PLL3	N1(N2)	L2(L3)					
	N3(N4)	M2(M3)					
PLL4	N1(N2)	L2(L3)					
	N3(N4)	M2(M3)					
PLL5	B11(C11)	A13(B13)	B9(C9)	A10(B10)	C10(D10)	A10(B10)	C10(D10)
	B12(C12)	C13(D13)	B9(C9)				
PLL6	AB13(AA13)	AA11(Y11)	W9(V9)	AB10(AA10)	AA9(Y9)	AB10(AA10)	AA9(Y9)
	AA12(Y12)	Y10(W10)	W9(V9)				
PLL7	(4)				—	—	
PLL8					—	—	
PLL9					—	—	
PLL10					—	—	
PLL11					(4)		
PLL12					(4)		

**Notes to Table 5:**

- (1) Package balls B9, C9, W9, and V9 are used as either external clock outputs or for external feedback inputs. If the design uses external feedback input pins, you lose one (or two, if Fbin is differential) dedicated output clock pin.
- (2) PLL1 to PLL4, PLL5 to PLL10 are Fast PLLs; PLL5, 6, 11, 12 are Enhanced PLLs.
- (3) There are no dedicated external clock output pins for fast PLL. The fast PLL global or regional outputs can drive any I/O pins as external clock output pins.
- (4) Stratix II FPGAs (EP2S30, EP2S60, and EP2S90) in the 484-pin package do not have fast PLLs 7-10 and enhanced PLLs 11 and 12.

**Table 6.** Dedicated I/O Pin Names for Package F672 (Note 1)

Package F672 (2)	Input Clocks			Output Clocks								
	Inclk		Fbin	C0-C3		C4-C5						
	P(N)	P(N)	P(N)	P(N)		P(N)						
PLL1	P25(P24)	R26(R25)	—	(3)								
	N25(N24)	P23(P22)										
PLL2	P25(P24)	R26(R25)										
	N25(N24)	P23(P22)										
PLL3	R1(R2)	P2(P3)										
	R3(R4)	N2(N3)										
PLL4	R1(R2)	P2(P3)										
	R3(R4)	N2(N3)										
PLL5	B13(C13)	A15(B15)						C12(D12)	A12(B12)	D13(E13)	A12(B12)	D13(E13)
	B14(C14)	C15(D15)							C12(D12)			
PLL6	AF15(AE15)	AE14(AD14)						AD12(AC12)	AF12(AE12)	AE13(AD13)	AF12(AE12)	AE13(AD13)
	AC14(AB14)	AC13(AB13)							AD12(AC12)			
PLL7	(4)			—	—	—	—					
PLL8	(4)			—	—	—	—					
PLL9	(4)			—	—	—	—					
PLL10	(4)			—	—	—	—					
PLL11	(4)			(4)								
PLL12	(4)			(4)								

**Notes to Table 6:**

- (1) Package balls C12, D12, AD12, and AC12 are used as either external clock outputs or for external feedback inputs. If the design uses external feedback input pins, you lose one (or two, if Fbin is differential) dedicated output clock pin.
- (2) PLL1 to PLL4, PLL5 to PLL10 are Fast PLLs; PLL5, 6, 11, 12 are Enhanced PLLs.
- (3) There are no dedicated external clock output pins for fast PLLs. The fast PLL global or regional outputs can drive any I/O pins as external clock output pins.
- (4) Stratix II FPGAs (EP2S60) in the 672-pin package do not have fast PLLs 7-10 and enhanced PLLs 11 and 12.

**Table 7.** Dedicated I/O Pin Names for Package F780 (Note 1)

Package F780 (2)	Input Clocks			Output Clocks			
	Inclk		Fbin	C0-C3		C4-C5	
	P(N)	P(N)	P(N)	P(N)		P(N)	
PLL1	P28(P27)	R28(R27)	—	(3)		—	
	N28(N27)	T28(T27)					
PLL2	P28(P27)	R28(R27)					
	N28(N27)	T28(T27)					
PLL3	R1(R2)	P1(P2)					
	T1(T2)	N1(N2)					
PLL4	R1(R2)	P1(P2)					
	T1(T2)	N1(N2)					
PLL5	A15(B15)	A16(B16)	C12(D12)	A12(B12)	D13(E13)	A12(B12)	D13(E13)
	D14(C14)	C15(D15)		C12(D12)			
PLL6	AH16(AG16)	AH15(AG15)	AD12(AC12)	AF12(AE12)	AE13(AD13)	AF12(AE12)	AE13(AD13)
	AF15(AE15)	AF14(AE14)		AD12(AC12)			
PLL7	(4)				—	—	
PLL8					—	—	
PLL9					—	—	
PLL10					—	—	
PLL11					(4)		
PLL12							

**Notes to Table 7:**

- (1) A12, B12, AH12, and AG12 are used as either external clock outputs or for external feedback inputs. If the design uses external feedback input pins, you lose one (or two, if Fbin is differential) dedicated output clock pin.
- (2) PLL1 to PLL4, PLL5 to PLL10 are Fast PLLs; PLL5, 6, 11, 12 are Enhanced PLLs.
- (3) There are no dedicated external clock output pins for fast PLL. The fast PLL global or regional outputs can drive any I/O pins as external clock output pins.
- (4) Stratix II FPGAs (EP2S90, EP2S130) in the 780-pin package do not have fast PLLs 7-10 and enhanced PLLs 11 and 12.

**Table 8.** Dedicated I/O Pin Names for Package F1020 (Note 1)

Package F1020 (2)	Input Clocks			Output Clocks								
	Inclk		Fbin	C0-C3		C4-C5						
	P(N)	P(N)	P(N)	P(N)		P(N)						
PLL1	T32(T31)	U32(U31)	—	(3)								
	T30(T29)	U30(U29)										
PLL2	T32(T31)	U32(U31)										
	T30(T29)	U30(U29)										
PLL3	U1(U2)	T1(T2)										
	U3(U4)	T3(T4)										
PLL4	U1(U2)	T1(T2)										
	U3(U4)	T3(T4)										
PLL5	A16(B16)	A17(B17)						D15(E15)	B15(C15)	C16(D16)	B15(C15)	C16(D16)
	E16(F16)	C17(D17)							D15(E15)			
PLL6	AM17(AL17)	AM16(AL16)						AL15(AK15)	AK16(AJ16)	AJ15(AH15)	AK16(AJ16)	AJ15(AH15)
	AK17(AJ17)	AH16(AG16)							AL15(AK15)			
PLL7	T32(T31)	U32(U31)	—	(3)								
	T30(T29)	U30(U29)	—									
PLL8	T32(T31)	U32(U31)	—									
	T30(T29)	U30(U29)	—									
PLL9	U1(U2)	T1(T2)	—									
	U3(U4)	T3(T4)	—									
PLL10	U1(U2)	T1(T2)	—									
	U3(U4)	T3(T4)	—									
PLL11	A16(B16)	A17(B17)	A19(B19)					B18(C18)	D18(E18)	B18(C18)	D18(E18)	
	E16(F16)	C17(D17)						A19(B19)				
PLL12	AM17(AL17)	AM16(AL16)	AM19(AL19)	AL18(AK18)	AJ18(AN18)	AL18(AK18)	AJ18(AN18)					
	AK17(AJ17)	AH16(AG16)		AM19(AL19)								

**Notes to Table 8:**

- (1) D15, E15, AL15, AK15, A19, B19, AM19, and AL19 are used as either external clock outputs or for external feedback inputs. If the design uses external feedback input pins, you lose one (or two, if Fbin is differential) dedicated output clock pin.
- (2) PLL1 to PLL4, PLL5 to PLL10 are Fast PLLs; PLL5, 6, 11, 12 are Enhanced PLLs.
- (3) There are no dedicated external clock output pins for fast PLL. The fast PLL global or regional outputs can drive any I/O pins as external clock output pins.

**Table 9.** Dedicated I/O Pin Names for Package F1508 (Note 1)

Package F1508 (2)	Input Clocks			Output Clocks								
	Inclk		Fbin	C0-C3		C4-C5						
	P(N)	P(N)	P(N)	P(N)		P(N)						
PLL1	W39(W38)	Y39(Y38)	—	(3)		—						
	W37(W36)	Y37(Y36)										
PLL2	W39(W38)	Y39(Y38)										
	W37(W36)	Y37(Y36)										
PLL3	Y1(Y2)	W1(W2)										
	Y3(Y4)	W3(W4)										
PLL4	Y1(Y2)	W1(W2)										
	Y3(Y4)	W3(W4)										
PLL5	A20(B20)	C21(D21)						D18(E18)	A19(B19)	B18(C18)	A19(B19)	B18(C18)
	C19(D19)	C20(D20)							D18(E18)			
PLL6	AU20(AT20)	AW20(AV20)	AT18(AR18)	AW19(AV19)	AV18(AU18)	AW19(AV19)	AV18(AU18)					
	AU21(AT21)	AU19(AT19)		AT18(AR18)								
PLL7	W39(W38)	Y39(Y38)	—	(3)		—	—					
	W37(W36)	Y37(Y36)	—			—	—					
PLL8	W39(W38)	Y39(Y38)	—			—	—					
	W37(W36)	Y37(Y36)	—			—	—					
PLL9	Y1(Y2)	W1(W2)	—			—	—					
	Y3(Y4)	W3(W4)	—			—	—					
PLL10	Y1(Y2)	W1(W2)	—			—	—					
	Y3(Y4)	W3(W4)	—			—	—					
PLL11	A20(B20)	C21(D21)	D22(E22)			A21(B21)	B22(C22)	A21(B21)	B22(C22)			
	C19(D19)	C20(D20)				D22(E22)						
PLL12	AU20(AT20)	AW20(AV20)	AT22(AR22)	AW21(AV21)	AV22(AU22)	AW21(AV21)	AV22(AU22)					
	AU21(AT21)	AU19(AT19)		AT22(AR22)								

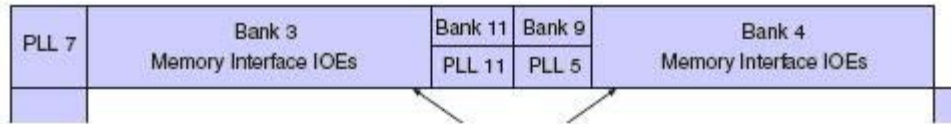
**Notes to Table 9:**

- (1) D18, E18, AT15, AR18, D22, E22, AT22, and AR22 are used as either external clock outputs or for external feedback inputs. If the design uses external feedback input pins, you lose one (or two, if Fbin is differential) dedicated output clock pin.
- (2) PLL1 to PLL4, PLL5 to PLL10 are Fast PLLs; PLL5, 6, 11, 12 are Enhanced PLLs.
- (3) There are no dedicated external clock output pins for fast PLL. The fast PLL global or regional outputs can drive any I/O pins as external clock output pins.

The dedicated clock input pins drive the clock networks directly, ensuring lower skew than other I/O pins. Use the dedicated routing network to have a predictable delay with less skew for high fan-out signals. In addition, dedicated input pins connect to specific PLLs, which can drive low skew routing networks. Analyze the global resource availability for each PLL and the PLL availability for each clock pin.

Selecting the appropriate PLLs to connect to the memory IOE and high-speed IOE is important for reducing clock skew. All memory interface I/O pins should connect to the closest PLLs. For example, [Figure 7](#) shows that if the DQ/DQS pins of HardCopy II device HC230 are selected to be in I/O bank 3, PLL11 or PLL7 should be used for this memory interface.

**Figure 7.** Connecting PLLs to the Memory and High-Speed IOE



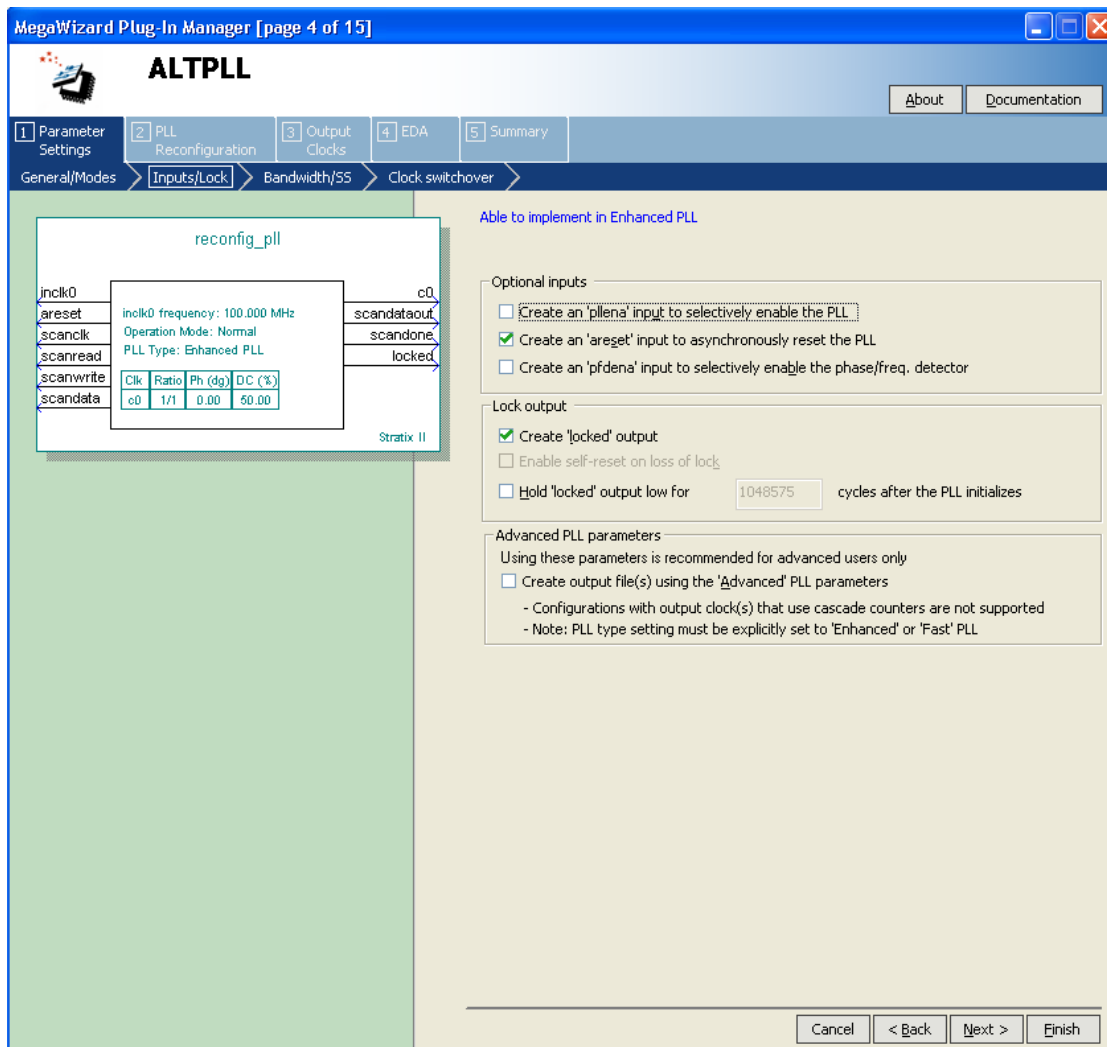
For information about PLL and clock management, refer to *PLLs in Stratix II and Stratix II GX Devices* in volume 2 of the *Stratix II Device Handbook*.

### PLL Reconfiguration

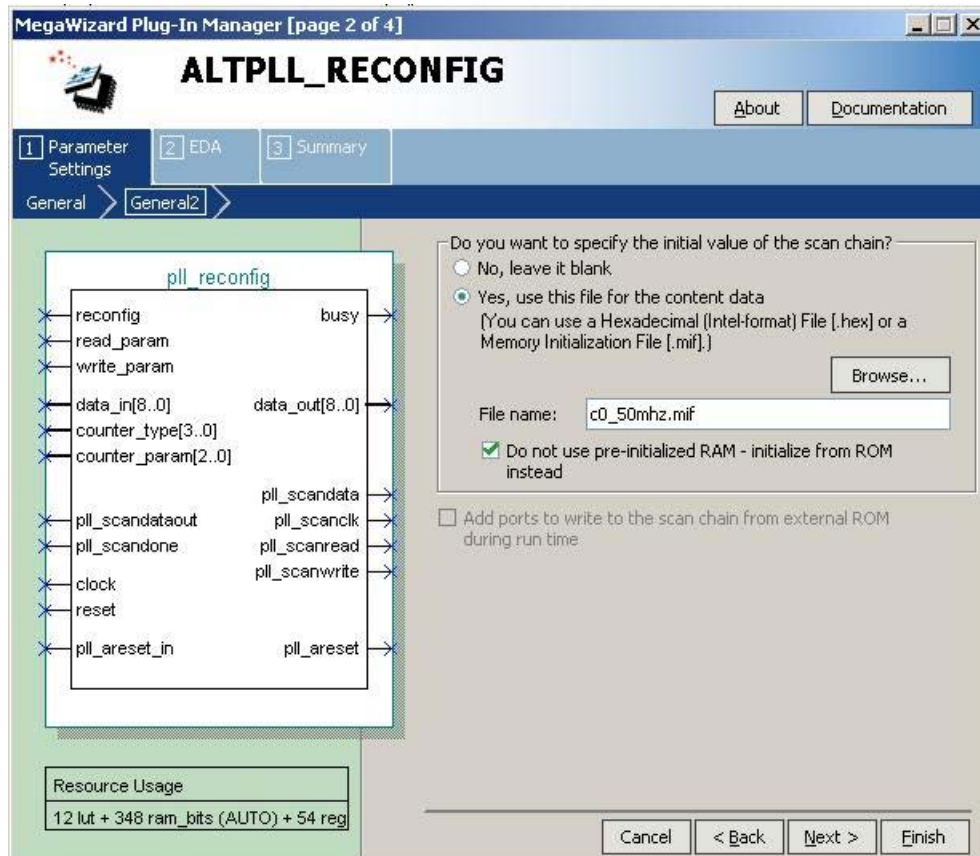
Altera HardCopy Design Center (HCDC) requires users to have PLL reconfiguration for HardCopy II devices if you use any memory interface. You must build the HardCopy II devices with PLL reconfiguration where possible. PLL reconfiguration allows you to adjust the PLL clock output frequency and fine-tune the output phase for optimal timing margin.

The ability to reconfigure the PLL is useful in applications that might operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output clock phase on the fly. For example, a system generating test patterns is required to generate and transmit patterns at 50 to 100 MHz, depending on the device being tested. Reconfiguring the PLL components in real time allows you to switch between two such output frequencies within a few microseconds. You can also use this feature to adjust clock-to-output delays by changing the output clock phase shift. For Stratix II devices, this approach eliminates the need to regenerate a configuration file with the new PLL settings. For HardCopy II devices, this feature avoids the need to re-spin the design.

To reconfigure the PLL, you should use the `altpll` MegaWizard Plug-In Manager to enable the PLL reconfiguration circuitry, which automatically adds the `scanclk`, `scanread`, `scanwrite`, `scandata`, `scandataout`, and `scandone` ports to the `altpll` instance as shown in [Figure 8](#).

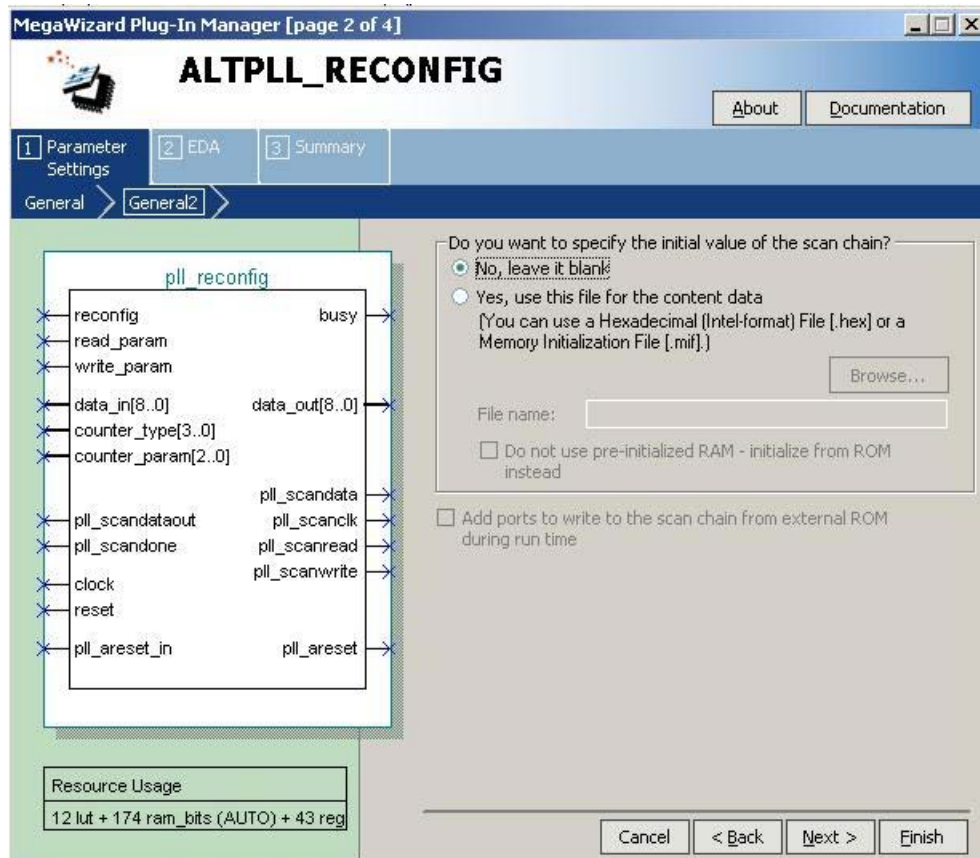
**Figure 8.** Enabling PLL Reconfiguration in the Quartus II MegaWizard Plug-In Manager

Using the `altpll_reconfig` megafunction simplifies the process of reconfiguring the PLLs on the fly. The initial configuration file, a memory initialization file (.mif), is generated by the MegaWizard Plug-In Manager to initialize the `altpll_reconfig` megafunction. Since HardCopy II devices do not support pre-initialized RAM, you can choose to initialize from ROM instead. **Figure 9** shows that the **Do not use pre-initialized RAM – initialize from ROM instead** option is specifically intended for HardCopy II devices. When the HardCopy II device powers up, the contents of ROM are copied to RAM, which is then used to load the PLL counters.

**Figure 9.** Check Box for Not Using Pre-initialized RAM Instead of ROM

Alternatively, you can choose to leave the initial value of the scan chain blank as shown in [Figure 10](#). If you make this choice, the device powers up with all the PLL counters programmed with zeroes, and it does not affect the PLL functionality for making this change.

Figure 10. Blank for Initial Value of the Scan Chain



For more information about unsupported pre-initialized RAM in HardCopy II devices, refer to the section [“Memory Blocks Planning” on page 32](#).

### PLL Settings for Stratix II and HardCopy II Devices

When you design for a Stratix II FPGA and a HardCopy II companion device, you may need different PLL settings for the two designs due to slightly different timing requirements. The different setting presents a problem for the HardCopy II companion revision comparison utilities, which report a failed comparison between the Stratix II FPGA and the HardCopy II device revisions.

To work around this problem, add the following `.qsf` assignment to the initial design (Stratix II FPGA first or HardCopy II ASIC first):

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE
<filename(s)>
```

This assignment should be added before creating the companion revision. After the companion revision is created, the PLL source files, shown as `<filename(s)>` above, identified in the `.qsf` assignment are copied and can be changed to the necessary PLL settings.


You need to modify the PLL source file manually or with the MegaWizard Plug-In Manager. In either case, the source file list in the `.qsf` for the companion revision must be updated to reflect the use of the new source file.

After updating the PLL source file in the companion revision, verify that the `.qsf` source file setting contains the newly modified PLL source file:

```
set_global_assignment -name <VHDL|VERILOG_FILE> <filename(s)>
```


Then compile your design. The new settings for the PLL will be used.

After compilation is completed, run the HardCopy II companion revision comparison utility to observe and track changes made to the PLLs and design settings. These changes are captured as critical warnings in the revision comparison report and must be reviewed before the design is accepted for migration.

 For information about the different PLL settings for Stratix II FPGAs and HardCopy II devices, refer to [AN 432: Using Different PLL Settings Between Stratix II and HardCopy II Devices](#).

## Memory Blocks Planning

HardCopy II memory blocks are functionally equivalent to Stratix II memory blocks. HardCopy II memory blocks can implement various Stratix II memory configurations, including simple and true dual port modes, FIFO, parity bits, ROM modes, and many other features.

 For more information about which Stratix II memory features can be implemented in the HardCopy II memory blocks, refer to the [Description, Architecture, and Features](#) chapter in volume 1 of the *HardCopy II Device Handbook*.

Two areas need to consideration for the HardCopy II memory resource planning:

- HardCopy II devices do not support M512 memory blocks
- HardCopy II devices cannot pre-load M4K memory blocks with a `.mif` when used as RAM

[Table 10](#) shows all the memory block offerings when compiling for a Stratix II FPGA in conjunction with a HardCopy II companion device. Use [Table 10](#) as a guide when optimizing memory requirements for selected Stratix II and HardCopy II pairs.

**Table 10.** HardCopy II Embedded Memory Resources

Feature	HC210W	HC210	HC220	HC230	HC240
M512 blocks (512 bits) <i>(1)</i>	—	—	—	—	—
M4K RAM blocks (4 Kbits)	190	190	408	614	768
M-RAM blocks (512 Kbits)	0	0	2	6	9
Total RAM bits (bits)	875,520	875,520	3,059,712	6,368,256	8,847,360

**Note to Table 10:**

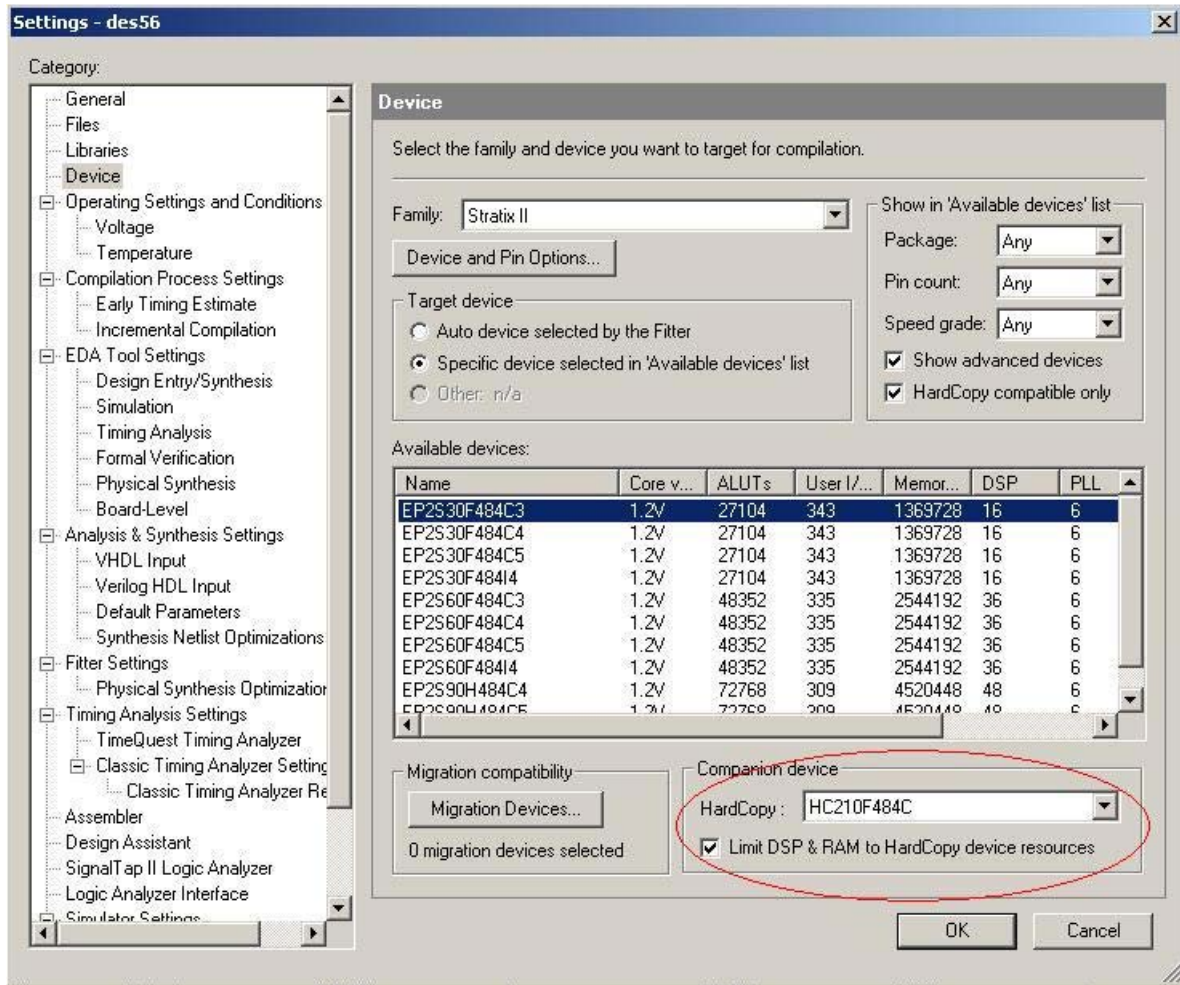
(1) HardCopy II devices do not support M512 memory blocks.

### Unsupported M512 Memory Blocks

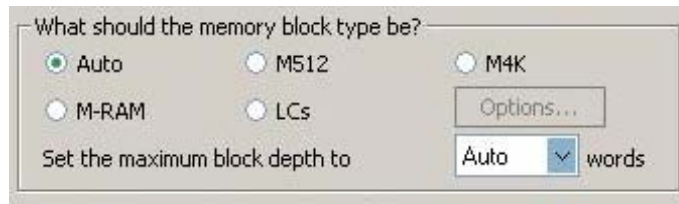
HardCopy II devices do not support M512 blocks. Use the following approaches to achieve memory design requirements:

1. When you compile a Stratix II design with the HardCopy II companion device selected in the Quartus II software, you must check the **Limit DSP & RAM to HardCopy Device Resources** box in the **Device Settings** dialog box (Assignment menu). This automatically restricts the available memory blocks for the design to those that are common to the Stratix II device and the HardCopy II device. When you select a Stratix II device and HardCopy II companion device in the Quartus II software, the **Limit DSP & RAM to HardCopy Device Resources** checkbox is turned on by default as shown in [Figure 11](#).

**Figure 11.** Limit DSP and RAM to HardCopy II



2. You can use M4K memory blocks in the HardCopy II design to implement memory designs instead of M512 blocks. In this approach, the Quartus II software offers several memory implementation options, one of which allows the memory to be implemented with M4K blocks. When using the Quartus II MegaWizard Plug-In Manager to configure the megafunction, Altera recommends selecting the **Auto** option to allow the Quartus II software to determine how the design is implemented in the memory blocks as shown in [Figure 12](#). This allows the Quartus II software to optimize memory selection based on memory size and placement requirements in the available memory blocks of the selected Stratix II and HardCopy II companion pair.

**Figure 12.** Quartus II Megafunction RAM Selection

3. You can use logic cells in the megafunction to implement small memory blocks in your design. This implements the memory design in Stratix II ALMs or HardCopy II HCells. However, there may be power and performance trade-offs when choosing between an M4K or M-RAM block or using the ALMs (or HCells). HardCopy II devices power down unused M4K blocks, M-RAM blocks, and HCells.



Implementing memory block using logic cells (LCs), as shown in [Figure 12](#), allows you to select a memory implementation functionally equivalent to M512 blocks or a non-equivalent option to save resources. Altera recommends setting the option to a functionally equivalent version with the M512 blocks. You must implement memory blocks using LCs for both Stratix II and HardCopy II companion device, or else it will trigger a Revision Compare failure later on.

For very small memory implementations such as 8×16 single port RAM, the M4K or M-RAM blocks will be under-used, and may be less power efficient than a small number of HCells. If you select the logic cell option, only a fraction of ALMs are required in the Stratix II device, which translates into a small number of HCells used in the HardCopy II device. However, when performance is a key factor, or your design requires ALMs to implement other logic, it may be more efficient to use M4K blocks. Altera recommends using the Quartus II software to analyze performance trade-offs between the given options.

### M4K Memory Initialization File

You cannot pre-load HardCopy II M4K blocks with a `.mif` when they are configured as RAM because that feature is not supported in HardCopy II devices. Also, unlike Stratix II devices, the HardCopy II M4K RAM contents and their output registers are unknown after power up. However, if the HardCopy II M4K block is designated as ROM, it powers up with the ROM contents. When designing M4K blocks as RAM, Altera recommends writing to the block before reading from it to avoid reading unknown initial power-up data.

### M4K and M-RAM Power Optimization

M4K and M-RAM memory blocks in a HardCopy II device have a one-to-one mapping from the Stratix II M4K and M-RAM resources. Therefore, HardCopy II M4K and M-RAM memory blocks share the same functionality as Stratix II M4K and M-RAM memory blocks. One key feature with HardCopy II M4K and M-RAM memory blocks is power optimization when the M4K and M-RAM memory blocks are not used. Unused M4K and M-RAM memory blocks in a HardCopy II device are disconnected from the power rails, optimizing overall power consumption.

## DSP Blocks Planning

Stratix II FPGAs have dedicated DSP blocks to implement various DSP functions. Stratix II DSP blocks consist of multipliers, an adder/subtractor/accumulator and a summation block, input and output interfaces, and input and output registers. During a HardCopy II migration, DSP block functions are implemented using HCells instead of dedicated DSP blocks as they are within a Stratix II FPGA. The total number of DSP blocks is dependent on the Stratix II device selected. HardCopy II devices will match the available DSP blocks in the Stratix II device. Table 11 lists the available DSP implementations based on the selected Stratix II device.

**Table 11.** DSP Multiplier Availability for Stratix II and HardCopy II Companion Devices

Stratix II Device	HC210W			HC210			HC220			HC230			HC240		
	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36	9 × 9	18 × 18	36 × 36
EP2S30	128	64	16	128	64	16	—	—	—	—	—	—	—	—	—
EP2S60	288	144	36	288	144	36	288	144	36	—	—	—	—	—	—
EP2S90	384	192	48	384	192	48	384	192	48	384	192	48	—	—	—
EP2S130	—	—	—	—	—	—	504	252	63	504	252	63	—	—	—
EP2S180	—	—	—	—	—	—	—	—	—	768	384	96	768	384	96

The HardCopy II DSP implementation is functionally equivalent to Stratix II DSP blocks and all features are supported except for dynamic-mode switching. Dynamic-mode switching allows the DSP block to operate among the following three modes:

- Up to four 18-bit independent multipliers
- Up to two 18-bit multiplier-accumulators
- One 36-bit multiplier

## HardCopy II ASIC Development Flow

In the Quartus II software, two methods are available for the HardCopy II development flow: Stratix II device first flow and HardCopy II device first flow.

- Stratix II device first flow — Design the Stratix II device first for system functional verification, and then create the HardCopy II ASIC companion device. Performing system verification early helps reduce the overall total project development time.
- HardCopy II device first flow — Design the HardCopy II ASIC first, and then create the Stratix II companion device for system functional verification. This method predicts more accurately the maximum performance of the HardCopy II device during development. If you optimize your design to maximize HardCopy II performance but are unable to meet your performance requirements with the Stratix II FPGA, you can still migrate your design with decreased performance requirements for in-system verification.

Whichever design flow you choose for your HardCopy II development, both the target design and the companion device design must be in one Quartus II project.

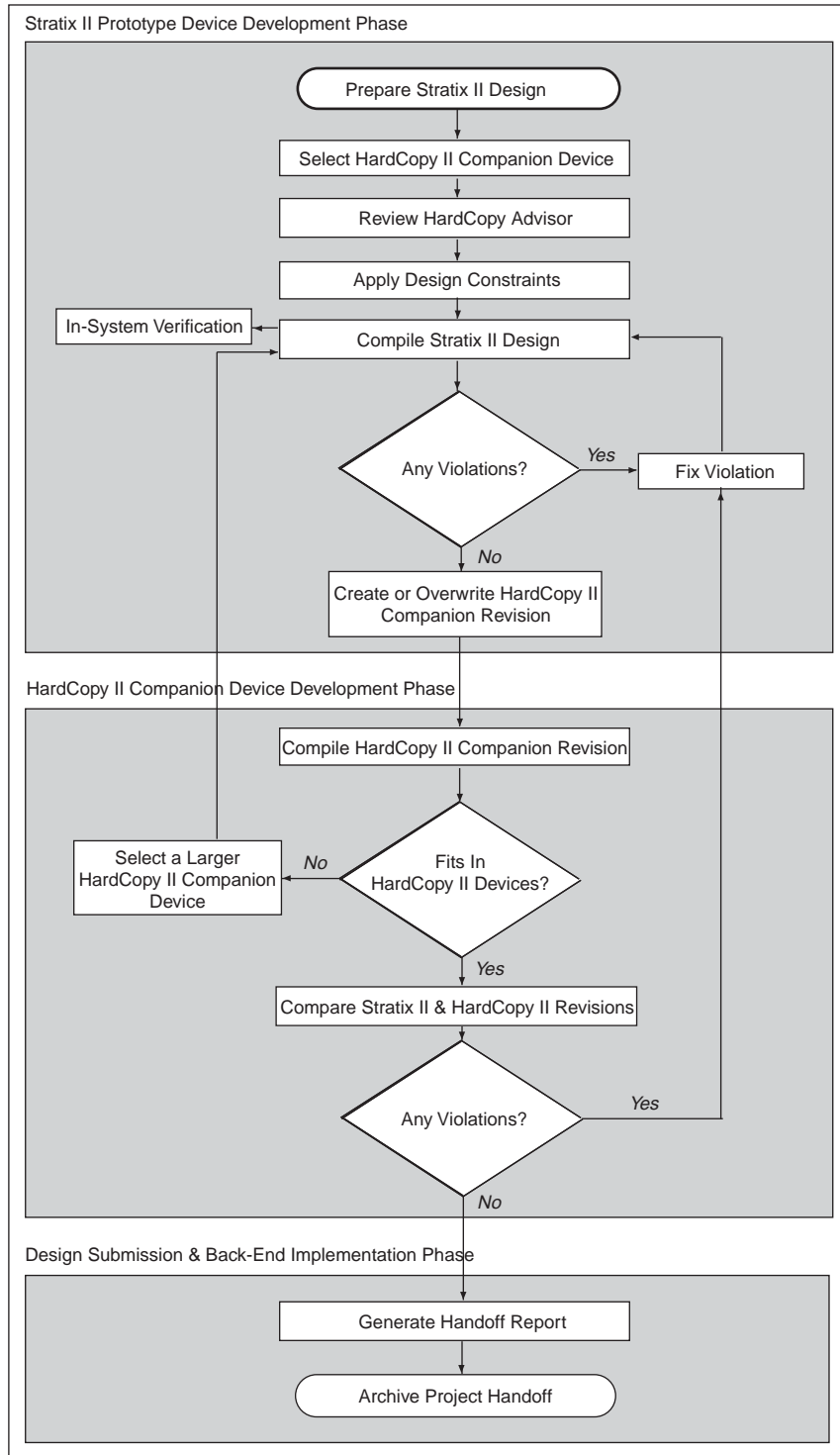
## Designing with the Stratix II Device First Flow

The HardCopy II development flow beginning with the Stratix II FPGA prototype is very similar to a traditional Stratix II FPGA design flow, but requires a few additional tasks be performed to migrate the design to the HardCopy II companion device. To design your HardCopy II device using the Stratix II FPGA as a prototype, complete the following tasks:

- Specify a HardCopy II device for migration
- Compile the Stratix II FPGA design
- Create and compile the HardCopy II companion revision
- Compare the HardCopy II companion revision compilation to the Stratix II device compilation

Figure 13 provides an overview highlighting the development process for designing with a Stratix II FPGA first and creating a HardCopy II companion device second.

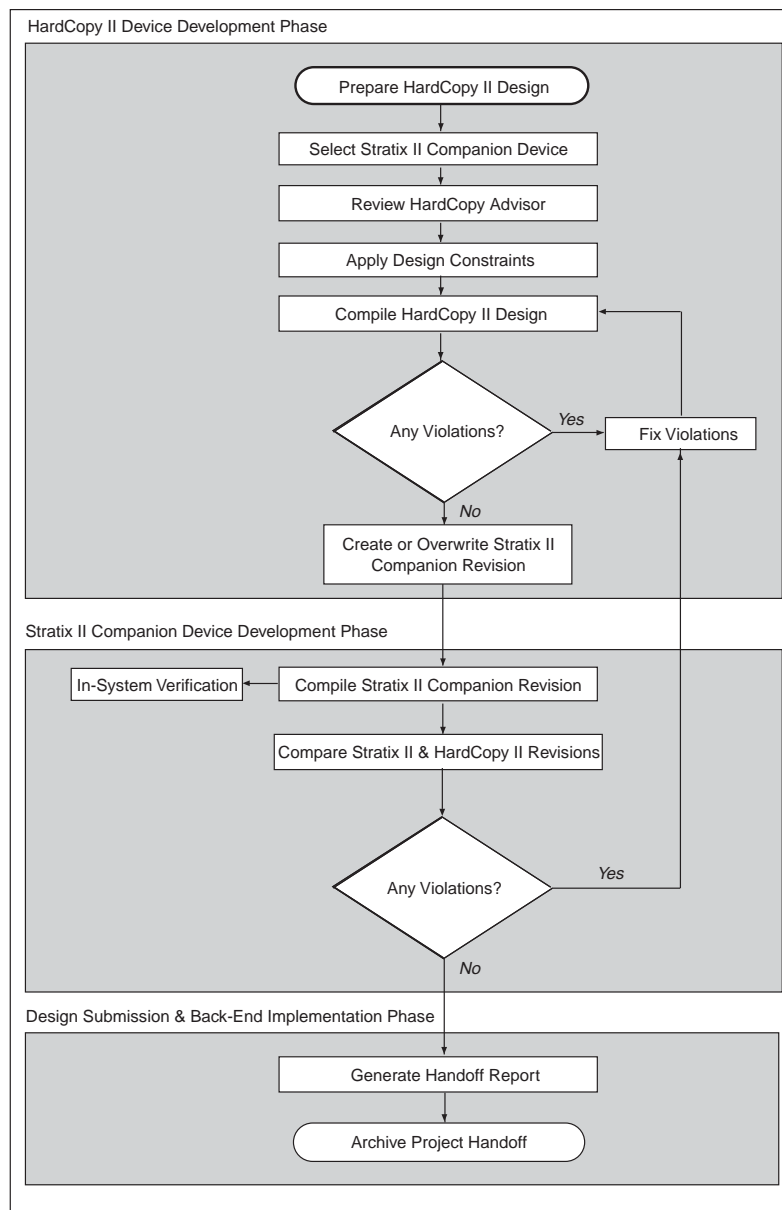
Figure 13. Designing with the Stratix II Device First Flow



## Designing with the HardCopy II Device First Flow

You can design your HardCopy II device first and create your Stratix II FPGA prototype second in the Quartus II software. This allows you to maximize performance in the HardCopy II device and migrate the design to the Stratix II FPGA prototype for in-system verification. The performance of the Stratix II prototype may be less than the HardCopy II device. This design process is similar to Stratix II FPGA first flow, but you must select HardCopy II as the target device and Stratix II as the companion device in the Device Settings dialog box. The remaining tasks to complete your design for both Stratix II and HardCopy II devices are outlined in [Figure 14](#). The HardCopy Advisor adjusts its list of tasks based on the device family you start with in order to guide you through the development process.

**Figure 14.** Designing with the HardCopy II Device First Flow



## HardCopy Advisor

In the HardCopy II development flow, the HardCopy Advisor guides you through a sequence of recommendations and actions. You can track your design progress, generate the design, and complete the comparison archiving and handoff file that you send to the Altera HardCopy Design Center.

 To run the HardCopy Advisor, on the Project menu, point to **HardCopy Utilities** and click **HardCopy Advisor**.

**Figure 15.** HardCopy Advisor in Quartus II Software

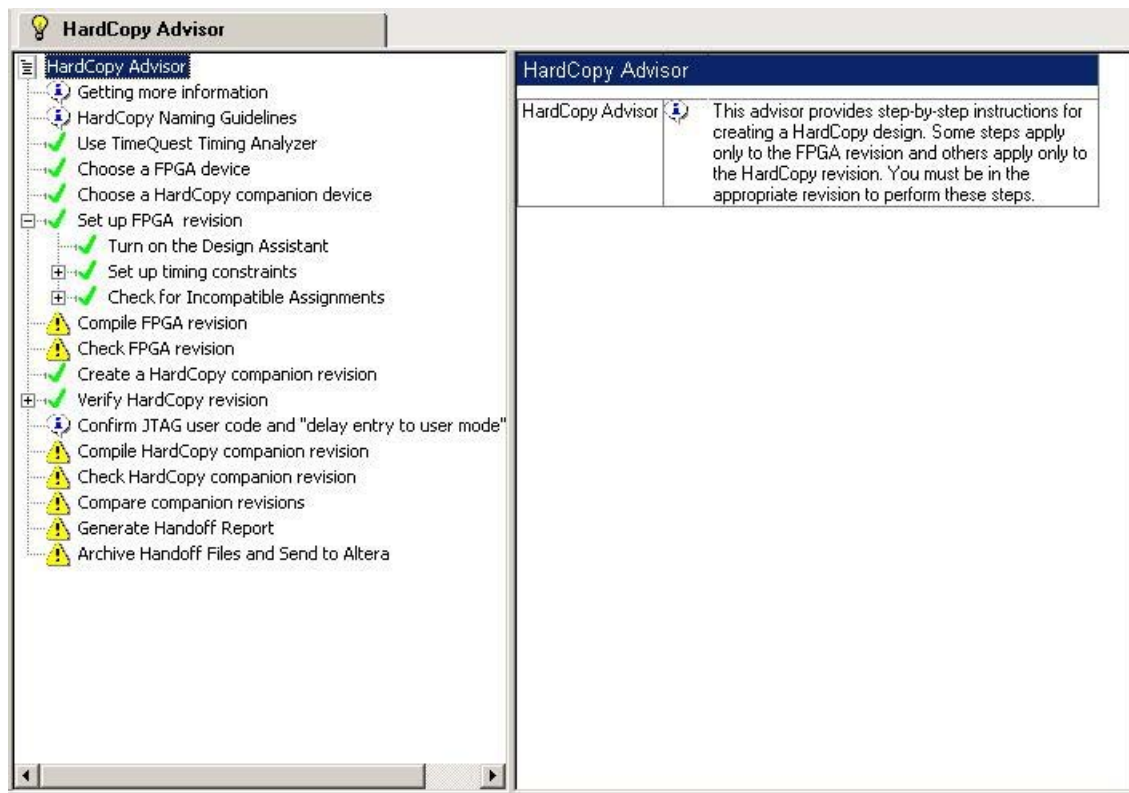


Figure 15 shows the HardCopy Advisor window for the Stratix II device first flow. It provides the list of tasks you should follow to develop your Stratix II prototype and HardCopy II companion design. Table 12 provides a list of the HardCopy Advisor's tasks along with recommendations for each task. This table guides you through a series of recommendations for developing a Stratix II design prototype and HardCopy II device. You can also run the HardCopy Advisor anytime during the development flow. All required tasks should be green with a check mark in the Quartus II software.

**Table 12.** Required Tasks in the Quartus II Software (Part 1 of 2)

Tasks	Recommendation
Use TimeQuest Timing Analyzer	The TimeQuest Timing Analyzer's increased power and flexibility enables you to constrain more complex designs, especially those with complex clock schemes including clock muxing or source synchronous clock schemes. TimeQuest uses the same timing paradigm and Synopsys Design Constraint syntax as Synopsys PrimeTime, allowing a smooth migration to final layout.
Choose a Stratix II FPGA/HardCopy II device	There are two HardCopy II development flows. For the Stratix II device first flow, you must create a design for a Stratix II FPGA before migrating to a HardCopy II device. After you have successfully compiled for the Stratix II FPGA, you can migrate to a HardCopy II device.  For the HardCopy II device first flow, you must choose a HardCopy II companion device for migration. You must choose a specific Stratix II FPGA if you did not do so in the previous step. Auto device is not supported for migration. After you have successfully compiled for the Stratix II FPGA, you can migrate to a HardCopy II device.
Design Assistant enabled	Altera requires all HardCopy II designs to be checked for design rule violations using the Quartus II Design Assistant. You must run the Design Assistant for all HardCopy II designs and all Critical and High level errors must be fixed before submitting your design to Altera's HardCopy Design Center.
Assembler enabled	All HardCopy II designs must be prototyped in a Stratix II FPGA before submitting for conversion.
HardCopy Design Readiness Check enabled	Altera requires all HardCopy II designs to be checked for I/O assignments using the HardCopy Design Readiness Check flow. You must run the HardCopy Design Readiness Check flow for all HardCopy II designs, and all I/Os without I/O assignments must be fixed before submitting your design to the Altera HardCopy Design Center.
Timing settings enabled	You must enable hold time optimization along all paths in the Fitter, allowing the Fitter to add delay to the appropriate paths, including internal core transfers. Set the Optimize Fast Corner Timing option to successfully enable optimizations of the hold time.  Enable fast-corner timing optimizations to tell the Fitter to optimize the design to meet timing at the Fast Timing process corner and operating condition, as well as at the Slow Timing process corner and operating condition. Turning this option ON helps create a design implementation that is more robust across process, temperature, and voltage variations.  Enable multicorner analysis to direct the TimeQuest Timing Analyzer to perform multicorner timing analysis, which analyzes the design against best-case and worst-case operating conditions. Turning this option ON helps to verify that the design implementation is more robust across process, temperature, and voltage variations.
Incompatible assignments	This setting reserves all unused pins on the target device as tri-stated inputs with weak pull-ups.
Current revision compiled	Compile the design and verify it fits in the selected Stratix II FPGA device.
Companion revision created	Verify that the specified companion HardCopy II device is compatible with the design, Design Assistant passes with no errors, the timing requirements are successfully met and all paths are timing constrained, and I/O types are fully defined for all the I/O pins.

**Table 12.** Required Tasks in the Quartus II Software (Part 2 of 2)

Tasks	Recommendation
JTAG user code and delay entry to user mode settings	Altera HardCopy Design Center uses this information to determine how long to wait for power up to enter user mode and what JTAG user code is applied to this design. These settings cannot be changed after the devices have been taped out.
Companion revision compiled	Compile the design and verify it in the selected HardCopy II device. Verify timing requirements are successfully met, all paths are timing constrained, Design Assistant passes with no errors, and the specified companion HardCopy II device is compatible with the design.
Comparison of revisions completed	For a project to be considered for HardCopy II conversion, it must have both the Stratix II FPGA and the HardCopy II revisions. These revisions are linked together and are called "Companion Revisions". The revisions must be synchronized and must not have any issues that would cause a problem for the HardCopy II conversion. To check if the companion revisions are compatible, you must run a command to compare the revisions.
Handoff report created	After your design is done and both companion revisions have been compared successfully, generate a handoff report for a final review.
Archive created	After your design is done and both companion revisions have been compared successfully, archive your handoff files and send the archive files to the HardCopy Design Center for the design conversion.

## Device Migration

When you compile a design targeting a HardCopy II device, you must select a target Stratix II device and a HardCopy II companion device for compilation in the Quartus II software. The Quartus II Compiler constrains the overall design's I/O pins and other resource assignments to the resources available in the selected HardCopy II device. This process allows migration between devices using the same package footprint. For example, if your design targets the EP2S130 device in the 1,020-pin FineLine BGA® package, the Quartus II software provides the EP2S90 and EP2S180 devices in the 1,020-pin FineLine BGA package as migration options, as well as the HC230 device in the 1,020-pin FineLine BGA package. [Table 13](#) shows migration options by package.

**Table 13.** Stratix II and HardCopy II Migration Options

Device	FineLine BGA Package						
	484 Pins		672 Pins	780 Pins	1,020 Pins	1,020 Pins	1,508 Pins
HardCopy II	HC210W	HC210	HC220	HC220	HC230	HC240	HC240
Stratix II	EP2S30	EP2S30	EP2S60	EP2S90	EP2S90	EP2S180	EP2S180
	EP2S60	EP2S60	—	EP2S130	EP2S130	—	—
	EP2S90 (1)	EP2S90	—	—	EP2S180	—	—

**Note to Table 13:**

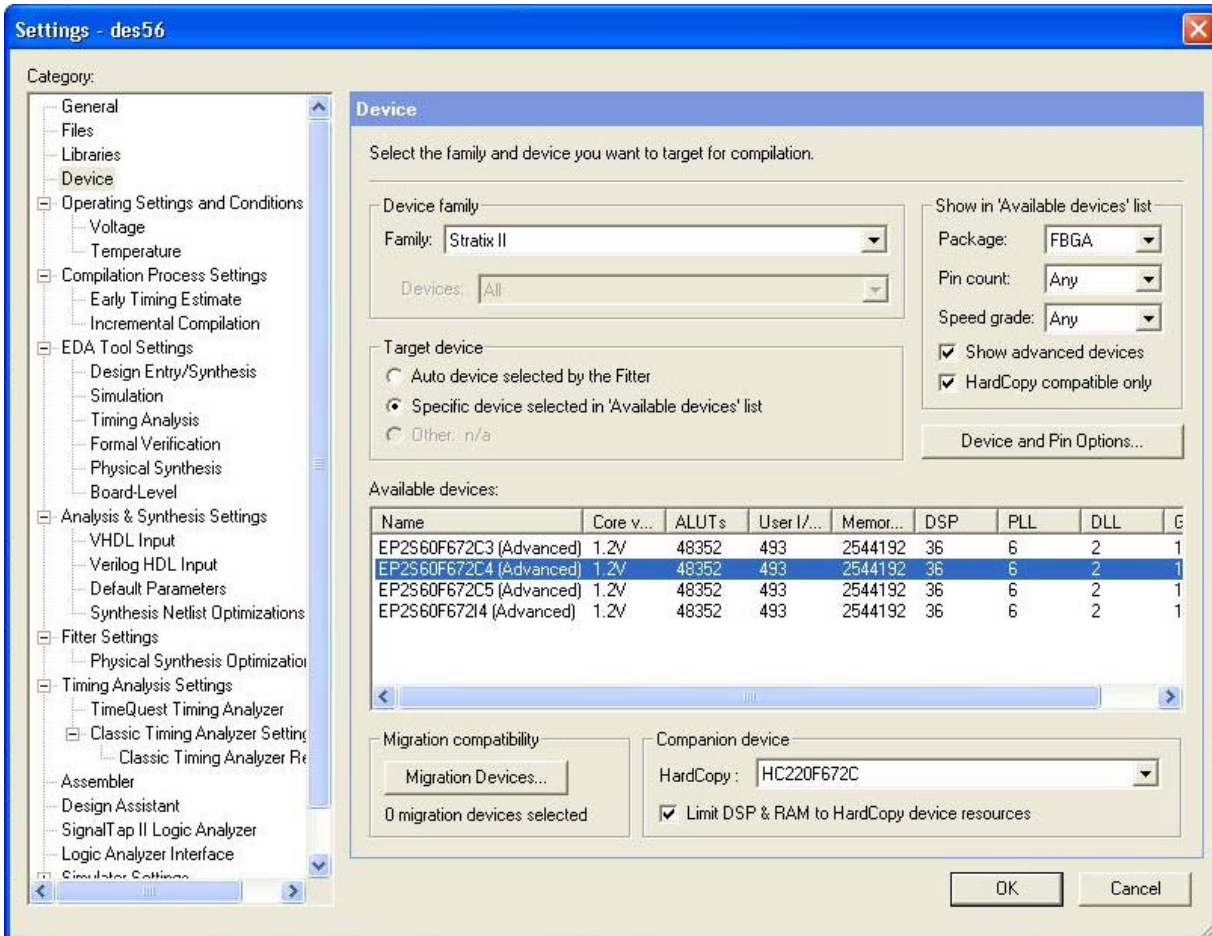
- (1) This is a Hybrid FineLine BGA package. For more details, refer to the [Package Information for Stratix II & Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II Device Handbook*.



To specify the target migration devices, on the Assignments menu, click **Device** and in the **Settings** dialog box, select **Migration Devices**.

[Figure 16](#) shows the proper settings for the **Settings** dialog box in the Quartus II software.

Figure 16. Quartus II Device Settings

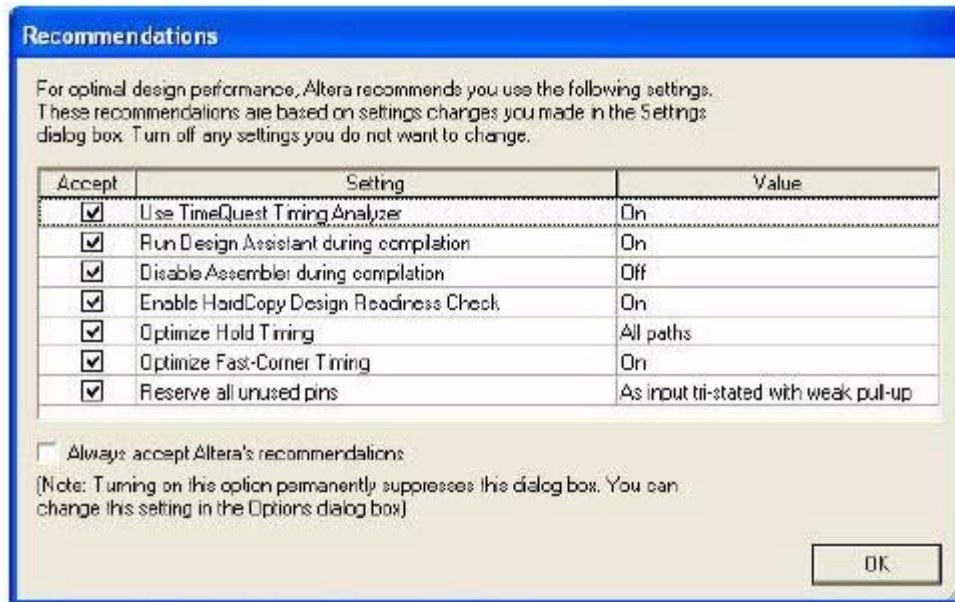


## Quartus II Settings for HardCopy II ASIC Development

The HardCopy II development flow involves additional planning and preparation in the Quartus II software compared to a standard FPGA design. This is because you are developing your design to be implemented in two devices: a Stratix II FPGA for prototyping and a HardCopy II ASIC for volume production. You need to consider the HardCopy II development flow and additional settings and constraints to make the design work in both the Stratix II FPGA and the HardCopy II device. In some cases, you must remove certain settings in your design to ensure compatibility. This section explains the additional settings and constraints necessary for your design to work successfully in both Stratix II FPGA and HardCopy II devices.

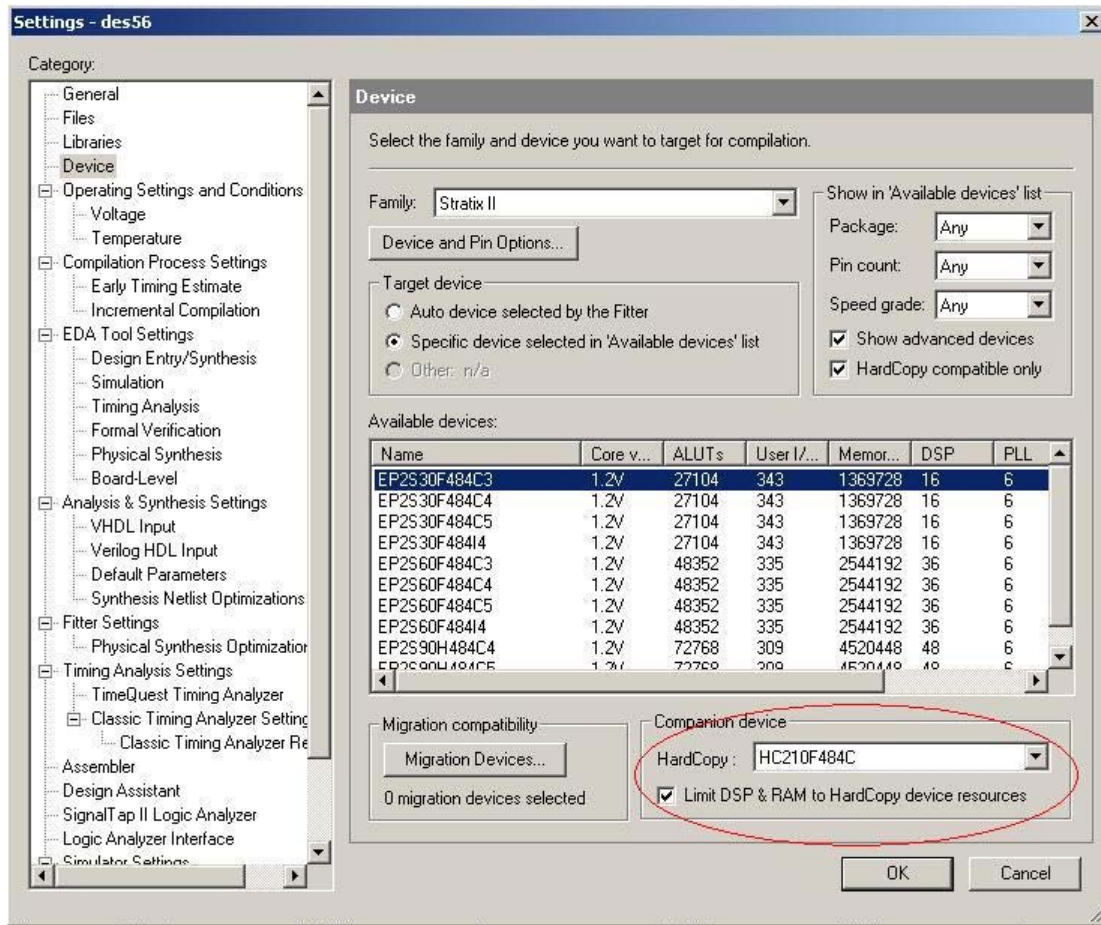
When you create the project for the Stratix II FPGA and the HardCopy II companion device, the **Recommendations** dialog box appears with the recommended settings, as shown in Figure 17. You should review and accept the recommendations provided by the Quartus II software.

Figure 17. Quartus II Recommended Settings



### Limit DSP and RAM to HardCopy Device Resources

To maintain compatibility between the Stratix II FPGA and HardCopy II devices, your design must use resources that are common to both devices. The Quartus II software setting **Limit DSP & RAM to HardCopy Device Resources** must be turned on by default before compiling the Stratix II FPGA. This prevents the Quartus II software from using resources in the Stratix II device that are not available in the HardCopy II device. Figure 18 shows the appropriate setting to select in the **Companion device**.

**Figure 18.** Limit DSP and RAM to HardCopy II Device Resources Check Box

- ☞ The Altera HardCopy Design Center requires that you compile your final Stratix II FPGA and HardCopy II designs with the **Limit DSP & RAM to HardCopy Device Resources** setting turned on before submitting to Altera HardCopy Design Center for back-end implementation.

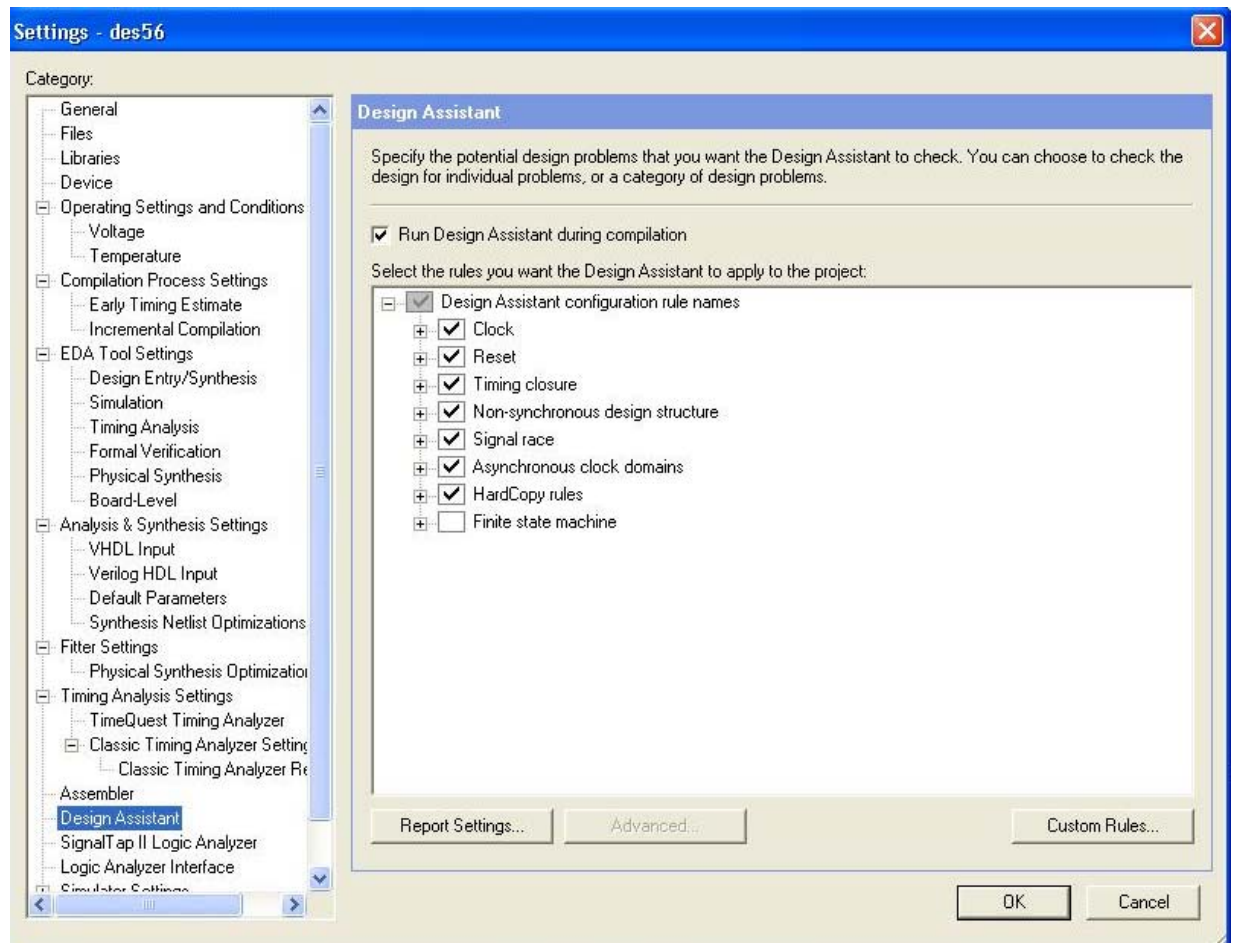
## Enable Design Assistant to Run During Compile

You must use the Quartus II Design Assistant to check for design rule violations before submitting the design to the Altera HardCopy Design Center. Additionally, you must fix all critical and high-level errors reported by the Quartus II Design Assistant. Altera recommends turning on the Design Assistant to run automatically during development.

- ☞ To enable the Design Assistant to run during compilation, on the Assignments menu, click **Settings**. In the **Category** list, select **Design Assistant** and turn on **Run Design Assistant during compilation** (Figure 19).

- For more information about the Design Assistant and its warnings, refer to the *Design Recommendations for Altera Devices and the Quartus II Design Assistant* chapter in volume 1 of the *Quartus II Software Handbook*.

Figure 19. Enabling the Design Assistant



## I/O Assignments Settings

Due to the complex rules governing the use of I/O cells and their availability for specific pins and packages, Altera highly recommends that I/O assignments be completed using the Pin Planning tool and the Assignment Editor in the Quartus II GUI. These tools ensure that all of the rules regarding each pin and I/O cell are applied correctly. The Quartus II GUI can export a .Tcl script containing all I/O assignments.


For more information about I/O location and type assignments using the Quartus II Assignment Editor and Pin Planner tools, refer to [“Pin Planning with the Quartus II Software”](#) on page 12.

To ensure the HardCopy II migration is successful, you must make accurate I/O assignments that include pin locations, I/O standards, drive strengths and capacitance loading for the design. It is also important to make sure the I/O assignments are compatible with all selected devices. Altera recommends that you do not leave any I/O with an unassigned I/O assignment.

## Timing Settings

Beginning with Quartus II software version 7.1, all HardCopy II ASIC designs must use TimeQuest Timing Analyzer as the timing analysis tool. The TimeQuest Timing Analyzer is a complete static timing analysis tool for Altera FPGAs and HardCopy II ASICs. The Altera HardCopy Design Center does not accept any designs that use Classic Timing Analyzer for timing closure.

If you are still using the Classic Timing Analyzer, you must switch to the TimeQuest Timing Analyzer during HardCopy II ASIC development.

 For information about how to switch to TimeQuest, refer to the *Switching to the Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

When you specify the TimeQuest Timing Analyzer as the timing analysis tool, the TimeQuest Timing Analyzer guides the Quartus II Fitter and analyzes the timing results during each Stratix II FPGA and HardCopy II design compilation.

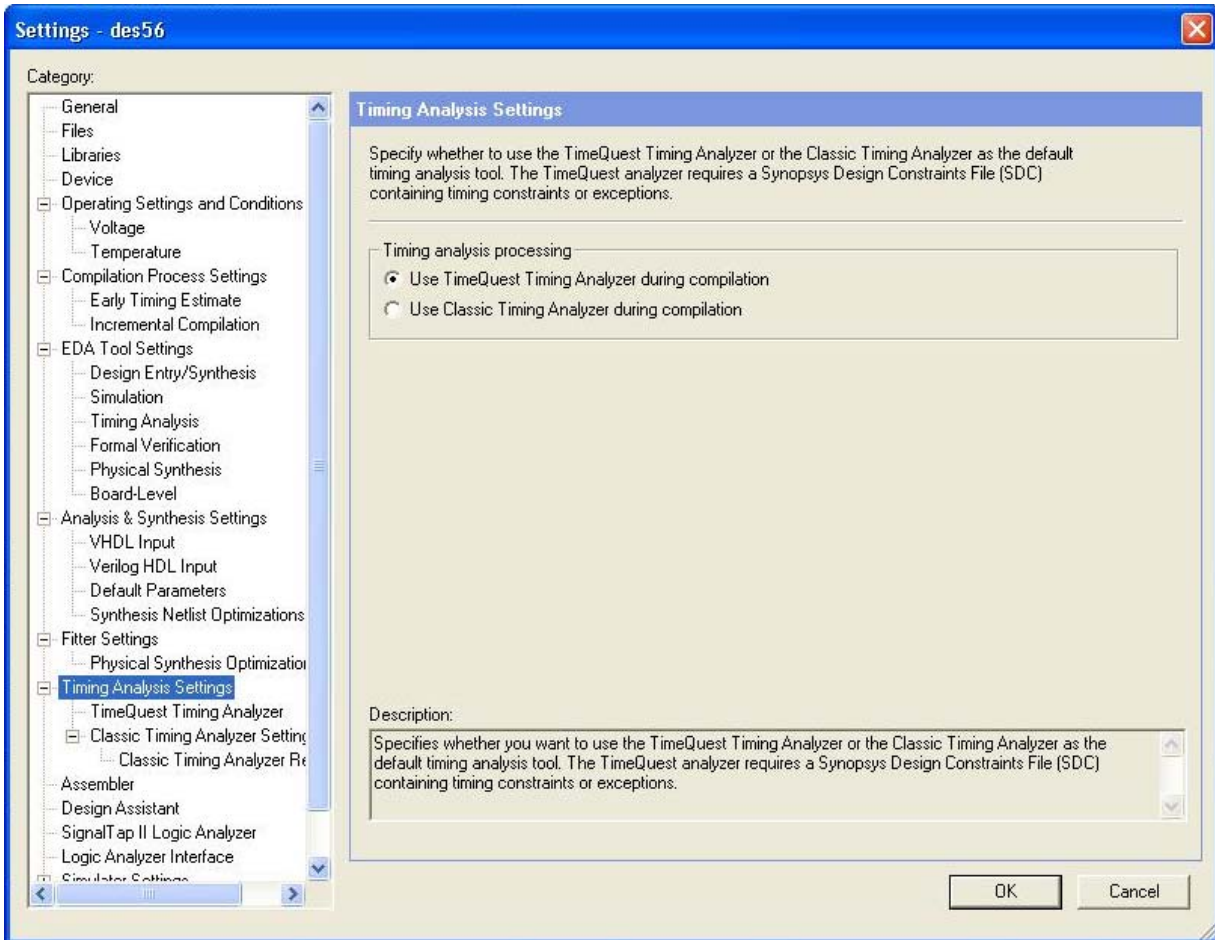
For information about how to set the Quartus II Fitter to use timing driven compilation, refer to “*HardCopy II Fitting*” on page 53.

### Setting Up the TimeQuest Timing Analyzer

You must use the TimeQuest Timing Analyzer during compilation for the HardCopy II development flow. To use the TimeQuest Timing Analyzer, follow these steps:

1. On the Assignments menu in the Quartus II software, click **Settings**.
2. In the **Category** list, select **Timing Analysis Settings**. In the **Timing Analysis Settings** window, select **Use TimeQuest Timing Analyzer during compilation**.

*Figure 20* shows the appropriate compilation setting for the HardCopy II design flow.

**Figure 20.** Setting the TimeQuest Timing Analyzer in the Quartus II Software

### TimeQuest Timing Analyzer

The TimeQuest Timing Analyzer is a powerful ASIC-style timing analysis tool that validates timing in your design by using industry-standard constraint, analysis, and reporting methodology. You can use the TimeQuest Timing Analyzer's GUI or command-line interface to constrain, analyze, and report results for all timing paths in your design.

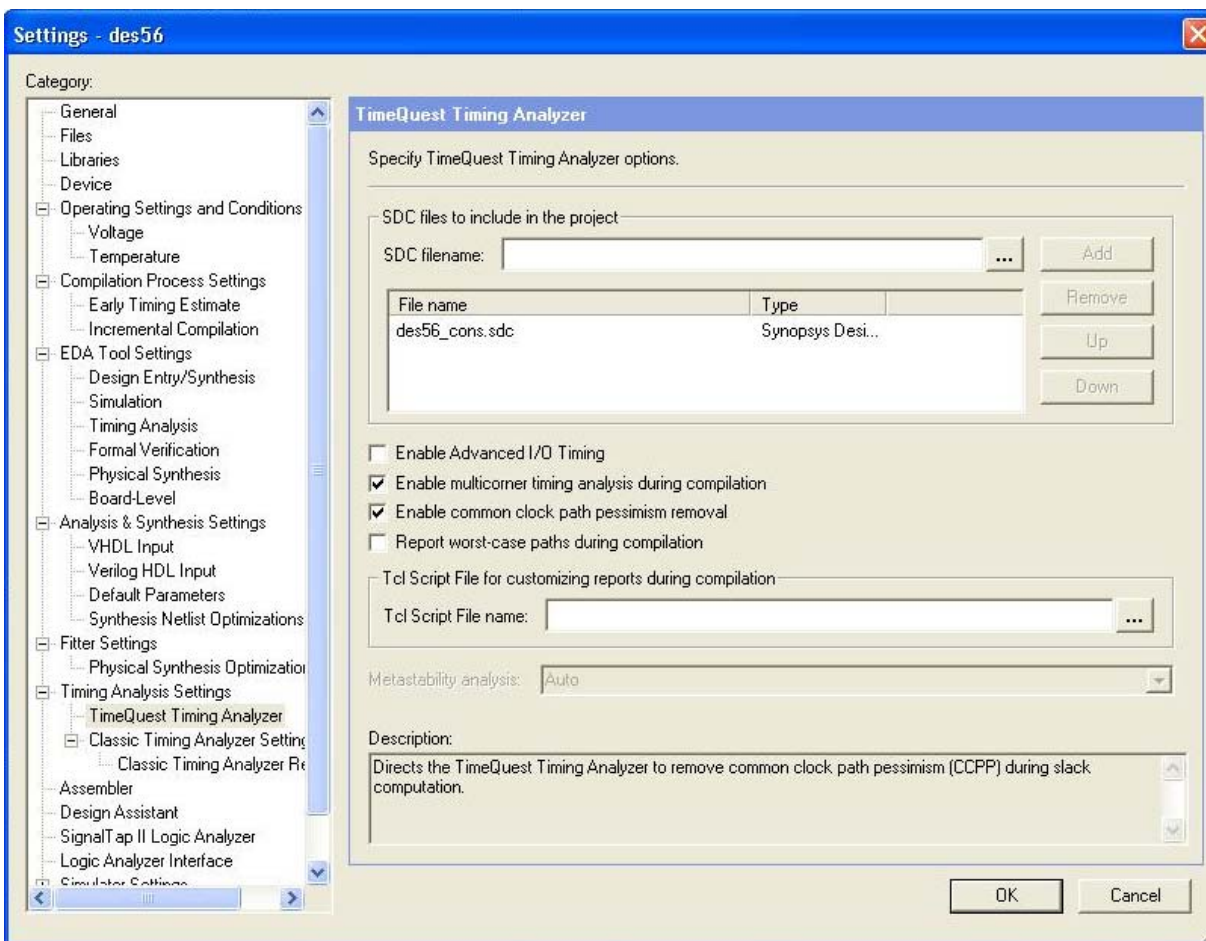
Before running the TimeQuest Timing Analyzer, you must specify initial timing constraints that describe the clock characteristics, timing exceptions, and signal transition arrival and required times. You can specify timing constraints in the Synopsis Design Constraints (.sdc) file format using the GUI or command-line interface. The Quartus II Fitter optimizes the placement of logic to meet your constraints.

During timing analysis, the TimeQuest Timing Analyzer analyzes the timing paths in the design, calculates the propagation delay along each path, checks for timing constraint violations, and reports timing results as slack in the **Report** panel and in the **Console** panel. If the TimeQuest Timing Analyzer reports any timing violations, you can customize the reporting to view precise timing information about the specific paths, and then constrain those paths to correct the violations. When your design is free of timing violations, you can be confident that the logic will operate as intended in the target device.

For more information about how to create .sdc file format timing constraints, refer to [“Timing Closure and Verification” on page 57](#).

### **TimeQuest Multicorner Timing Analysis Setting**

The Altera HardCopy Design Center requires that all HardCopy handoff files include a TimeQuest timing report for design review. From the TimeQuest timing report, you must include both fast-timing and slow-timing corner timing analysis for setup, hold and I/O paths. To do this, you must turn on **enable multicorner timing analysis during compilation** on the **TimeQuest Timing Analyzer** page under **Timing Analysis Settings** in the Quartus II software. This option directs TimeQuest to analyze the design and generate slack reports for the slow and fast corners, as shown in [Figure 21](#).

**Figure 21.** TimeQuest Multicorner Timing Analysis Settings

## Quartus II Software Features Supported for HardCopy II ASICs

The Quartus II software supports optimization features for HardCopy II prototype development, including:

- Physical Synthesis Optimization
- LogicLock Regions
- Incremental Compilation
- PowerPlay Power Analyzer
- HardCopy II Fitting

### Physical Synthesis Optimization

Physical Synthesis optimizations take place during the Fitter stage of the Quartus II compilation flow. These optimizations make placement-specific changes to the netlist that improve performance results for a specific Altera device.

When a design is migrated to a HardCopy II device, you can target Physical Synthesis optimizations to the Stratix II FPGA architecture in the Stratix II device first flow. The optimizations are mapped to the HardCopy II device architecture during the migration process. Note that you cannot target optimizations to optimize for both the Stratix II FPGA and HardCopy II device architectures individually because doing so would result in a different post-fitting netlist for each device. Physical Synthesis can be run on individual partitions within the originating device only. The resulting optimizations are preserved in the migration to the companion device.

To enable Physical Synthesis optimizations for the Stratix II FPGA revision of the design, follow these steps:

1. On the Assignments menu, click **Settings**.
2. In the **Settings** dialog box, in the **Category** list, select **Fitter Settings**. These optimizations are migrated into the HardCopy II companion revision for placement and timing closure.

When designing with a HardCopy II device first, Physical Synthesis optimizations can be enabled for the HardCopy II device, and these post-fit optimizations are migrated to the Stratix II FPGA revision.



For information about physical synthesis for fitting and performance, refer to the *Netlist Optimizations and Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

## LogicLock Regions

LogicLock regions are user-defined rectangular regions within the device. A LogicLock region is defined by its size (height and width) and location (where the region is located on the device). It can be used to create a floorplan for your design. Your floorplan may contain several non-overlapping LogicLock regions.

The use of LogicLock regions in a Stratix II FPGA is supported for designs migrating to a HardCopy II device. However, LogicLock regions are not passed into the HardCopy II companion revision. LogicLock regions are suggested for design partitions but are not migrated to the HardCopy II device, due to the difference in device architectures.

You can use LogicLock regions in the Stratix II design but you must create new LogicLock regions in the HardCopy II companion revision. To edit the properties of the LogicLock regions of a HardCopy II design, in the Quartus II software open the Assignments menu and choose **LogicLock Regions Window**. LogicLock regions in HardCopy II devices can have their properties set to **Auto** (by default) or **Fixed Size**. In addition, floating LogicLock regions are supported. You can adjust the size and location of the LogicLock regions you created in the HardCopy II device before compiling the design.



For more information about how to set the size and location of the LogicLock regions, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.



## Incremental Compilation

Quartus II incremental compilation supports two design methodologies: top-down and bottom-up. It enhances the standard Quartus II design flow by allowing you to reuse satisfactory results from previous compilations and save compilation time. However, bottom-up incremental compilation is not supported in HardCopy II ASIC and Stratix II FPGA compilations when using the migration device setting in the Quartus II software.

During HardCopy II device development in the Quartus II software, the top-down incremental compilation is supported for the base family for both the FPGA first and HardCopy first flows. Design partition assignments are migrated to the companion device. LogicLock regions are suggested for design partitions but are not migrated to the companion device, due to the different device architecture. However, you cannot make changes to the design after migration because the design would not match the compilation results for the base family. Therefore, you can perform top-down incremental compilation on one device family, but cannot perform any incremental compilations after migration.

The Netlist Only preservation level is not supported for Post-Fit netlists for Stratix II or HardCopy II device compilations when a migration device is specified (that is, for HardCopy ASIC device compilations with a FPGA migration device, or FPGA device compilations with a HardCopy ASIC migration device).

The complete incremental compilation flow using a top-down methodology (all partitions are contained in one top-level project) for the HardCopy first flow is described in these steps:

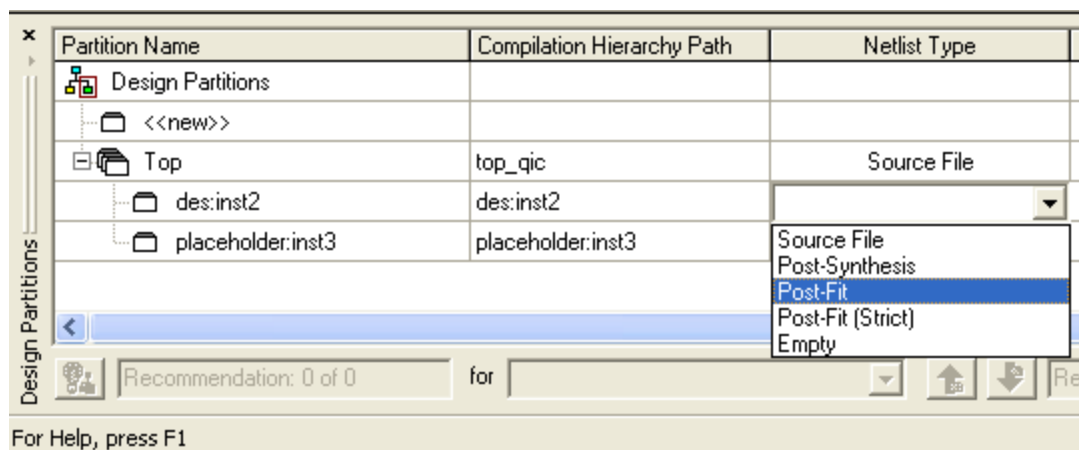
1. Elaborate the design for the Stratix II revision. On the Processing menu, point to **Start** and click **Start Analysis & Elaboration**, or run any compilation flow that includes this step. Elaboration is part of the synthesis process that identifies your design's hierarchy.
2. Create partitions in your design by designing specific instances called design partitions. In the **Project Navigator** window, on the **Hierarchy** icon  tab, click the + symbol next to the entity to expand the design hierarchy. Right-click on the entity you want to use as a design partition, and choose **Set as Design Partition**. The design partition icon  appears next to the entity.
3. Compile the design. On the Processing menu, click **Start Compilation**. The first compilation after creating a design partition and LogicLock assignments is a complete compilation that prepares the design for subsequent incremental compilations.

4. After compiling the design once and then making the RTL changes on the specific module(s), take advantage of incremental compilation. Use incremental compilation to recompile the changed parts of the design while preserving the results for the unchanged partitions. This saves time on subsequent compilations. To recompile the changed parts of the design, perform the following general steps:

- On the Assignment menu, click **Design Partition Windows**. Choose which of the following compilation results you intend to reuse for each partition:
  - To preserve previous placement results for a partition, set the **Netlist Type** assignment for that partition to **Post-Fit**.
  - To preserve routing information as well, set the **Fitter Preservation Level** to **Placement and Routing**.
  - To save only the synthesis results, set the **Netlist Type** assignment for that partition to **Post-Synthesis**.

For example, the "des" partition is set to reuse the previous compilation's fitter netlist, and preserve those placement results. Therefore, the **Netlist Type** assignment for the partition is set to **Post-Fit** as shown in [Figure 22](#).

**Figure 22.** Netlist Type Assignment for a Design Partition



Partitions with design changes are recompiled automatically with these Netlist Type settings. You can also direct the Quartus II software to recompile from the source code by choosing the **Source File** from **Netlist Type**. If you do not want to compile a specific partition at all, set its **Netlist Type** to **Empty**.

5. Compile the design. On the Processing menu, click **Start Compilation**. When you start a compilation for a partitioned design with incremental compilation turned on, the Quartus II software uses the incremental compilation flow, preserving the results you specified in Step 4.

After successfully compiling the design with incremental compilation turned on, you can create a HardCopy II companion revision. In the HardCopy II companion revision, incremental compilation is not supported. This is because changes to the design in the incremental compilation flow result in design discrepancies between a Stratix II revision and HardCopy II companion revision.

 For more information about incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.


### PowerPlay Power Analyzer

As FPGA designs grow larger and processes continue to shrink, power becomes an ever-increasing concern. When designing a printed circuit board, the power consumed by a device needs to be accurately estimated to develop an appropriate power budget, and to design the power supplies, voltage regulators, heat sink, and cooling system.

The Quartus II software allows you to estimate the power consumed by your current design during timing simulation. This section explains how to calculate the power consumption of your design using:

- Microsoft Excel-based power calculator
- Simulation-based power estimation features

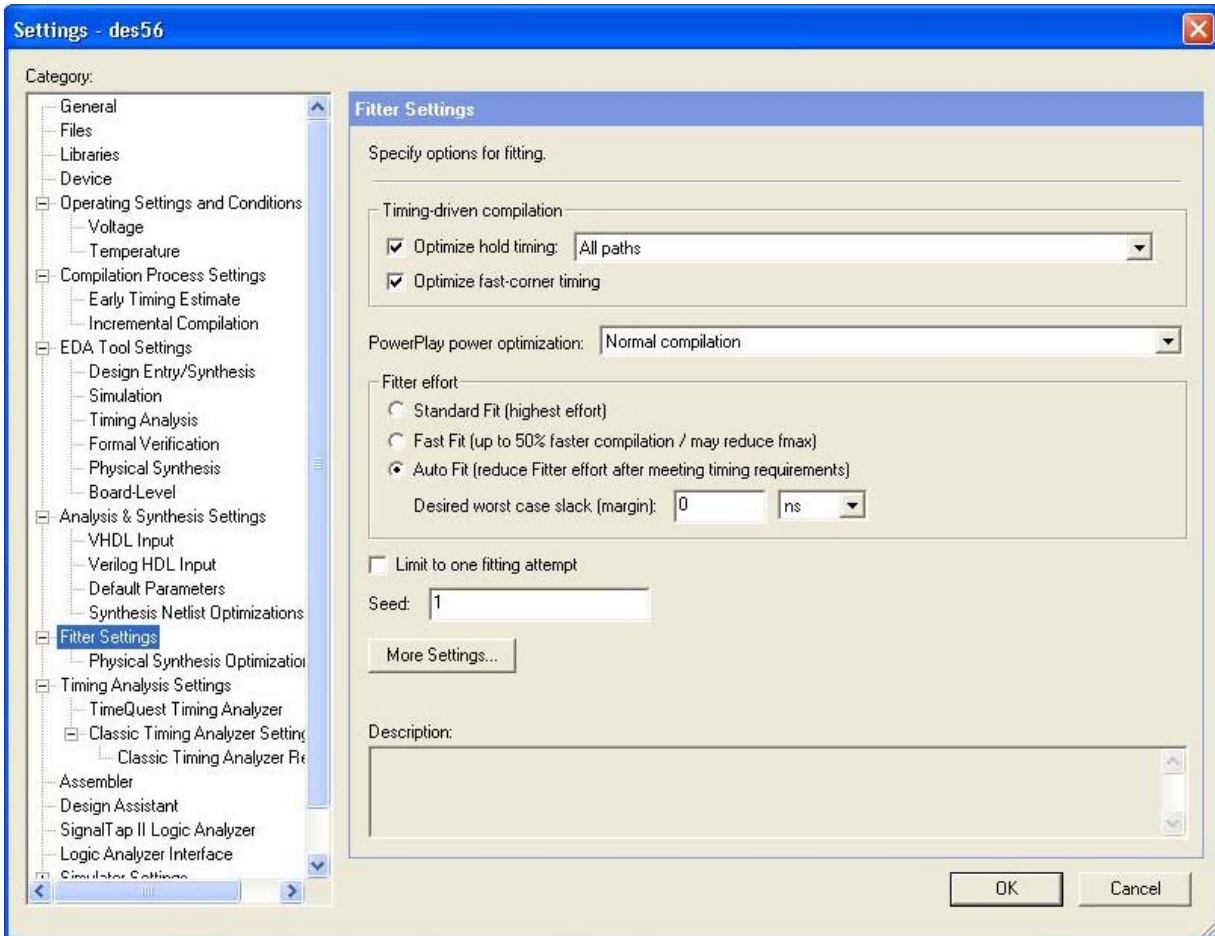
PowerPlay power analysis tools are designed for accurate estimation of power consumption from early design concept to design implementation. Designers can use the PowerPlay Early Power Estimator to estimate power consumption during the design concept stage. Power estimations can be refined during design implementation using the Quartus II PowerPlay Power Analyzer feature. The Quartus II PowerPlay Power Analyzer produces detailed reports that you can use to optimize designs for lower power consumption and verify that the design is within your power budget.

 For more information about using the Early Power Estimator, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

## HardCopy II Fitting

In order to make the HardCopy II device implementation more robust across process, temperature, and voltage variations, Altera's HardCopy Design Center requires that you enable the fast-corner optimization for the Quartus II Fitter. This setting enables the Fitter to optimize the design, meeting timing requirements for both the fast and the slow timing process corners and operating conditions. The HardCopy Design Center also requires that you enable the Optimize hold timing setting for the Quartus II Fitter. This setting allows the Fitter to optimize hold time by adding delay to the appropriate paths.

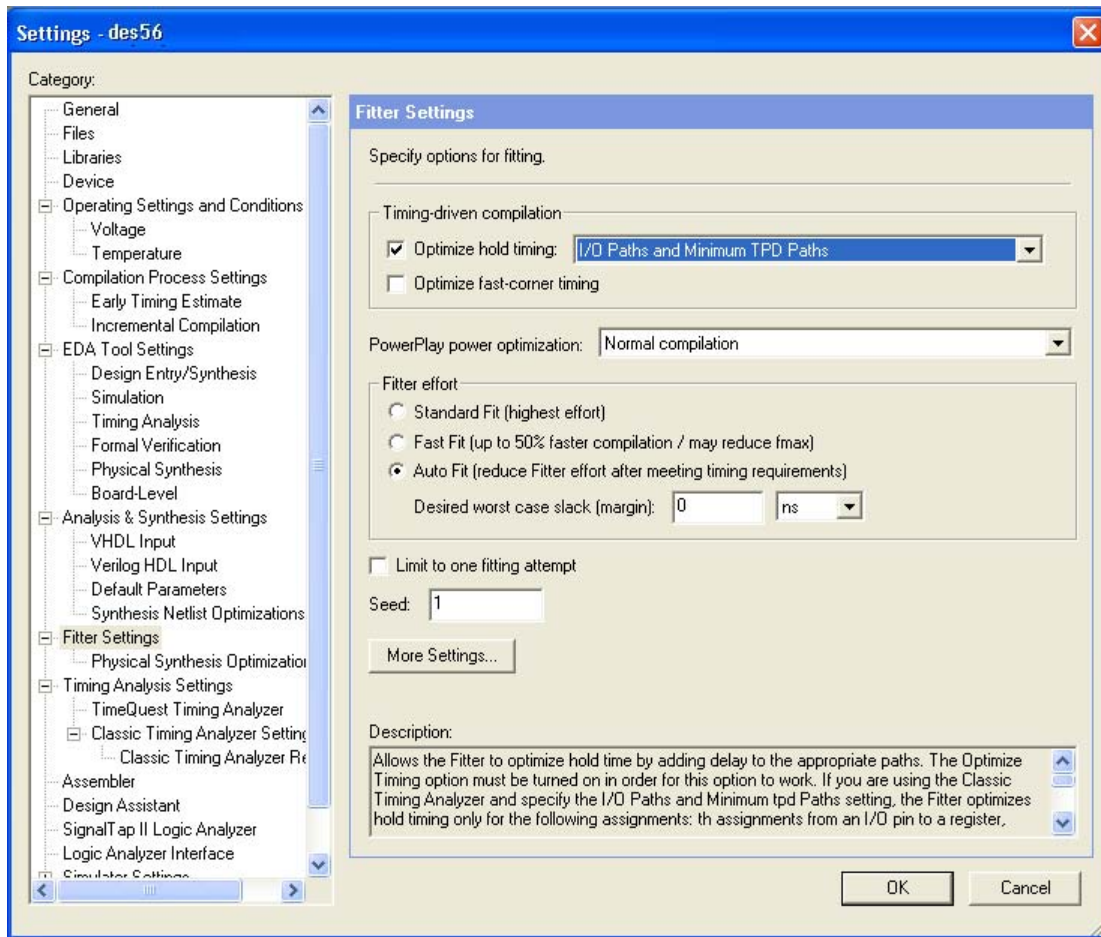
**Figure 23** shows the **Optimize fast-corner timing** and **Optimize hold timing** in the **Fitter Settings** window.

**Figure 23.** Quartus II Fitter Settings for Optimizing Fast Corner and Hold Time Fix

In some situations, your HardCopy II design may be hard to fit because nearly all the available routing resources are already used or there are routing congestions. Altera recommends two approaches to resolve HardCopy II fitting issues:

1. Turn off **Optimize fast-corner timing** and turn on **Optimize hold timing** for **I/O Paths and Minimum TPD Paths** as shown in [Figure 24](#).

**Figure 24.** Quartus II Fitter Settings for Optimizing Hold Time for I/O Paths and Minimizing TPD Paths

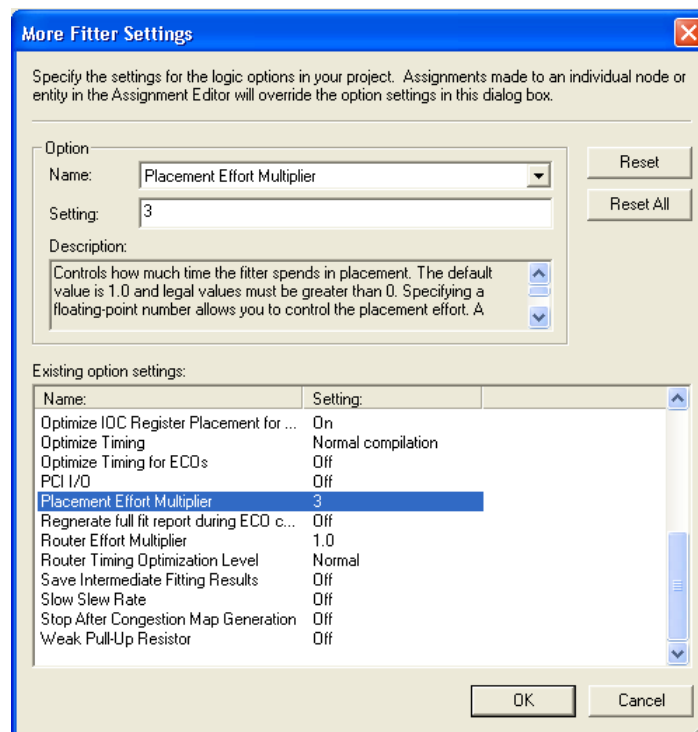


 Contact Altera's HardCopy Design Center before using these settings to ensure that the back-end tools are still able to close hold time requirements.

2. Set the **Placement Effort Multiplier** to as high as 3 to produce a better starting placement and improve routing.

Figure 25 shows the **Placement Effort Multiplier** set to 3 in the **More Fitter Settings** dialog box.

**Figure 25.** Placement Effort Multiplier



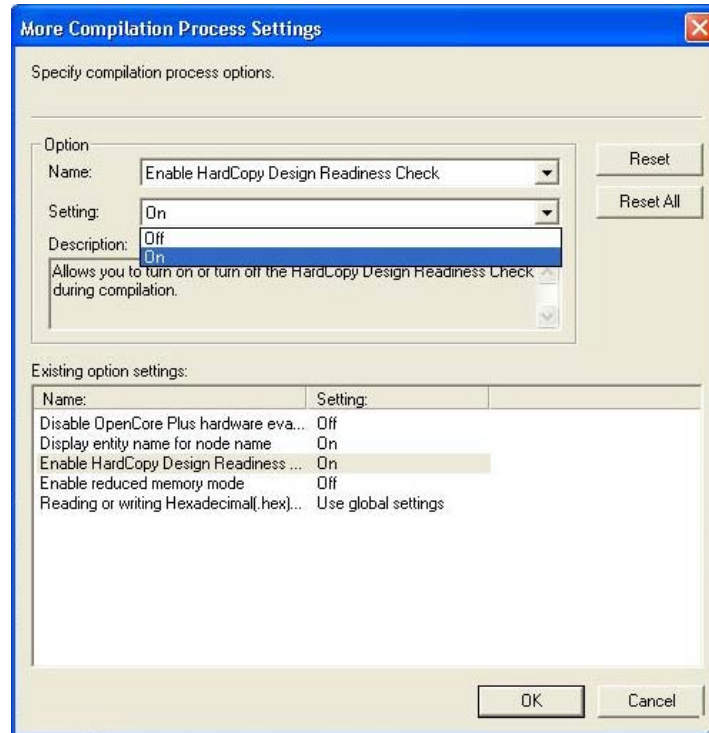
For more information about fitting in the Quartus II software, refer to [AN 453: HardCopy II Fitting Techniques](#).

## HardCopy Readiness Overview

The HardCopy Design Readiness Check (HCDRC) feature checks issues that must be addressed before handing off the HardCopy II design to the Altera HardCopy Design Center for the back-end processing. In the Quartus II software, the HCDRC includes logic checks such as PLL, RAM, and setting checks (**Global Setting**, **Instance Setting**, and **Operating Setting**) that were previously done in the HardCopy hand-off report. With the Quartus II software version 8.0, the default setting for running HCDRC is **On**. You can run HCDRC at post-Fitter either turned on through QSF or the GUI, as follows:

```
set_global_assignment -name \
FLOW_HARDCOPY_DESIGN_READINESS_CHECK ON\
set_global_assignment -name\
FLOW_HARDCOPY_DESIGN_READINESS_CHECK OFF
```

The tool can also be turned on through the GUI, as shown in [Figure 26](#).

**Figure 26.** HardCopy Design Readiness Check in Quartus II Software

For more information about the HardCopy Design Readiness Check, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

## Timing Closure and Verification

After compiling the project for the Stratix II and HardCopy II designs, check the device used and verify that the designs meet your timing requirements. Analyze the messages generated from the Quartus II software during compilation to check for any potential problems. You must also verify the design functionality between a Stratix II FPGA and a HardCopy II device with the Compare HardCopy Companion Revision option in the Quartus II software.

### Timing Analysis of the Prototype Stratix II Device

You should perform optimization and timing analysis for the Stratix II FPGA prototype of the design before migrating it to the HardCopy II companion revision. Timing analysis determines whether the design's performance meets the timing requirements. If the timing analysis results do not meet your requirements, modifying the constraints for synthesis or compilation may be necessary. If timing meets your requirements, the Stratix II implementation of your prototype design can be used in a chip-level environment.

## Timing Analysis of the HardCopy II Device

After the Stratix II design achieves the timing requirements, is fully tested in-system, and satisfies the HardCopy design rules, the design can be migrated to a HardCopy II companion revision. The Quartus II software performs rigorous timing analysis on the HardCopy II device during its implementation, ensuring that it meets the timing requirements. The timing analysis must be done for both setup and hold time checks on all design paths, including internal paths and input and output paths.

It is important to meet the timing requirements constrained in the Quartus II software, the actual Stratix II FPGA prototype timing you observe in the hardware is not duplicated in the HardCopy II ASIC. The timing differences between the Stratix II FPGA and the HardCopy II ASIC are inconsequential as long as both are checked against a complete set of timing constraints. The timing differences may result in the timing performance gain for HardCopy II ASIC over Stratix II FPGA. While maintaining the same set of features as the corresponding Stratix II FPGA, a HardCopy II device has a highly optimized die size and custom interconnect routing structure to make it as small as possible. That improves the timing performance in HardCopy II ASIC.

## Timing Constraints Using the TimeQuest Timing Analyzer

The TimeQuest Timing Analyzer is a powerful ASIC-style timing analyzer tool that validates the timing performance of all logic in your design. The TimeQuest Timing Analyzer requires .sdc format, which is ideal for constraining high-speed source-synchronous interfaces and clock multiplexing design structure.

In the HardCopy II migration flow, timing-driven synthesis and fitting achieve the optimal result with accurate timing constraints.

To account for clock effects, such as clock jitter, duty cycle distortion, and phase shift error in the HardCopy II device, clock uncertainty must be added into the .sdc file of HardCopy II revision for timing analysis. In the Quartus II software, you can use the command `derive_clock_uncertainty` to automatically derive the clock uncertainties in your SDC file. This command is useful when you are unsure what the clock uncertainties might be. The calculated clock uncertainty values are based on I/O buffer, static phase errors (SPE), and jitter in the PLLs, clock networks, and core noise.

Following is a guideline for writing a TimeQuest constraint file for a typical design in .sdc format:

```
*****
# Create Clock
*****
# Constraints for base clocks would be in this section

*****
# Create Generated Clock
*****
# PLL and internally generated clocks would be in this
# section

*****
# Set Clock Latency
*****
```

```
# Based on your board parameters you may or may not
# have clock latency constraints

#####
# Set Input Delay
#####
# Constrain all your input pins in this section.
# Separate the input delays according to clock domain.
# If possible explain how the numbers were obtained!

#####
# Set Output Delay
#####
# Constrain all your output pins in this section

#####
# Set Clock Groups
#####
# Constrain unrelated clocks in your design in this section

#####
# Set False Path
#####
# If your design has any false paths, set them in this section
# You may want to use set_clock_groups -exclusive instead

#####
# Set Multicycle Path
#####
# Multicycle paths can be constrained in this section

#####
# Set Maximum Delay
#####
# Set maximum delay constraint for your design in here

#####
# Set Minimum Delay
#####
# Set minimum delay constraint for your design in here.

#####
# Set Clock Uncertainty
#####
# Clock Uncertainty for the HardCopy II revision goes here
if {${::TimeQuestInfo(family)} == "HardCopy II"} {
# HCII Specific constraints can be placed here
# For example
# Clock Uncertainty(CU) which is only needed in HCII
```

```
# FPGA Timing model is pessimistic so CU not needed - you can
# still model CU in an FPGA if you want to, just use the
# following constraint outside of this TCL construct.

derive_clock_uncertainty
}
```

## FPGA and HardCopy Revisions Verification

Altera uses the companion revisions in a single Quartus II project to maintain compatibility between the Stratix II FPGA and HardCopy II ASIC. This methodology allows you to design with one set of Register Transfer Level (RTL) code to be used in both the Stratix II FPGA and the HardCopy II ASIC, guaranteeing functional equivalency.

When making changes to the companion revisions, use the **Compare HardCopy Companion Revisions** command to ensure that your design matches your HardCopy II design functionality and compilation settings. To compare companion revisions, on the Project menu, point to **HardCopy Utilities** and click **Compare HardCopy Companion Revisions**.



You must perform this comparison after both the Stratix II FPGA and HardCopy II designs are compiled to hand off the design to Altera's HardCopy Design Center.

The Comparison Revision Summary is found in the Compilation Report. It identifies where assignments were changed between revisions or if there is a change in the logic resource count due to different compilation settings.

## HardCopy II ASIC Handoff Process

To submit a design to Altera's HardCopy Design Center for design review and back-end implementation, you must generate a HardCopy II handoff report and archive the HardCopy II project. Before you generate the HardCopy II handoff report, you must first successfully perform the following tasks:

- Compile both the Stratix II and HardCopy II revisions of the design.
- Run the Compare HardCopy Companion Revision utility.

Then you must archive the HardCopy II project for submission to the HardCopy Design Center for back-end implementation. This is the last step in the HardCopy II design flow. The HardCopy II archive utility creates a different Quartus II Archive File (**.qar**) than the standard Quartus II project archive utility generates. This archive contains only the necessary data from the Quartus II project needed to implement the design in the HardCopy Design Center.

To use the Archive HardCopy Handoff Files utility, you must perform all tasks for generating a HardCopy II handoff report.

After a HardCopy II handoff report is generated, you can select the handoff option. On the Project menu, point to **HardCopy Utilities** and click **Archive HardCopy Handoff File utility**.

The Archive HardCopy Handoff File utility archives your design, settings, results, and database files for delivery to Altera. These files are generated at the same directory level as the targeted project created with an `_hcii` extension. [Example 1](#) shows some of the files collected by the Archive HardCopy Handoff Utility.

**Example 1.** Example Files Collected by the Archive Copy Handoff Utility

---

Timing Constraints File: `<project_name>_hcii_constraints.sdc`  
Placement File: `<project_name>_hcii.qpef`  
Routing File: `<project_name>_hcii.qref`  
Post-Fitting Netlist: `<project_name>_hcii.v`

---

## Conclusion

This application note provides a set of guidelines when designing the Stratix II FPGAs and the HardCopy II companion devices. To achieve robust results, avoid common issues, and improve your design productivity, follow the recommendations throughout the design process. These guidelines ensure that your design is ready to be handed off to Altera's HardCopy Design Center for back-end processing.

## Referenced Documents

This application note references the following documents:

- [AN 432: Using Different PLL Settings Between Stratix II and HardCopy II Devices](#)
- [AN 453: HardCopy II Fitting Techniques](#)
- [Assignment Editor](#) chapter in volume 2 of the *Quartus II Handbook*
- [DC and Switching Specifications and Operating Conditions](#) chapter in the *HardCopy II Device Handbook*
- [Description, Architecture, and Features](#) chapter in volume 1 of the *HardCopy II Device Handbook*
- [Design Recommendations for Altera Devices and the Quartus II Design Assistant](#) chapter in volume 1 of the *Quartus II Software Handbook*
- [I/O Management](#) chapter in volume 2 of the *Quartus II Handbook*
- [Migrating Stratix II Device Resources to HardCopy II Devices](#) in volume 2 of the *HardCopy II Device Handbook*
- [Netlist Optimizations and Physical Synthesis](#) chapter in volume 2 of the *Quartus II Handbook*
- [Package Information for Stratix II and Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II Device Handbook*
- [PLLs in Stratix II and Stratix II GX Devices](#) in volume 2 of the *Stratix II Device Handbook*
- [Power Estimation and Analysis](#) chapter in volume 3 of the *Quartus II Handbook*
- [Power-Up Modes and Configuration Emulation in HardCopy Series Devices](#) chapter in the *HardCopy Series Handbook*

- *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*
- *Signal Integrity with Third-Party Tools* chapter in volume 3 of the *Quartus II Handbook*
- *Switching to the Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*
- *White Paper: Input Signal Edge Rate Guidance*

## Document Revision History

**Table 14.** Document Revision History

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
September 2008, v1.0	Initial release.	—